Designer's Guide Consulting

Bridging the gap between design and EDA

Trends in RF/Mixed-Signal Design and Its Implications on Computer Aided Design

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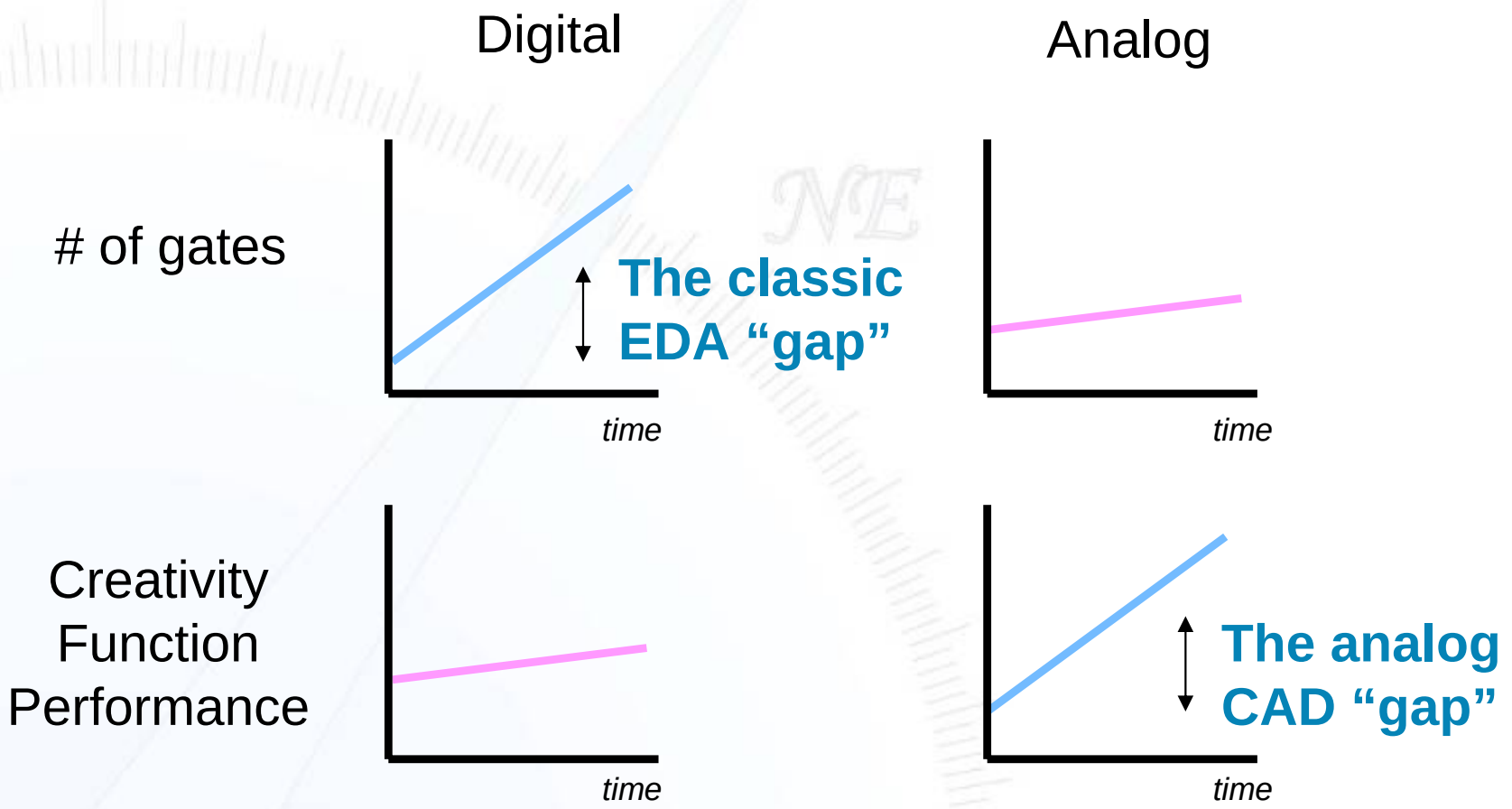
9/22/05

Bridging the GAP



Outline

- Design Drivers
- Design Challenges
- Addressing Challenges
  - Design Teams
  - Methodology and CAD
- Conclusions

The Morning Paper

Friday's Fry's Electronics circular-
8 pages of the electronics
***We Make*!!!**

With "Cool" Mixed-Signal Chips

***Best Buy and CompUSA ads also**

Latest and More Expensive

***Best Buy and CompUSA ads also**

New Technology Premium

600% Premium!!!!

800%

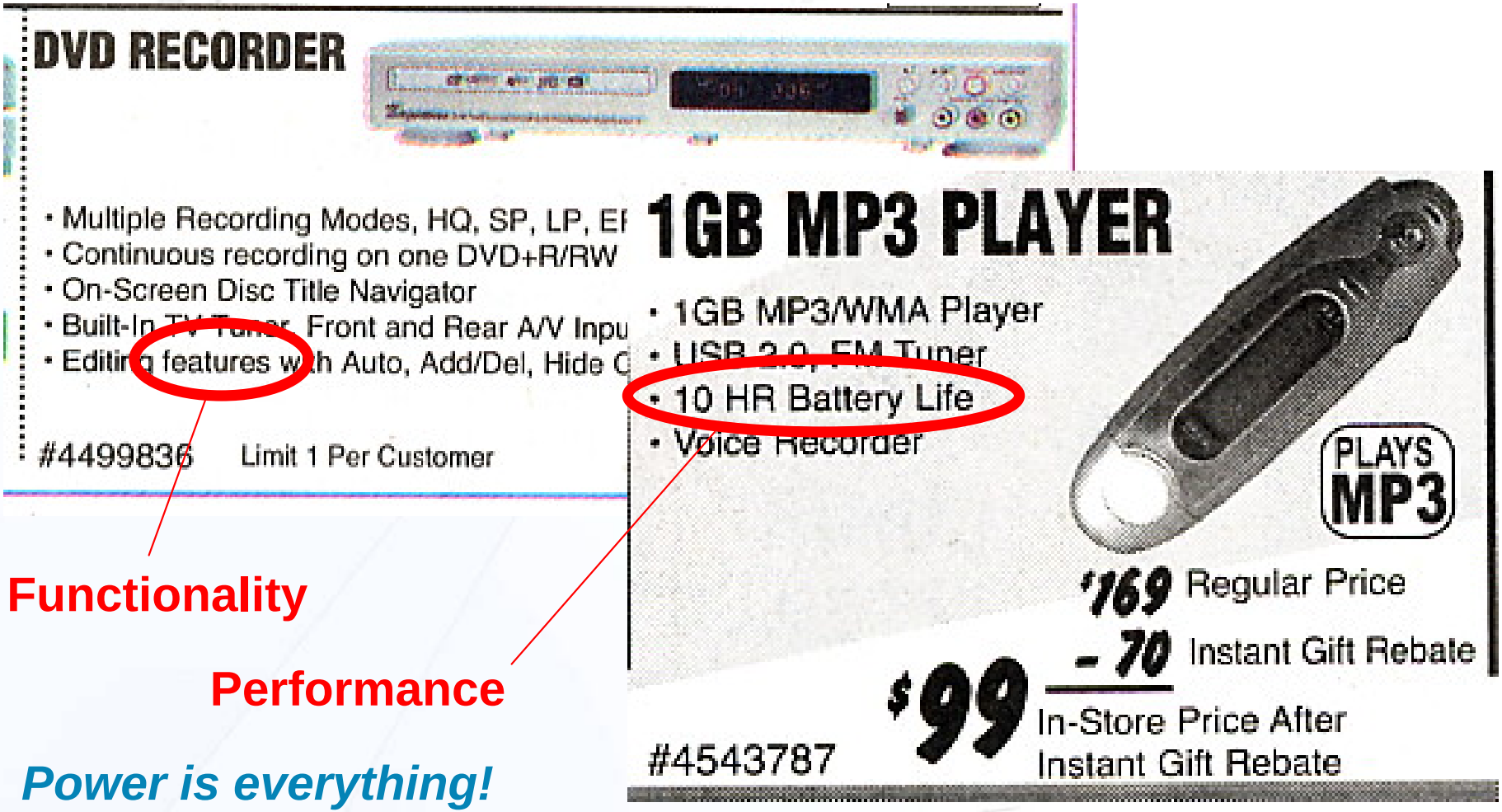
Could Be Worse

Software

Free

Bright Spot

Not Just Cost



Functionality

Performance

Power is everything!

One Device, Do Everything

- 3D Video Games
- Streaming Video
- MP3 Player
- Bluetooth
- Mobile Web
- 1.3MP Camera
- Video Camera
- Speakerphone
- Voice Dial
- Mini SD Card
- Address Book
- Speed Dial

4 oz, 4 hour talk, 1 week standby

Fierce Competition

End Products

Selection

Prototypes

"Design In"

ICs

No margin for error!

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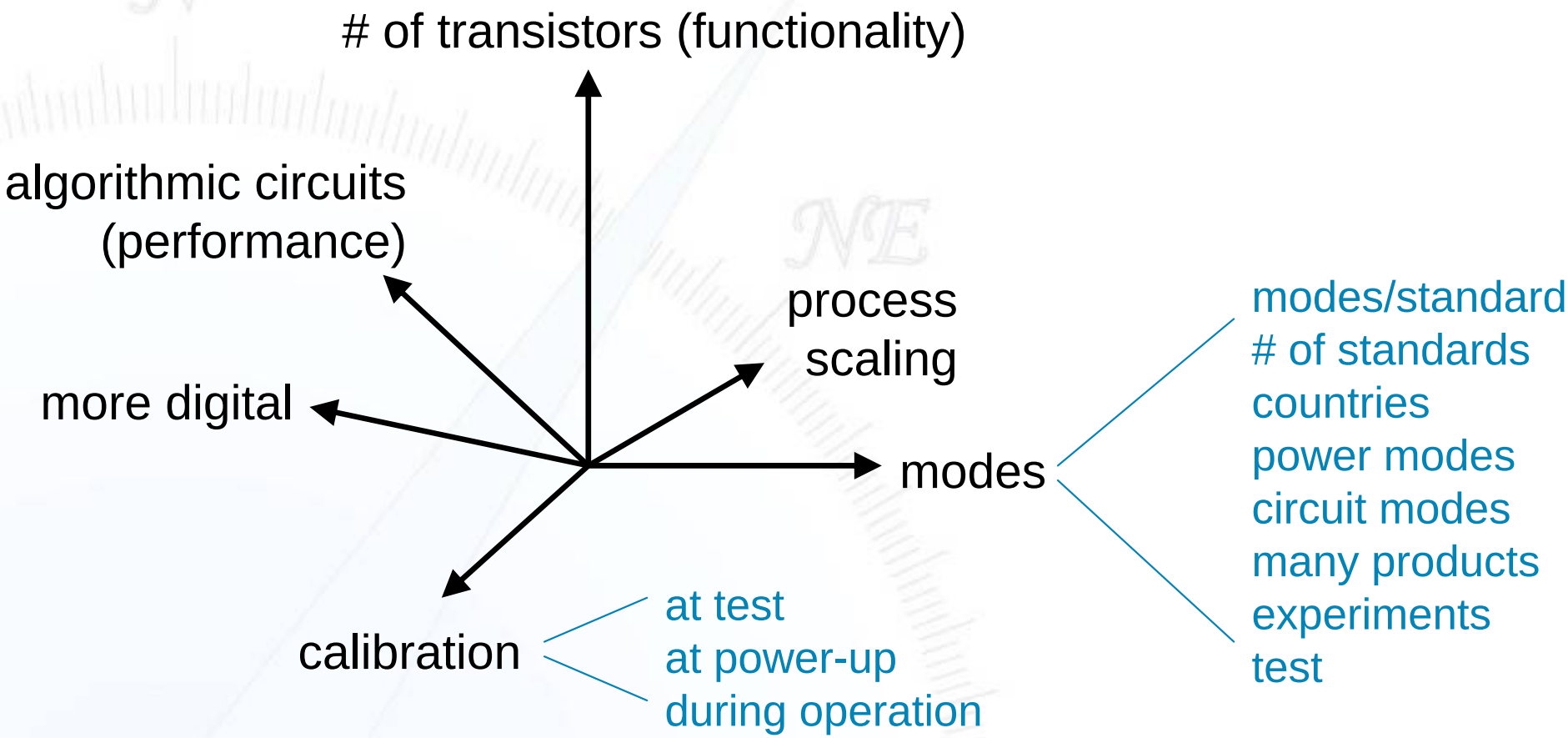
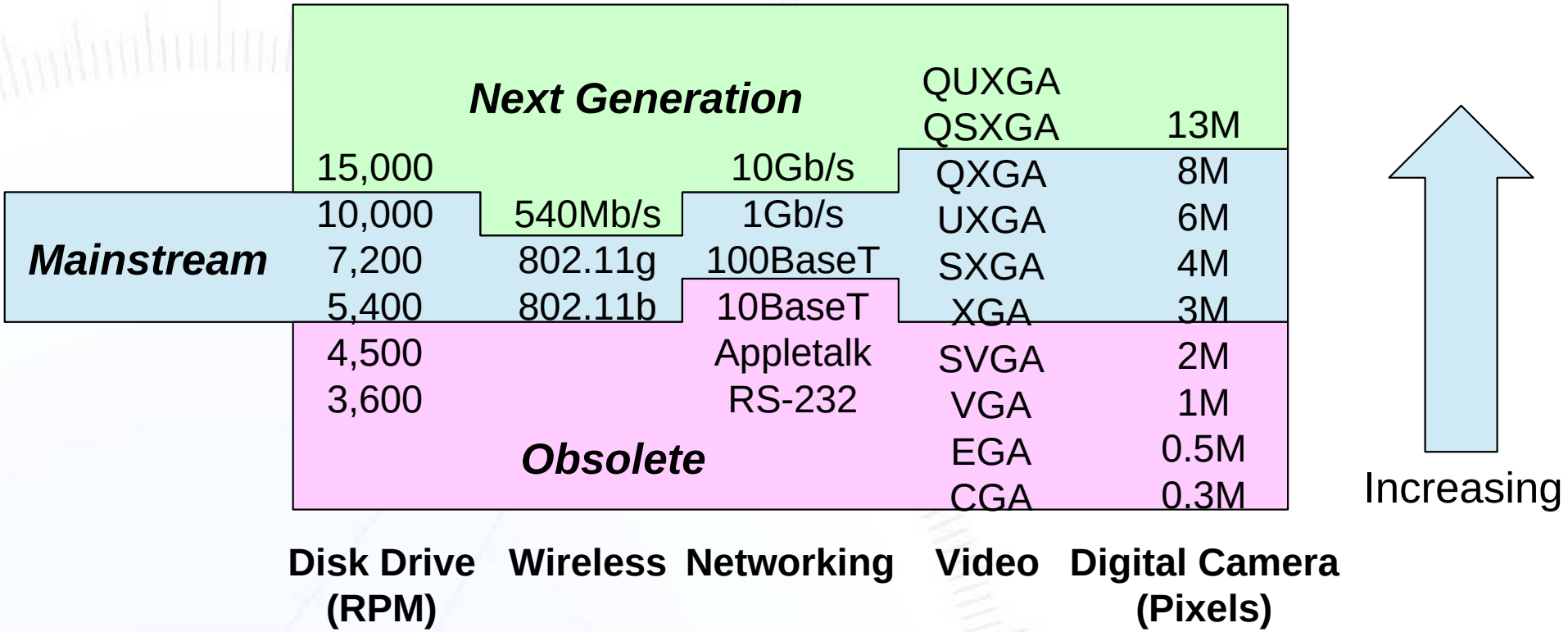
Design Challenges

- Functionality
  - Many standards
  - Adaptable to different end products
- Performance
  - Specifications and exceeding them
  - Low power
- Cost
  - High yield
  - Small die area
- All before the holidays!
  - Design productivity
  - Design quality
  - Fast ramp to volume
- Repeatable

Complexity

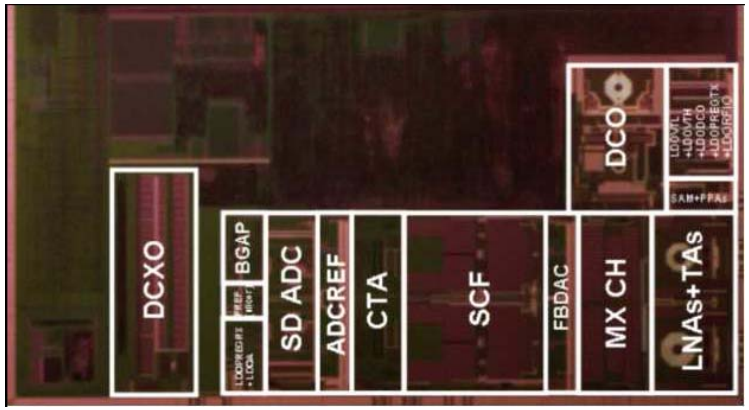


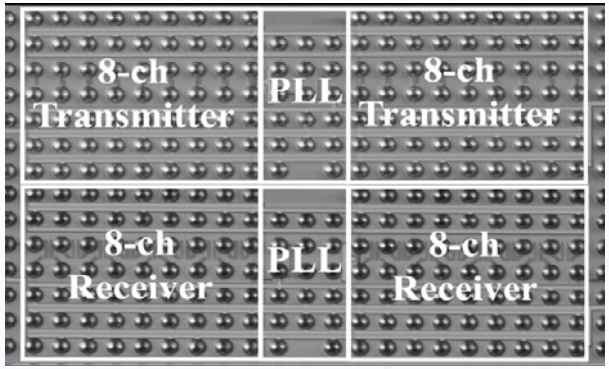
Performance



CICC 2005 Examples

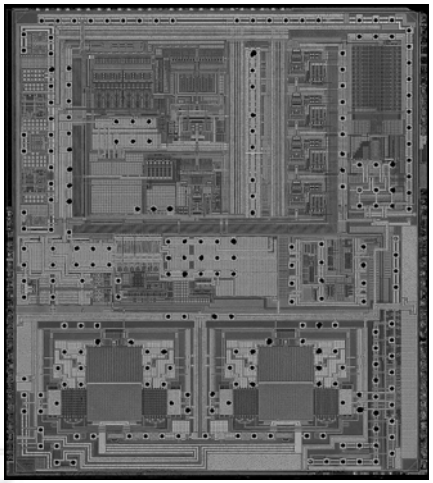
A Discrete Time Quad-band GSM/GPRS Receiver in a 90nm Digital CMOS Process [1]





A 0.8-1.3V 16-channel 2.5Gb/s High-speed Serial Transceiver in a 90nm Standard CMOS Process [2]

A Highly-Integrated CMOS Analog Baseband Transceiver with 180MSPS 13b Pipelined CMOS ADC and Dual 12b DACs [3]



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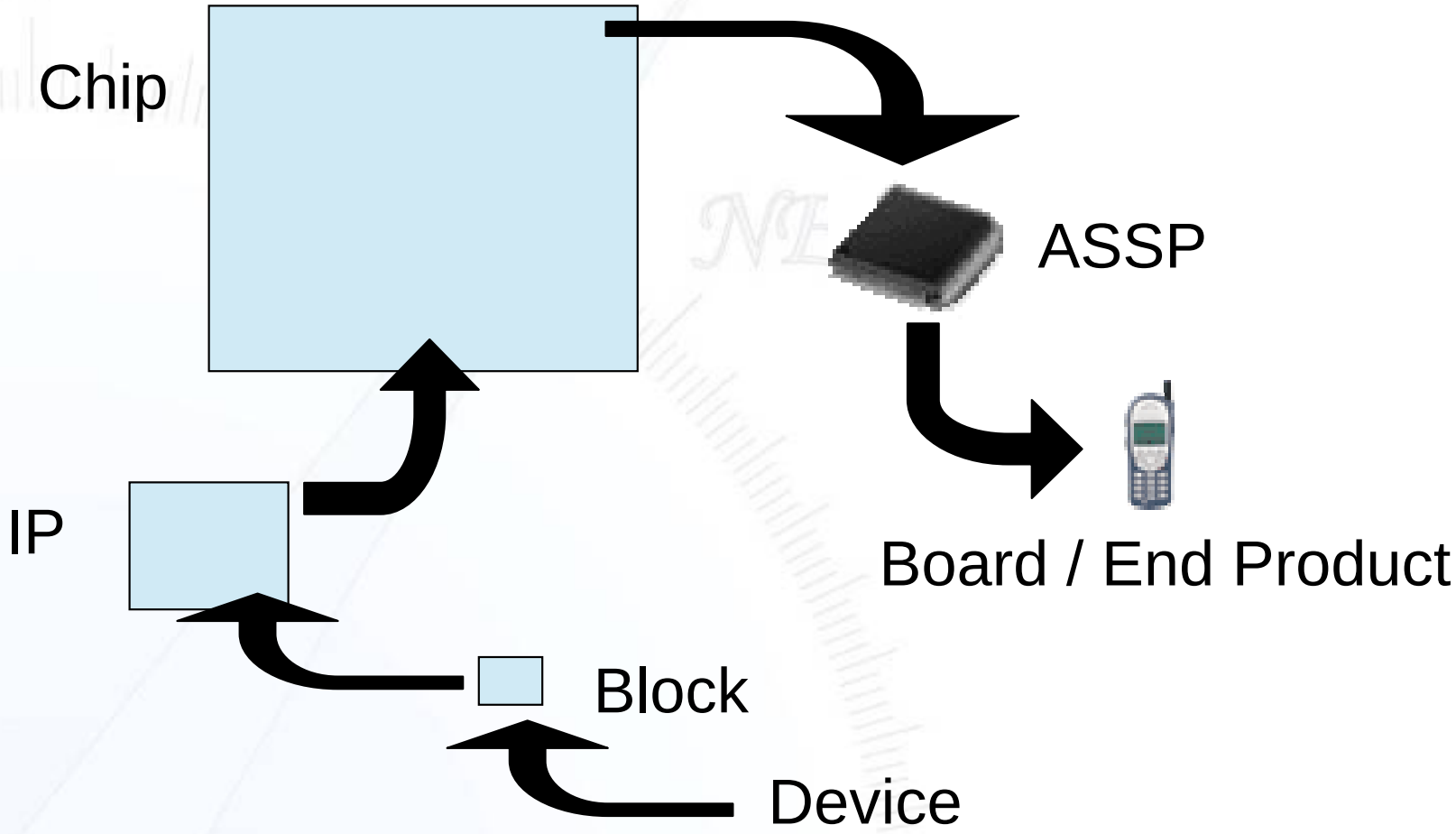
Design Levels



Design Teams

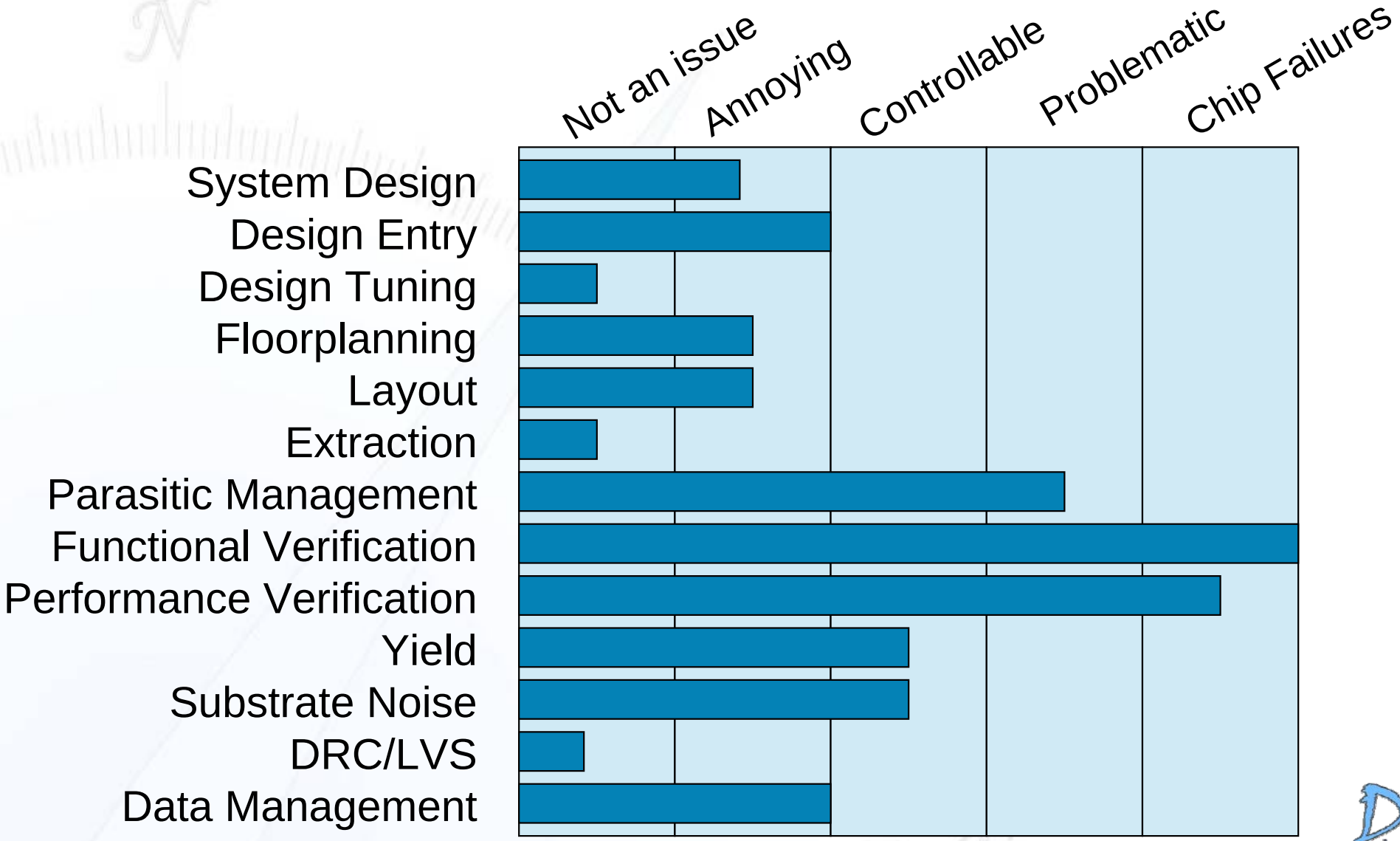
Design Level	Designer/Team	Cause of Sleepless Nights
Analog Block	Analog Designer	Function, Performance
Analog IP	Design Lead	Architecture, Function, Performance, IP Packaging
Chip	System Designer	Architecture, Performance
	Implementation	Schedule, Integration, Function
	Verification Engineer	Function (Performance)
ASSP	Production Engineer	Design for Test, Yield
	Business Owner	Schedule, Customer Relationship
End Product	"Customer"	System "Bring Up"

Own concerns ***plus*** communicating with others

Complex Communication

- Geography / time zone / language
- Different concerns
- Different design domains
- Different design languages

The Problem



Verification Issues

- Chip Functional Verification
- IP Functional Verification
- IP Performance Verification
- Block Performance Verification

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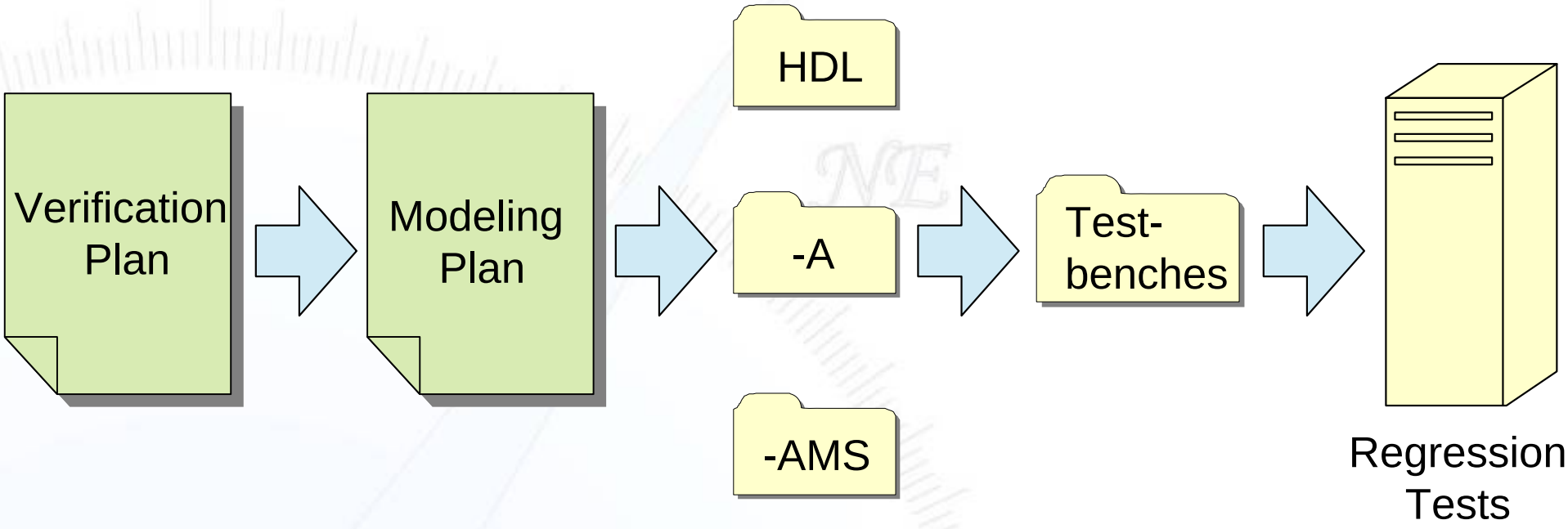
Top-Down Verification

- Verification planning
- Shared design representations
- Verification of each design change
- Continual refinement w/quick initial iteration
- Executable models and scripts used daily

Flow



Must be owned by design team and be an integral part of design process

Navigating the Details

- Verilog vs. VHDL?
- Verilog vs. Verilog-A vs. Verilog-AMS?
- When mixed-level? When mixed-mode?
- Level of model? How many levels?
- How to verify models?
- Verification vs. design models?
- Effort to invest?
- Build generic models?
- How to integrate with design?
- Who writes models?
- Purpose of each model? Concerns? What to model?
- Customer of model?
- Spice transient vs. timing simulator?
- Where does Matlab fit in?
- ***How to help design not impact design?***

Design vs. Verification

Design

Scratch Pad

Excel, Matlab, Models

Parametric Selection

Verification

Full functional verification

Full performance verification

Regression Testing

Monte Carlo / Corners Analysis

Are the same models used?
Same person for both tasks?

Analog Verification Engineer

- Modeling expert (digital and analog)
- Paired with analog IP design lead
- Understands top-down verification
- Understands simulation technologies
- Focuses on verification and delivering models to customers (internal and external)

The Real Issues

- Work jointly with designers
- Talk to designers
- Test ideas with them
- Read about what they are struggling with http://www.designers-guide.org/

Conclusions

- Fierce competition driving design
- Analog design is multi-dimensional
- Analog verification changing
- New methodologies required
- Analog behavioral modeling has new roles to play

Portable Music

- First AM/FM "walkman"
  - 25 years ago
  - $285 (adjusted for inflation)
  - 4 x AA batteries
  - Stereo
- FM/MP3 Player
  - $60
  - 1 x AAA battery
  - CD Quality
  - < 20% of the weight

Buyer's Remorse

References

[1] K. Muhammad et al, "A Discrete Time Quad-band GSM/GPRS Receiver in a 90nm Digital CMOS Process," *IEEE CICC Proceedings*, September 2005.

[2] Y. Doi et al, "A 0.8-1.3V 16-channel 2.5Gb/s High-speed Serial Transceiver in a 90nm Standard CMOS Process, " *IEEE CICC Proceedings*, September 2005.

[3] K. Gulati et al, "A Highly-Integrated CMOS Analog Baseband Transceiver with 180MSPS 13b Pipelined CMOS ADC and Dual 12b DACs," *IEEE CICC Proceedings*, September 2005.