Design Methodologies for Advanced Low Power Communication Circuits and Systems

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Motivation

Present case studies from the design of multiple layers of a wireless sensor network platform

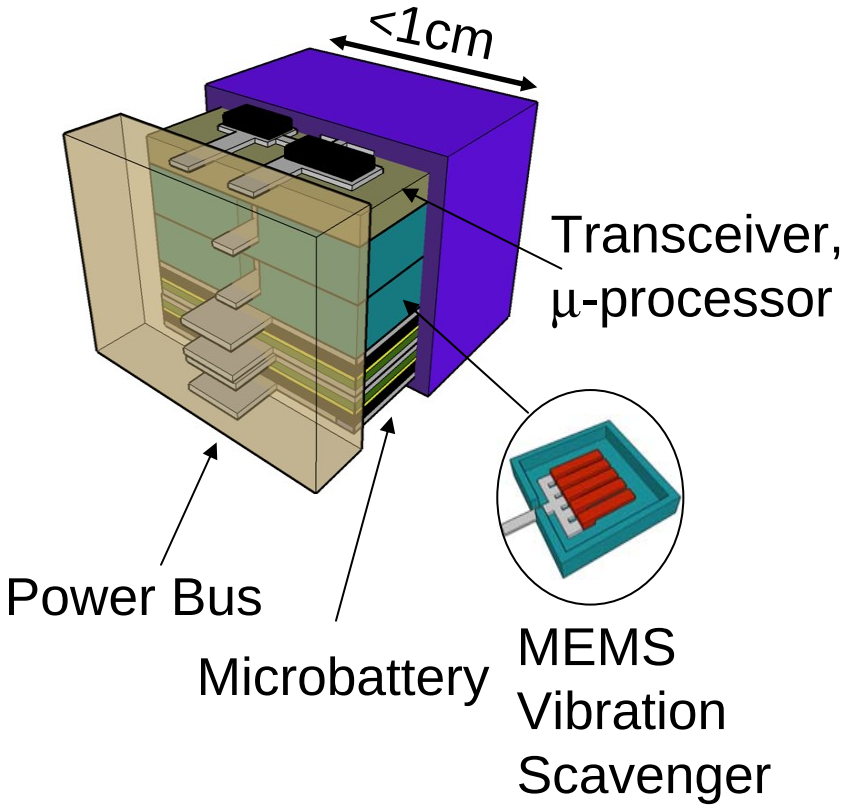
Show current methodologies, representative results, and difficulties with these methods

Observation: simulation across disciplines, not just technologies, is crucial for the success of future ultra-small electronic systems

I will highlight important questions that we were not able to answer with our current methodology

Application: Wireless Sensing

Nodes must be small (<1cm^3) & self-contained (use energy scavenging)



This network would allow:

- Saving energy in building environments
- Tire pressure monitoring
- Wildlife monitoring
- Radiation monitoring
- Biological and implantable devices

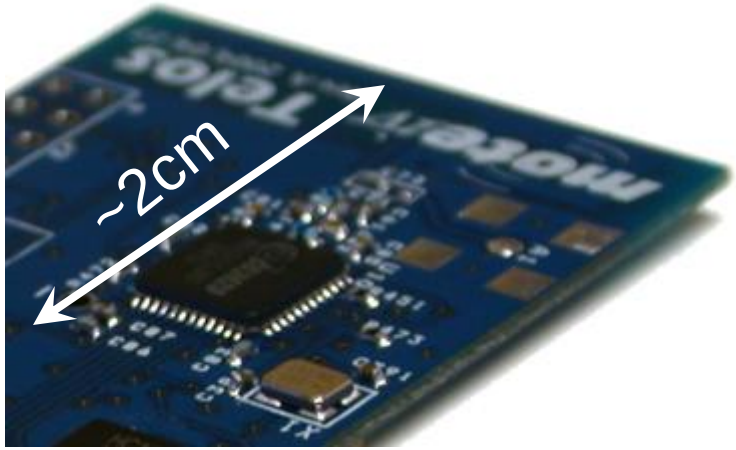
Why is this difficult?

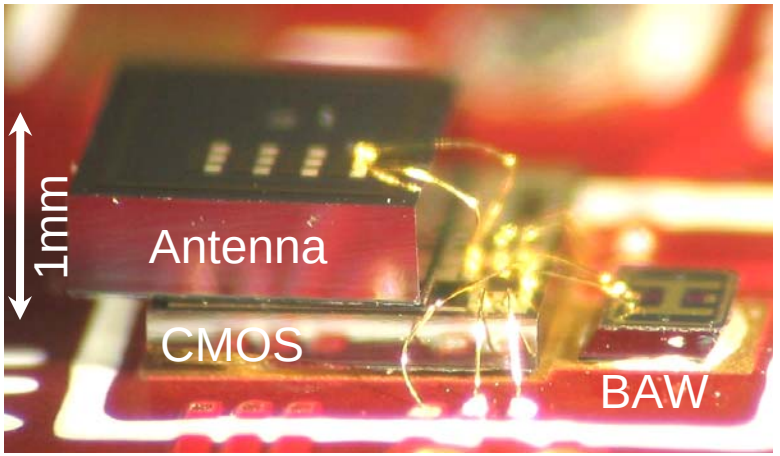
The environment is inherently energy starved

Confluence of many technologies, all of which are at their state-of-the-art (necessary to reduce form-factor and power dissipation over current solutions)

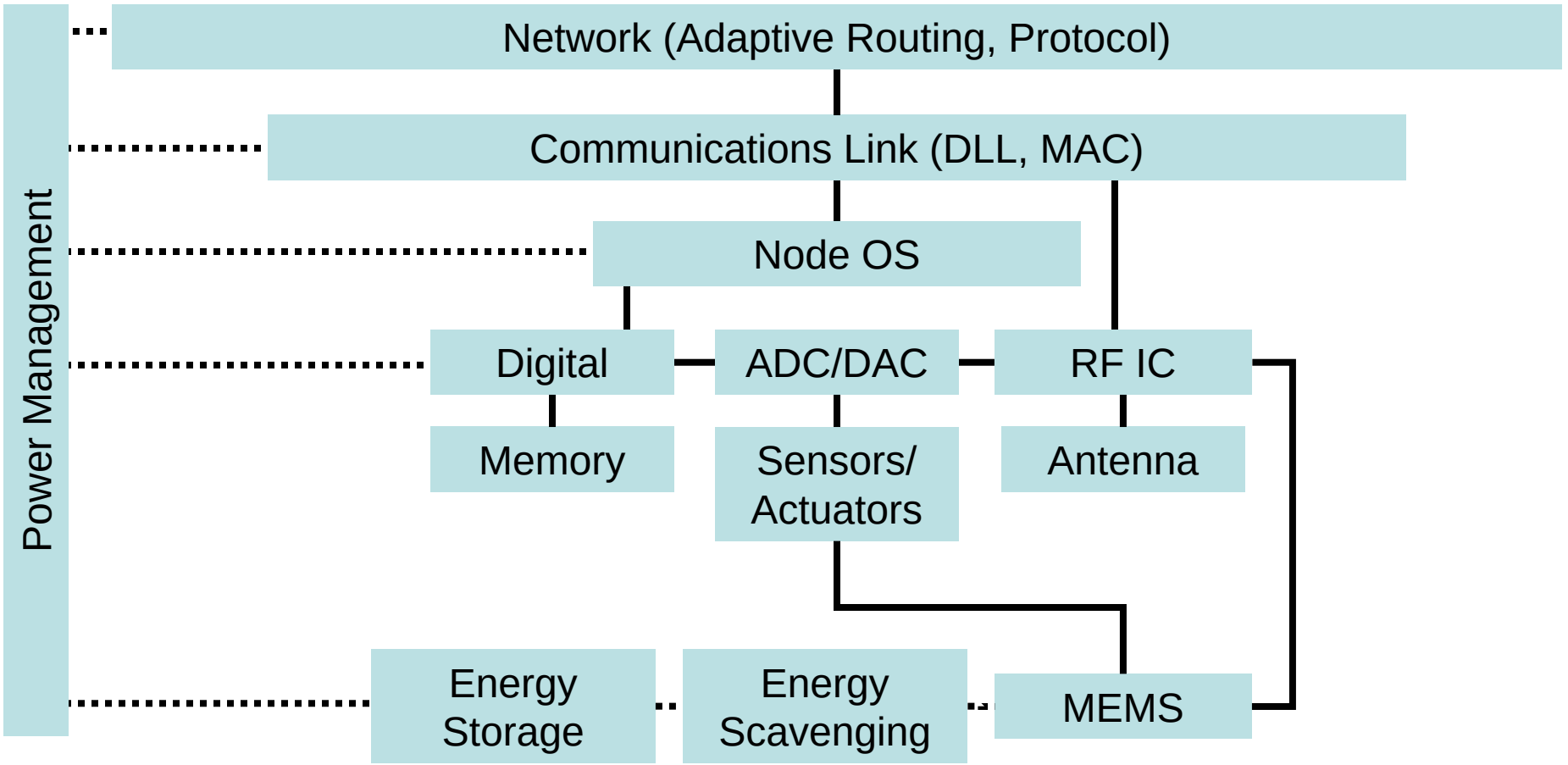
Large, ad-hoc networks assembled non-deterministically

Must communicate reliably over uncertain RF links



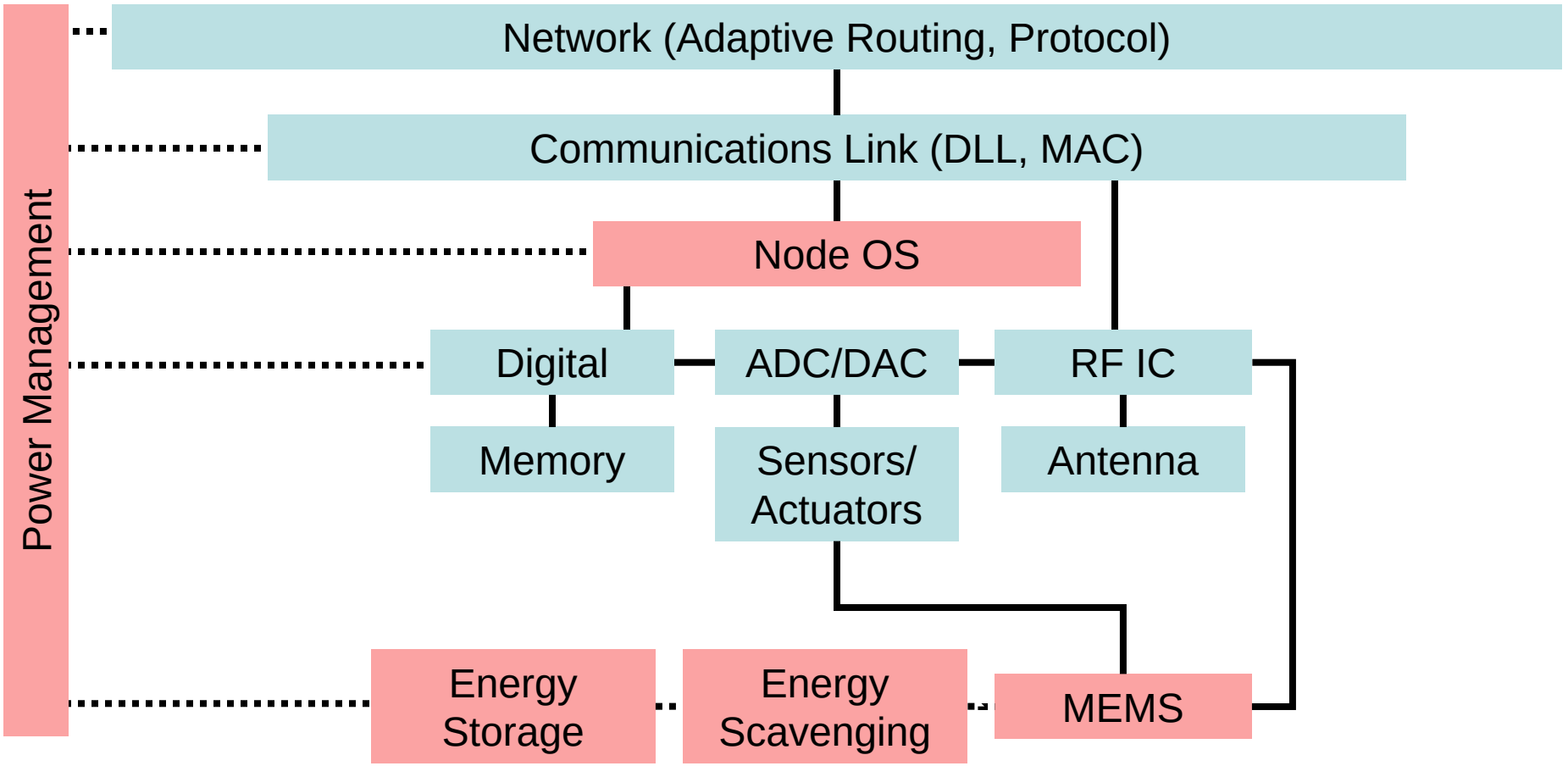


Sensor Network Hierarchy



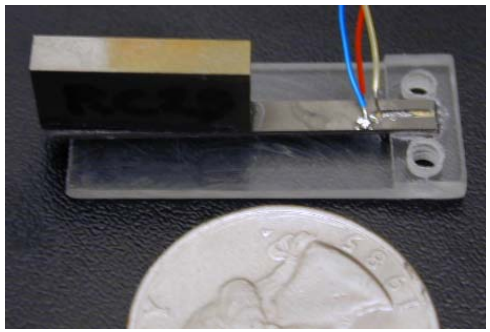
Must break down traditional abstractions and interfaces between systems and technologies to maximize efficiency

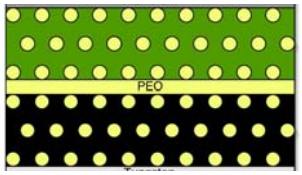
Part I: Power Distribution

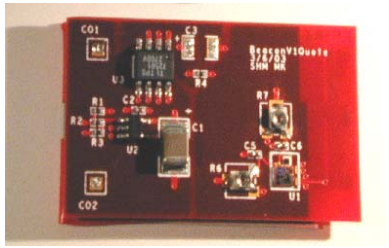


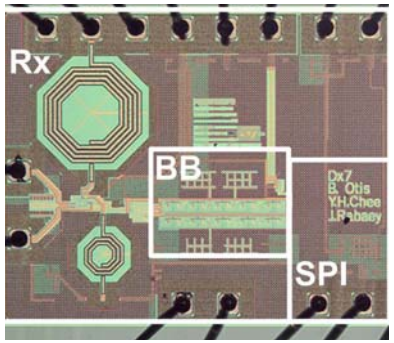
- Want indefinite operation from environmentally scavenged energy
- Power generation & management crucial

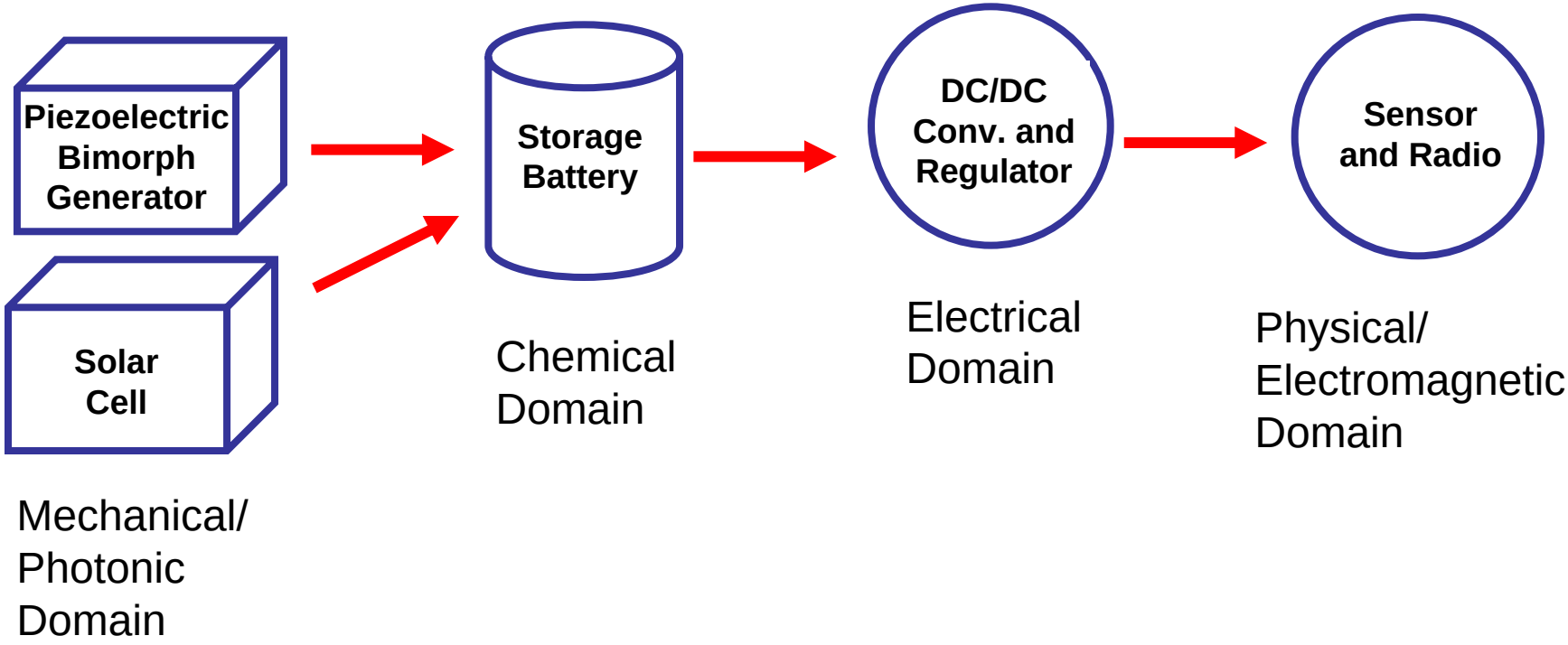
Energy Scavenging Power Train





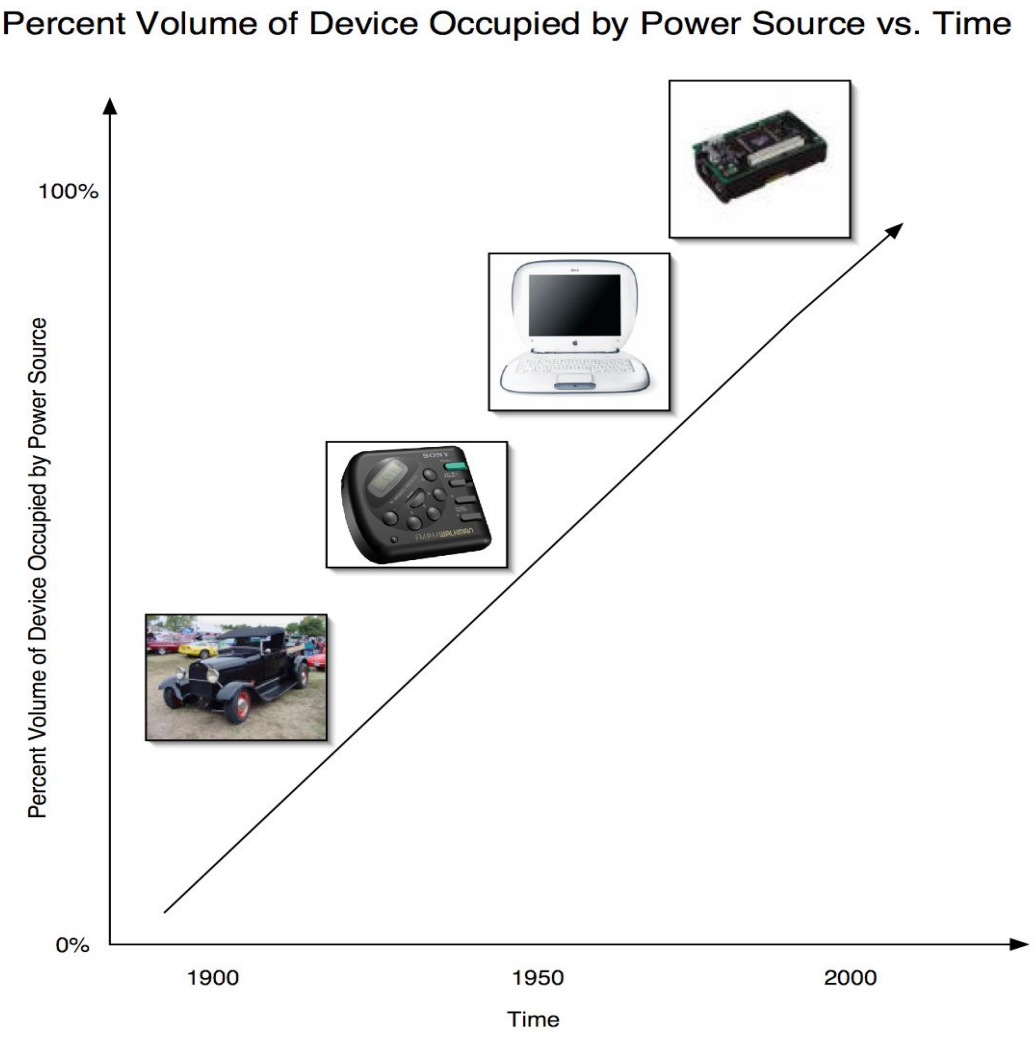






Thin-Film Battery Simulation

- Current sensor nodes are 80% - 90% battery by volume
- Must reduce power consumption and increase battery integration



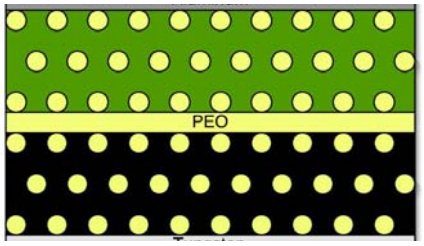
Courtesy: Dan Steingart

Small Battery Overview

1mm by 4mm^2

30µm by 3cm^2

400µm by 1cm^2



- Conventional
  - Thick Electrodes (400µm each)
  - Liquid Electrolyte
  - Built for Capacity (small surface area)
- Superflat
  - Sputtered Electrodes
  - Solid Polymer Electrolytes
  - Built for Power (high surface area)
- A Flexible Approach
  - Paste Applied Porous Electrodes
  - Solid Polymer Electrolytes
  - Low Temperature
  - Built for Scaling

Courtesy: Dan Steingart

Modeling

System Power Modeling

Output: Current vs. Time

1. Power TOSsim
   (Python, Harvard)
   - Estimates energy needed based on different TinyOS hardware for a given program
   - Sleep states not well modeled
2. Measurements in various states
3. Estimate with designed power consumption & anticipated duty cycle

Battery Charge Modeling

Output: State-of-charge vs. Time

1. Energy Density Balance

   1st order approximation based on known mAh/g, volume

   Poor accuracy as battery size decreaes
2. DualFoil (Berkeley)

   Comprehensive Fortran 1-D Solver
3. Empirical Models

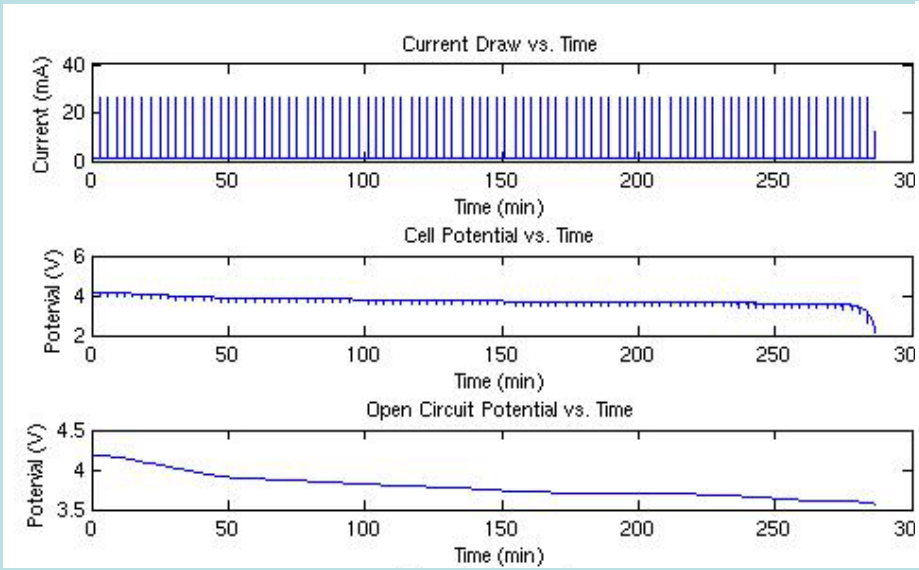
   Limited predictive ability (chemistry, form factor, etc)

   Limited physical significance

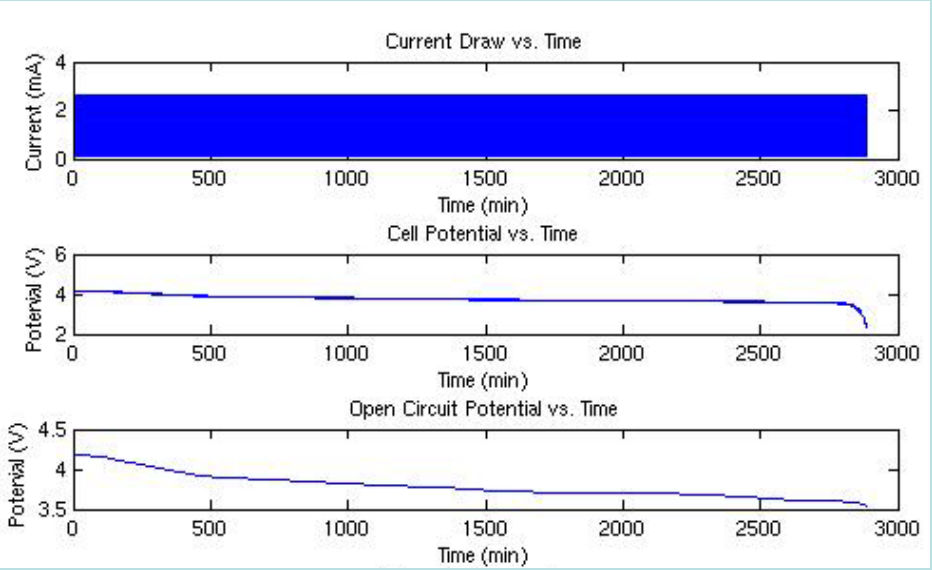
Battery Life Simulation

Simulation setup:
PowerTOSsim (Python) to DualFoil (Fortran) controlled via Matlab

LiCoO2 Li-Ion battery



Mica2



Custom Radio

But, how does the battery state influence network conditions, circuit performance?

Courtesy: Dan Steingart

Part I Summary:

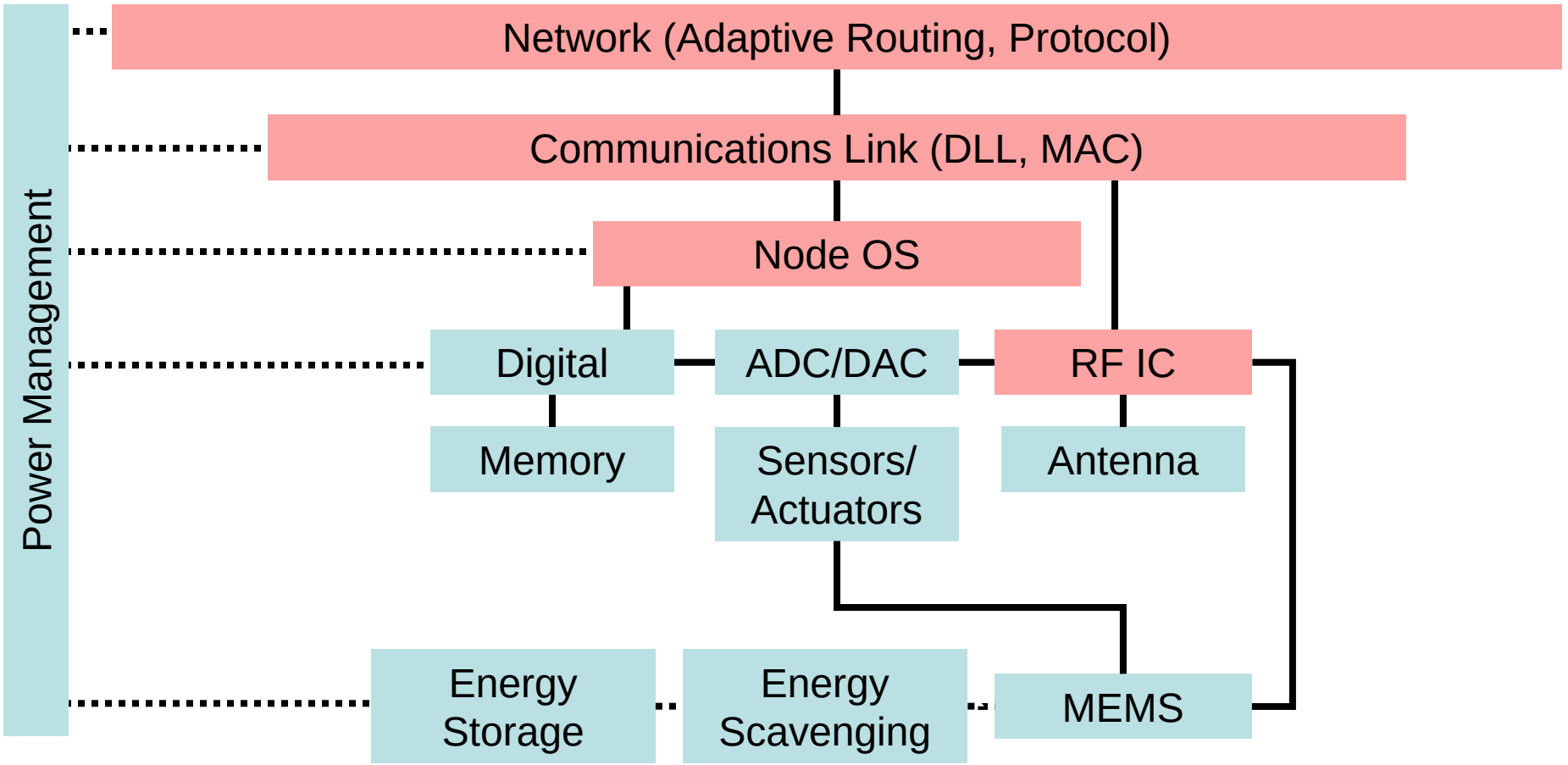
No tie-in between electro-mechanical powertrain and power management circuitry.

Required:

1. Model the interaction between the battery state-of-charge and electronics
   - Can we implement adaptive power algorithms sensitive to battery potential output?
   - Simulation of electronic performance over network conditions, environmental conditions, and battery charge

2. Parameterized battery models

Part II: Communications Link



- Develop efficient network schemes suitable to ad-hoc networks
- Huge gains in efficiency can occur at higher network layers

Communication Link: Protocol Stack

Step 1: Design, modeling and analysis

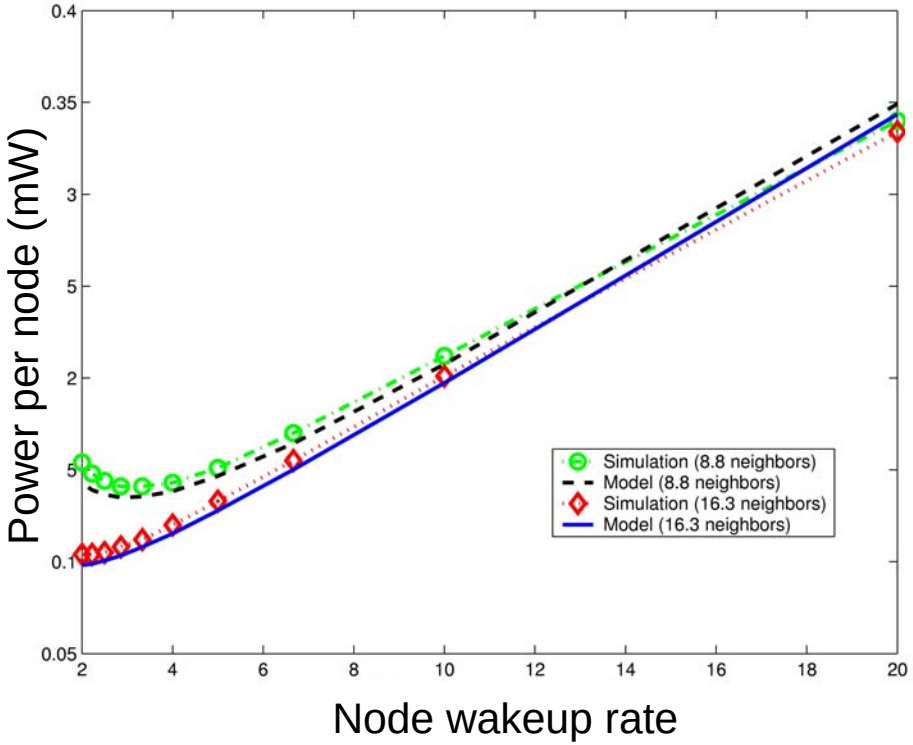
Step 2: Simulation (Omnet++)

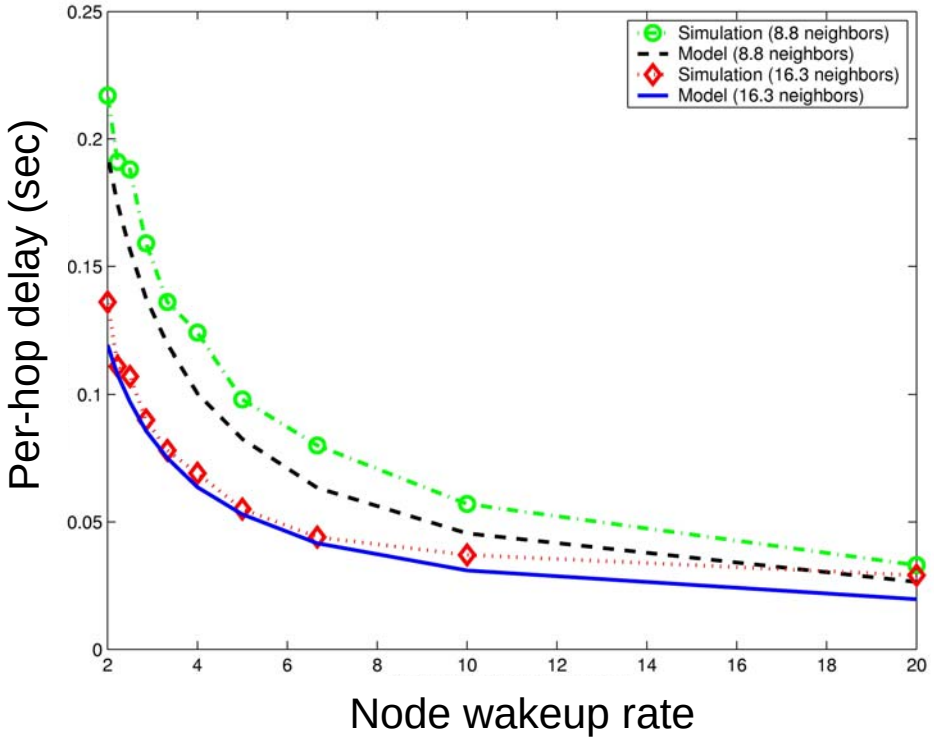
Step 3: Implementation (Berkeley motes)

The design included opportunistic routing, pseudo-asynchronous MAC and adaptive duty cycling.

Courtesy: R. Shah

Opportunistic Routing: Simulation results

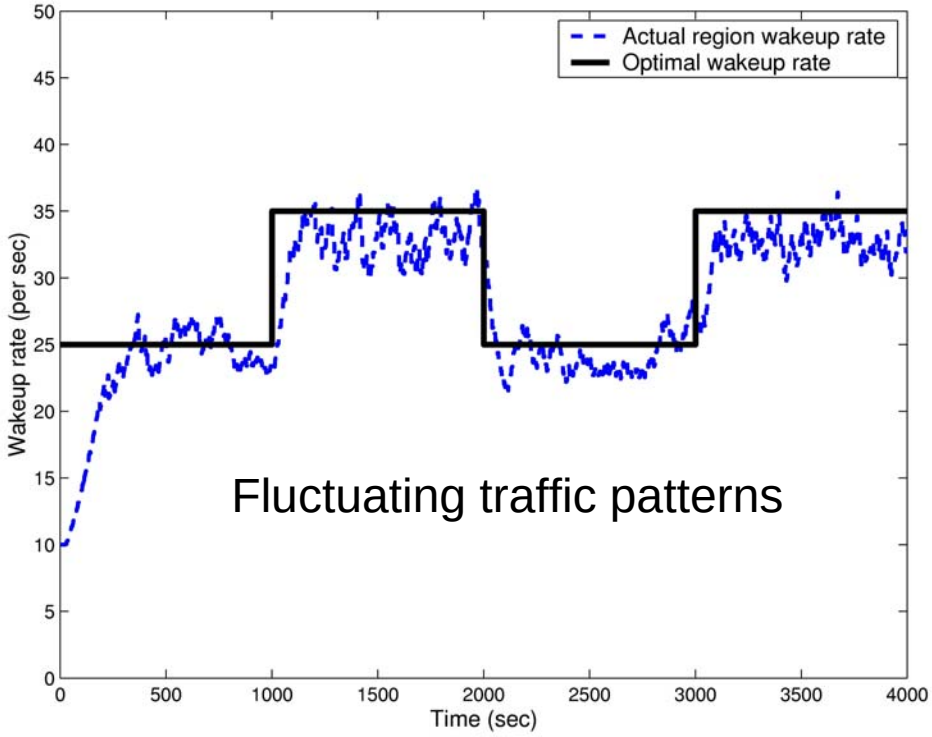




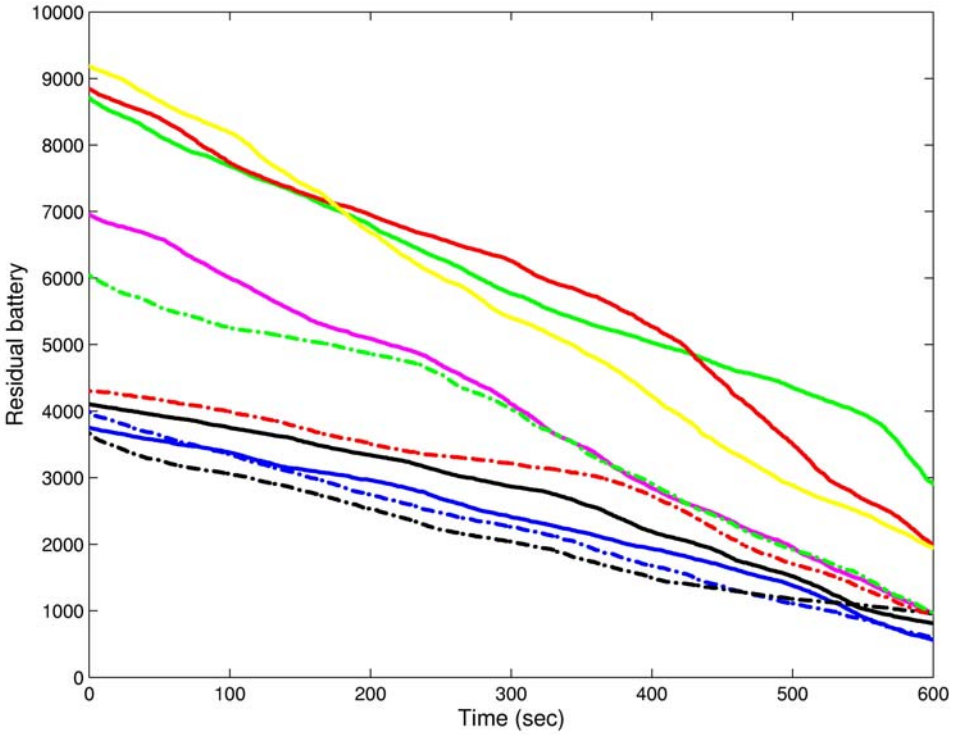
- The entire protocol stack was simulated in Omnet++
- To enable large size network simulations, only packet level errors were simulated

Courtesy: R. Shah

Adaptive Wakeup Rate Simulation



Optimal vs. Simulated wakeup rate

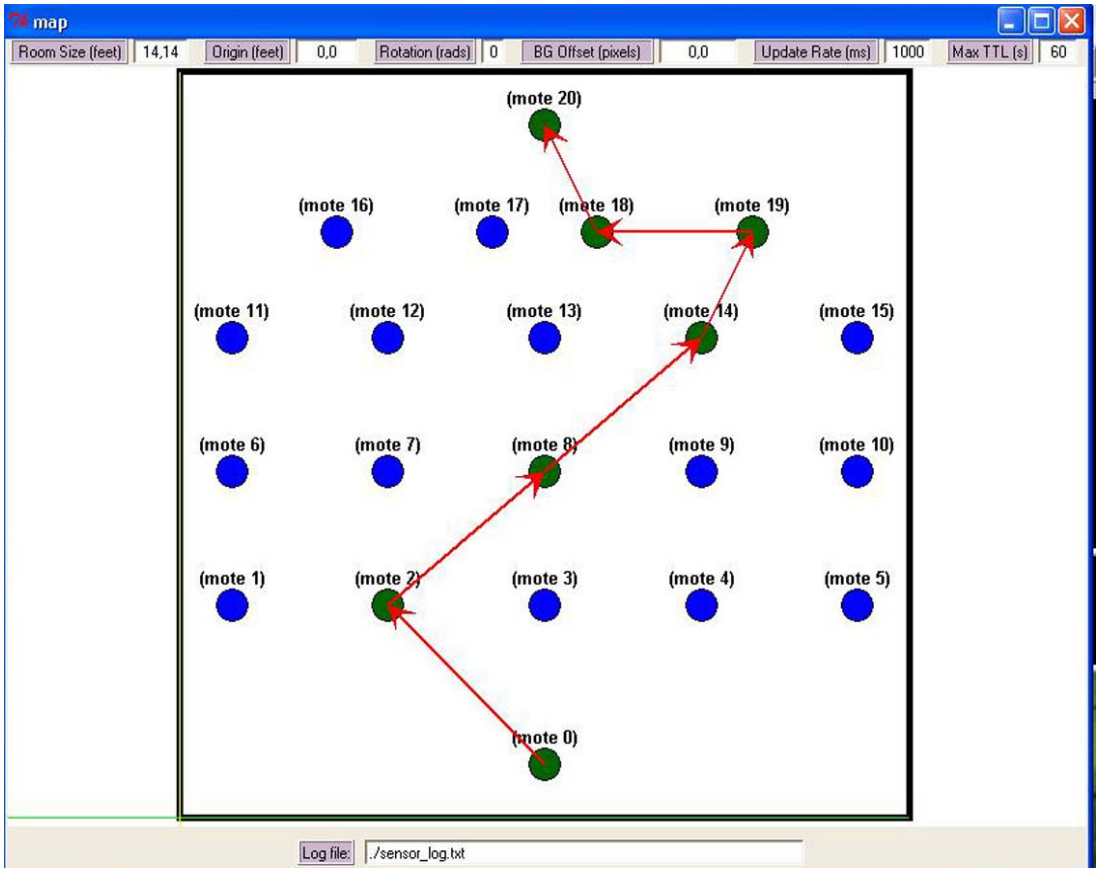


Battery Energy

Number of nodes in forwarding region = 10
Traffic rate is changed periodically

Courtesy: R. Shah

Simulation Setup



KEY:

= Sending / Receiving Motes

= Sensing / Sleeping Motes

RTS Transmit Time	352 uSec (11 bytes)
CTS Transmit Time	288 uSec (9 bytes)
Data Transmit Time	896 uSec (28 bytes)
ACK Transmit Time	288 uSec (9 bytes)
CTS Waiting Time	10 mSec
Data Waiting Time	10 mSec
ACK Waiting Time	10 mSec
RAM Usage	0.712 KB
ROM Usage	16.952 KB
Packet Generation Rate	0.2/Sec

Transmission times, Waiting times and Memory Usage

Courtesy: R. Shah

Part II Summary:

Protocol/MAC designed via analysis/simulation

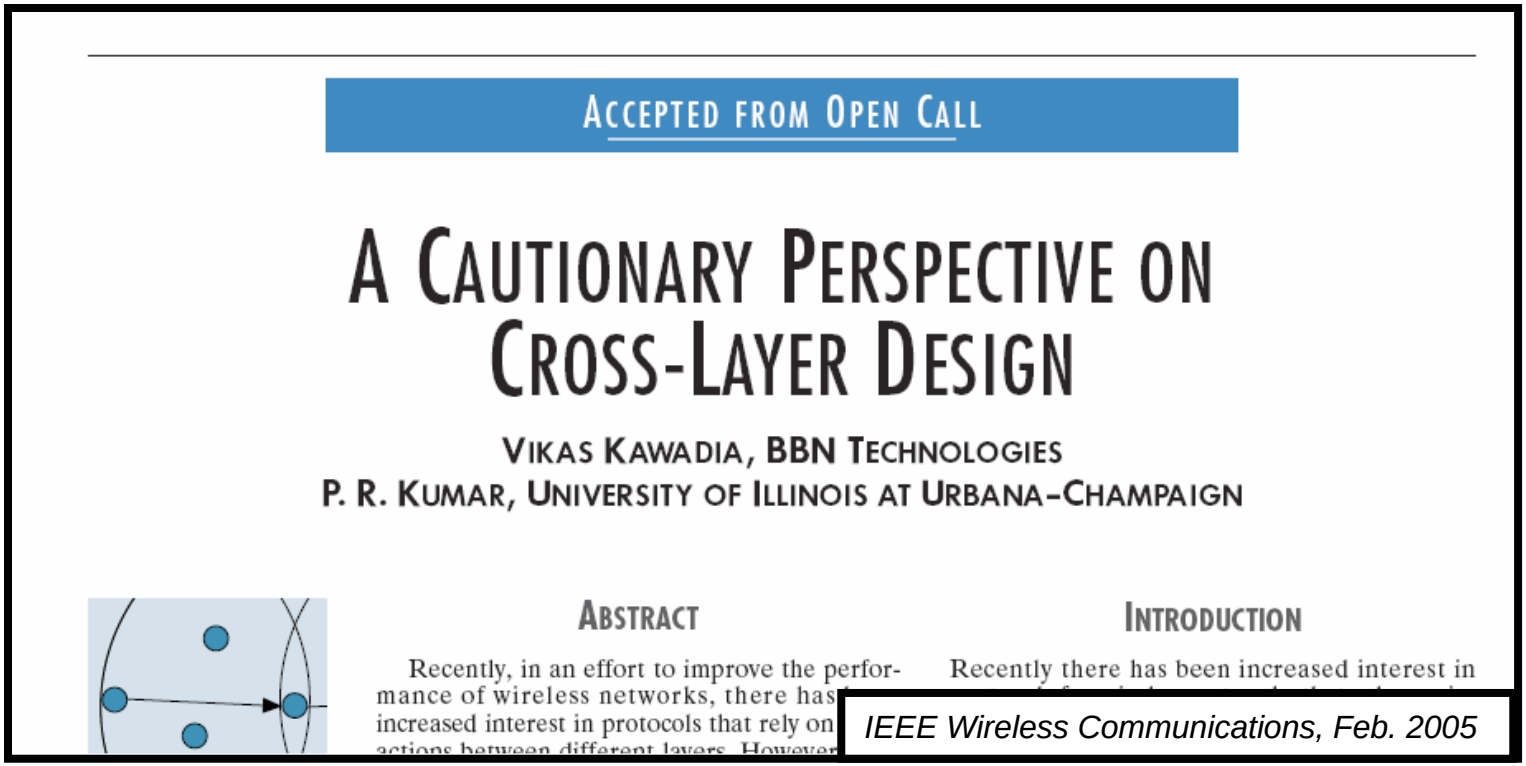
No connection to physical layer models, so joint optimization not possible

How much power is used during network discovery, etc?

How does changing the modulation scheme or transmitted power effect overall network performance?

How does the adaptive wakeup rate perform with a physical battery model?

An important point…



ACCEPTED FROM OPEN CALL

A CAUTIONARY PERSPECTIVE ON CROSS-LAYER DESIGN

VIKAS KAWADIA, BBN TECHNOLOGIES
P. R. KUMAR, UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

ABSTRACT

Recently, in an effort to improve the performance of wireless networks, there has increased interest in protocols that rely on actions between different layers. However

INTRODUCTION

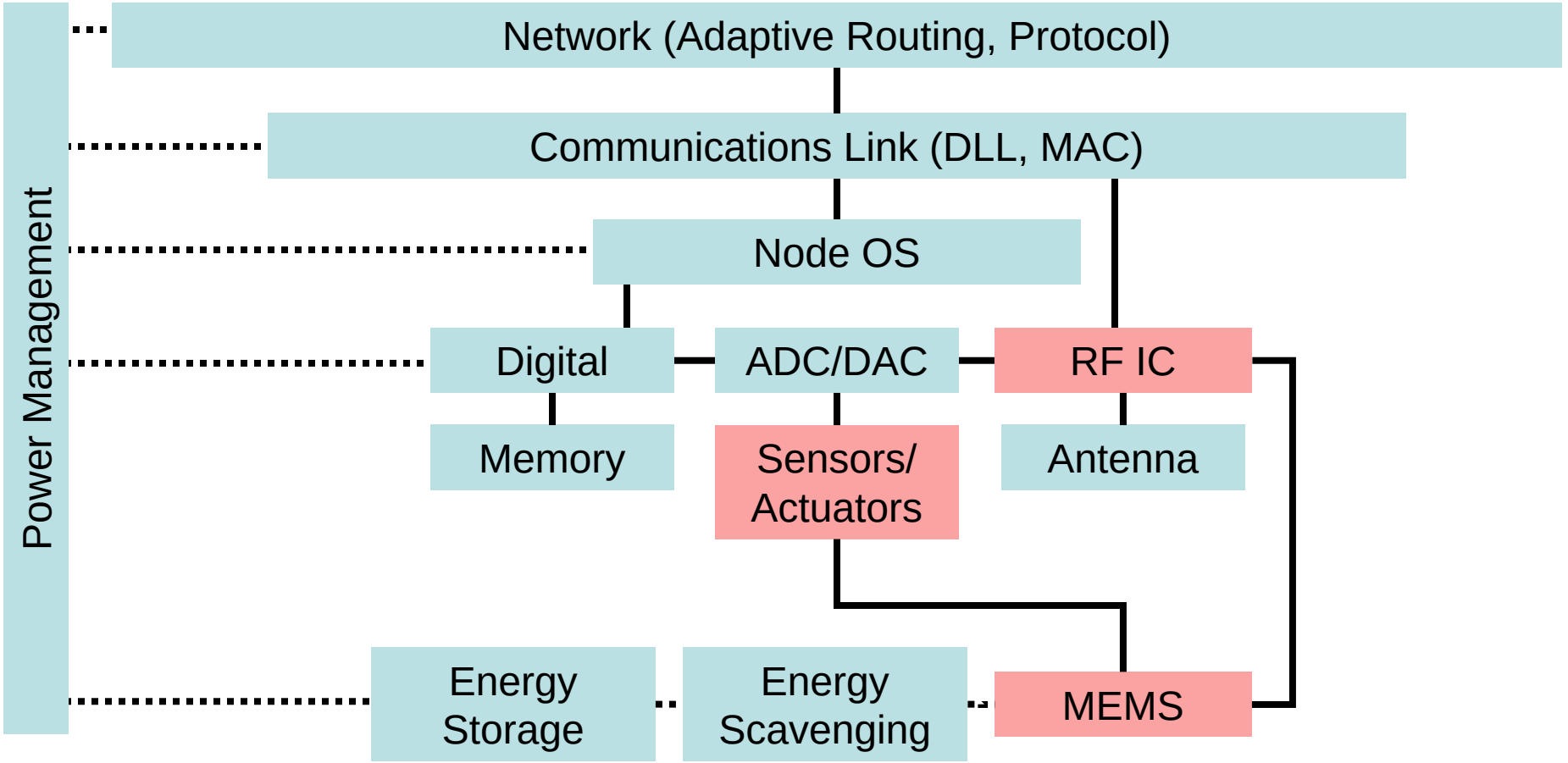
Recently there has been increased interest in

IEEE Wireless Communications, Feb. 2005

Does cross-layer design (rate-adaptive MACs, etc) make systems susceptible to the “Law of Unintended Consequences”?

By increasing the scope of the models, we are better able to predict complicated interactions between layers.

Part III: MEMS/Circuitry Co-design



- MEMS technologies can increase performance and greatly reduce size & power consumption of sensor networks

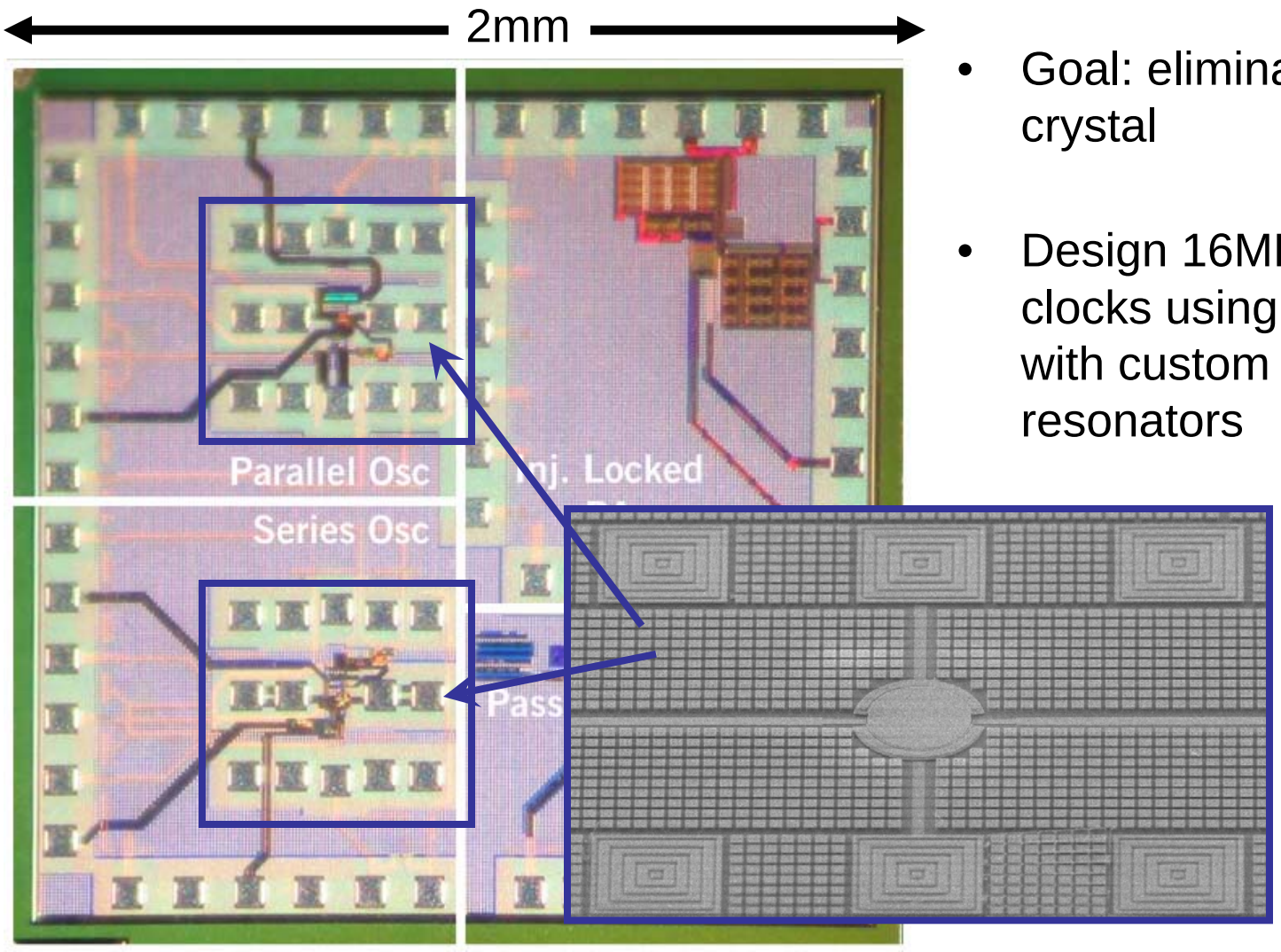
CMOS/MEMS systems

Micro Electromechanical Systems (MEMS) allow previously impossible implementations, including

1. Small sensing (Analog Devices ADXL Accelerometer)
2. Low power wireless implementations
3. Miniature reference clock generation

Two examples: reference clock design and low power transceiver design

MEMS-Based Reference Clocks



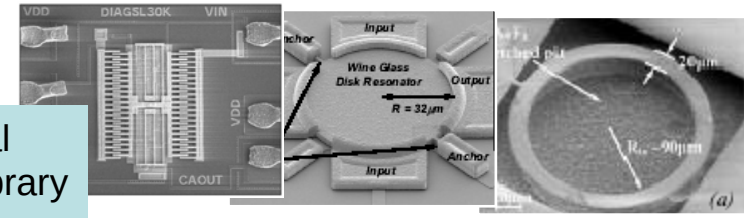
- Goal: eliminate bulky quartz crystal
- Design 16MHz reference clocks using 0.13µm CMOS with custom SiGe MEMS resonators

R. Howe
E. Quévy
N. Pletcher
J. Rabaey
B. Otis

MEMS Design: Structure Choice

MEMS resonator = Mechanical Structure + Transducer == RLC equivalent network

*At the system level, we start from the requested network to co-design **structure** first, then **transducer***



Courtesy:
Dr. E. Quevy

System specifications
- Center frequency
- Input/Output impedance
- Insertion loss
- Topology

Mechanical Structures Library
-Tuning Fork
- Disk
- Square

Transducer Efficiency
-Electrostatic
- Piezoelectric

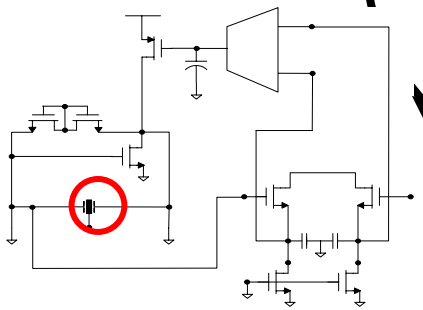
?

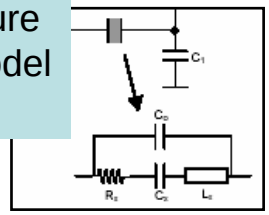
Structure Approximate Dimensions

Matlab Fast Analytical Model (1D)

$$f_{1st\,mode} = \frac{1}{2\pi}\cdot\sqrt{\frac{199.\frac{I_M(T).E(T)}{L(T)^3} + 4.89.\frac{F(T)}{L(T)}}{0.389.\rho_{SiGe}.W.L.h}}$$

Specification on Simple structure equivalent model (BVQ)





Spec-based Structure choice (Analytical) → Finite-Element Modeling (ANSYS) → Spice/Behavioral Modeling (Cadence) → Structure Layout (Cadence Virtuoso)

MEMS Design: FEM Modeling/Optimization

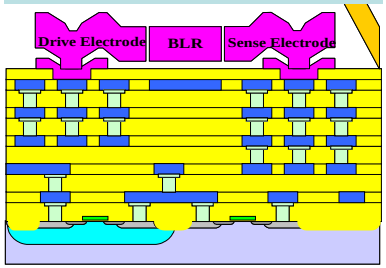
Courtesy:
Dr. E. Quevy

Structure Dimensions

Fabrication Process in place

Initial Layout

3D Synthesis



$$[M]\left[\ddot{X}\right]+[K][X]=0$$

$$[M]\left[\ddot{X}\right]+[C]\left[\dot{X}\right]+[K]\left[X\right]=[F]\cos(\omega t)$$

Geometrical Model (3D)

Modal Analysis

Harmonic Analysis

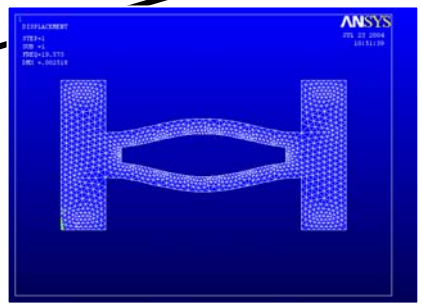
Parametric Analysis

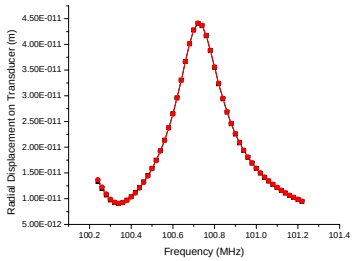
f_O

$[K_r, M_r]$ @ f_O

f_{res}
$[K_r, M_r]$
Q
…
=
func
(dim, E, T°, …)

Material / Topology Characteristics
- Thicknesses
-Residual stress
-Temperature coefficients
-Design Rules





Spec-based Structure choice (Analytical)

Finite-Element Modeling (ANSYS)

Spice/Behavioral Modeling (Cadence)

Structure Layout (Cadence Virtuoso)

MEMS Design: Electrical Modeling

f_{res}

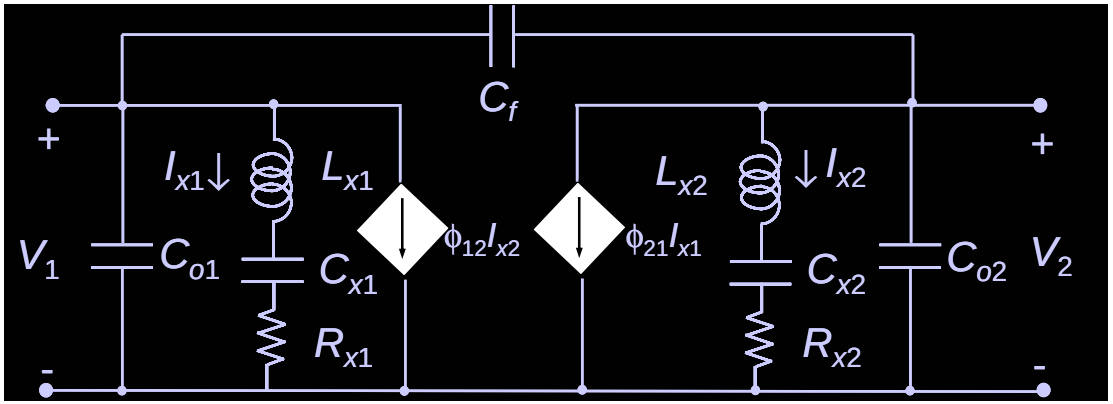
K_r

M_r

Q

Transducer Structure
(selected at step1)

Equivalent N-port spice/AHDL model



Includes : ***- Temperature***
- Noise Sources
- Bias

Courtesy:
Dr. E. Quevy

System Level Corner Simulation

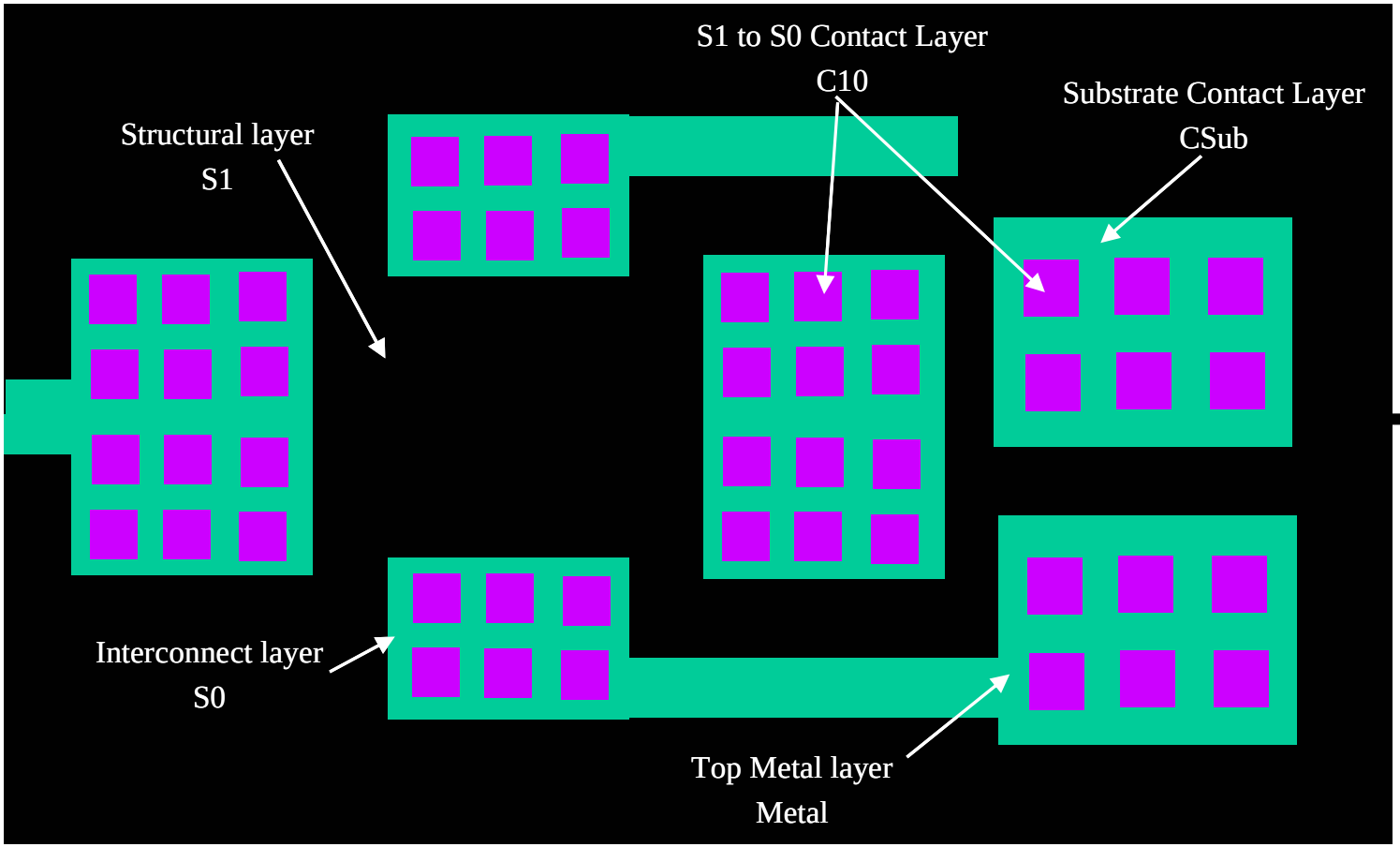
Note: This part of the model may need to be fitted with experimental parameter extraction results on stand-alone structures to input accurate process variation in system level simulation

Spec-based Structure choice (Analytical) → Finite-Element Modeling (ANSYS) → Spice/Behavioral Modeling (Cadence) → Structure Layout (Cadence Virtuoso)

MEMS Design: Layout, DRC, extract

Ex: Layout of a 24MHz Tuning Fork

Courtesy:
Dr. E. Quevy



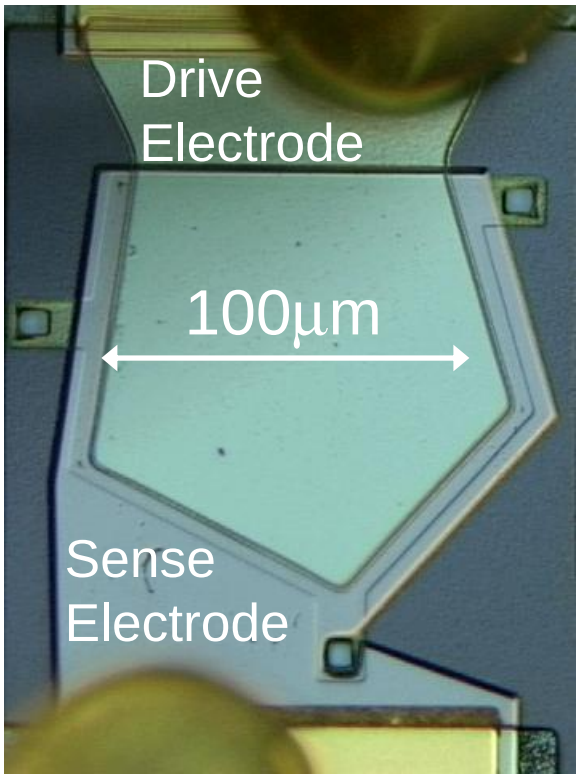
Parasitic Extraction And Simulation

Spec-based Structure choice (Analytical) → Finite-Element Modeling (ANSYS) → Spice/Behavioral Modeling (Cadence) → Structure Layout (Cadence Virtuoso)

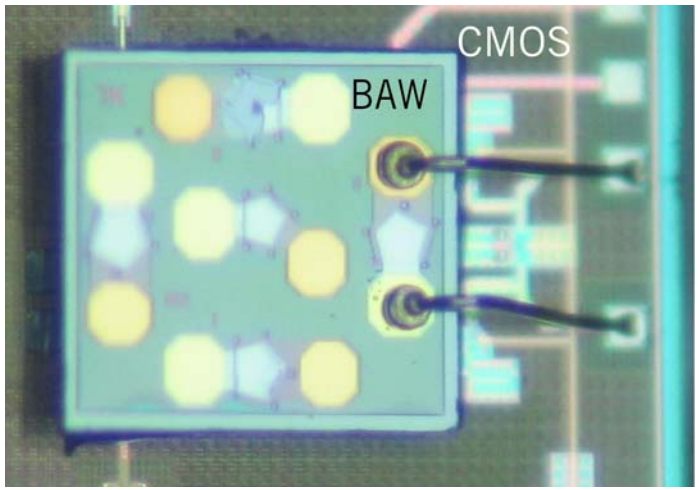
RF MEMS: path to ultra-small radios

Properties:

- High quality-factor (*Q ~ 1000)*
- Enables new transmit and receive architectures
- Defined lithographically, batch fab: can co-design with active devices



Agilent AlN FBAR

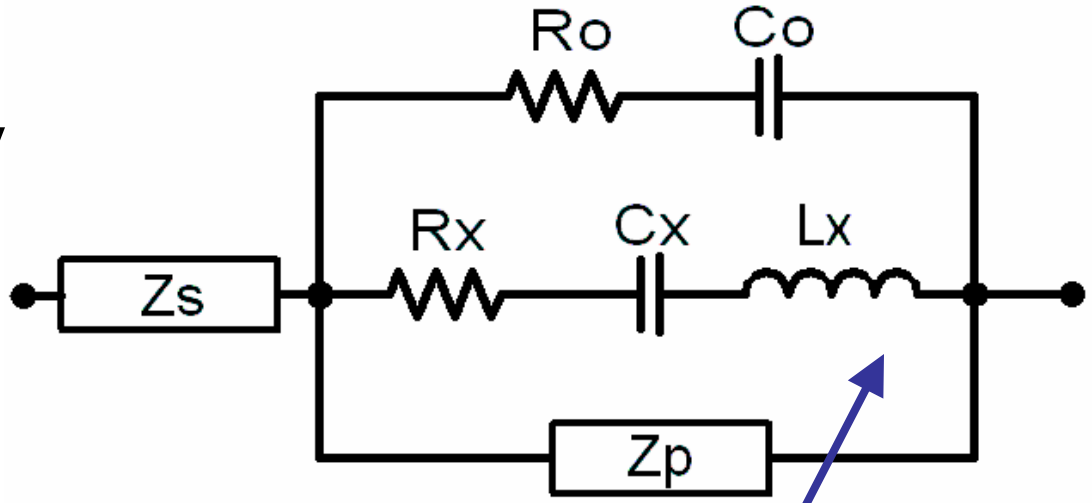


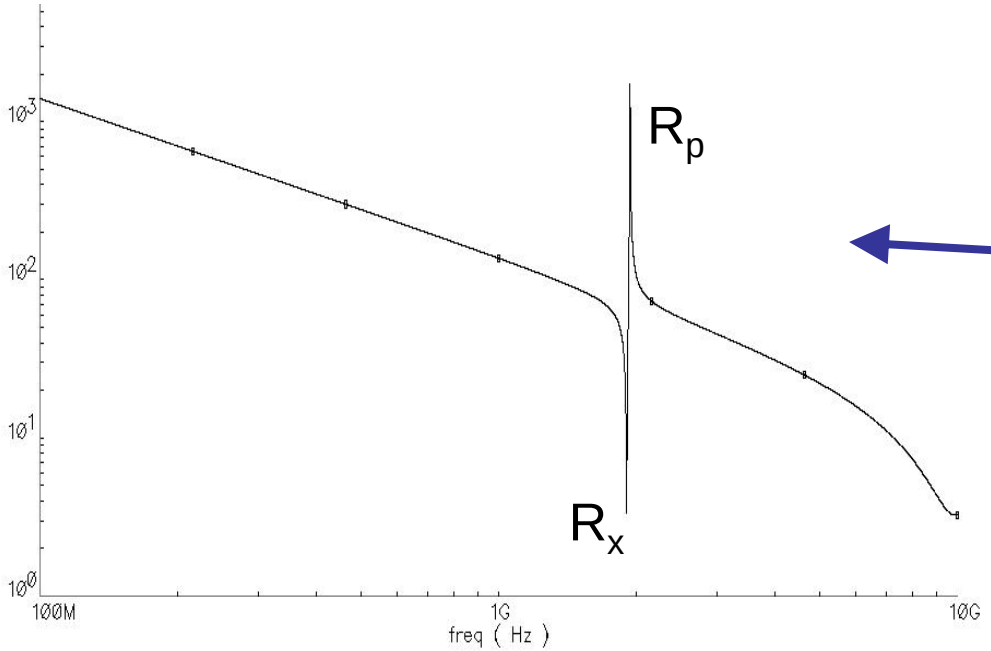
Differential ISM BAW Oscillator (2.4GHz)

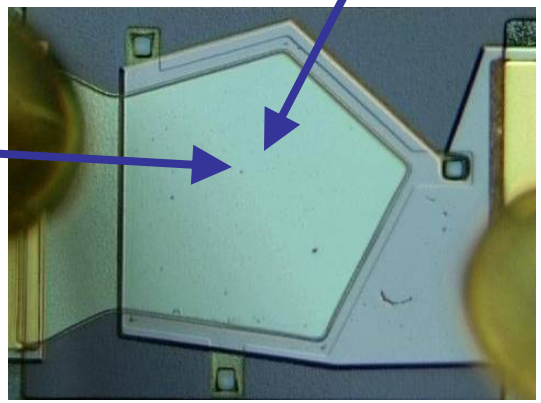
- 115μA
- Max Swing: 0.9Vp-p
- Supply Pushing: 0.4MHz/V
- -120dBc/Hz @ 100kHz

BAW/CMOS Co-Design

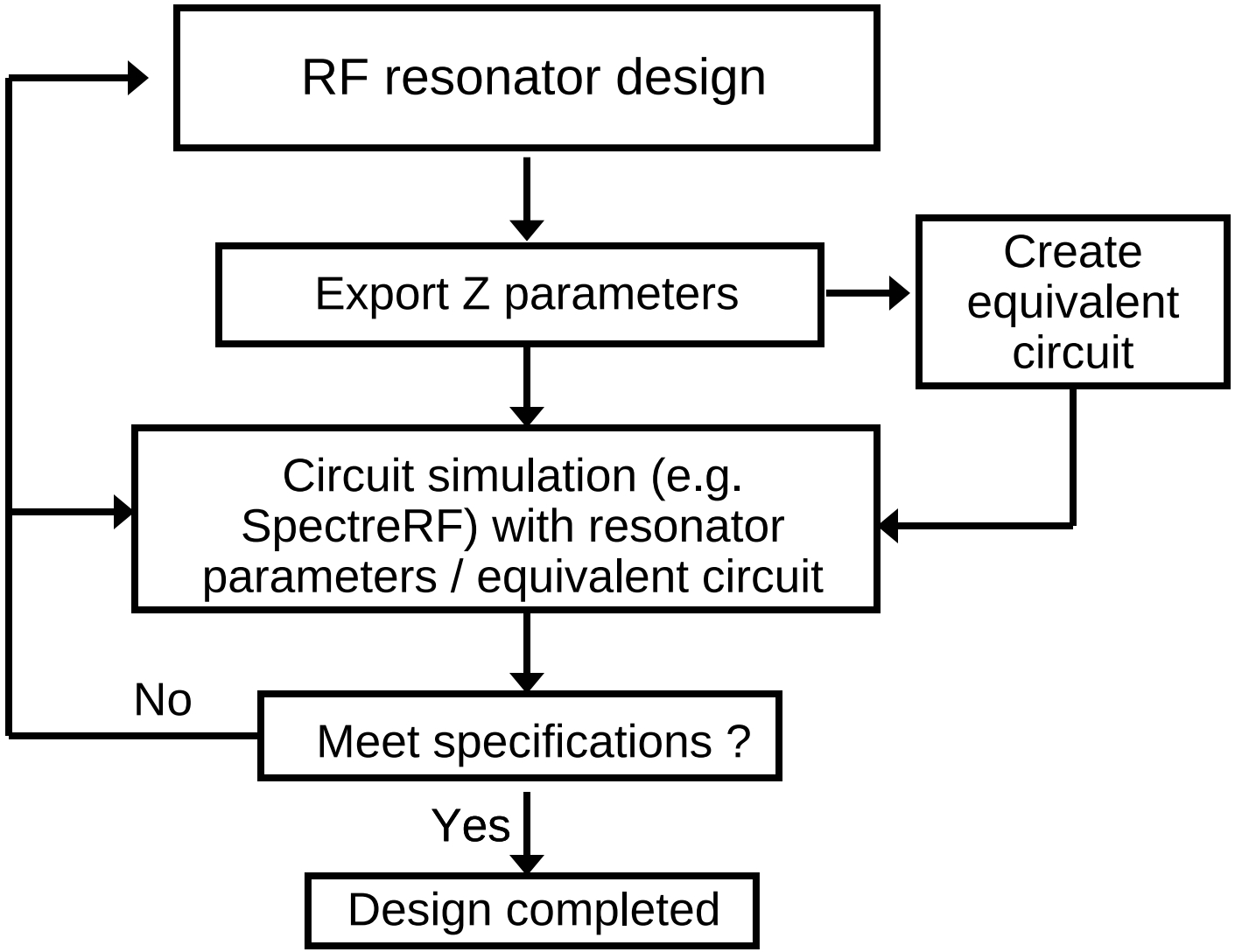
- Can control resonator parameters lithographically
- Co-design MEMS/circuit to achieve optimal performance



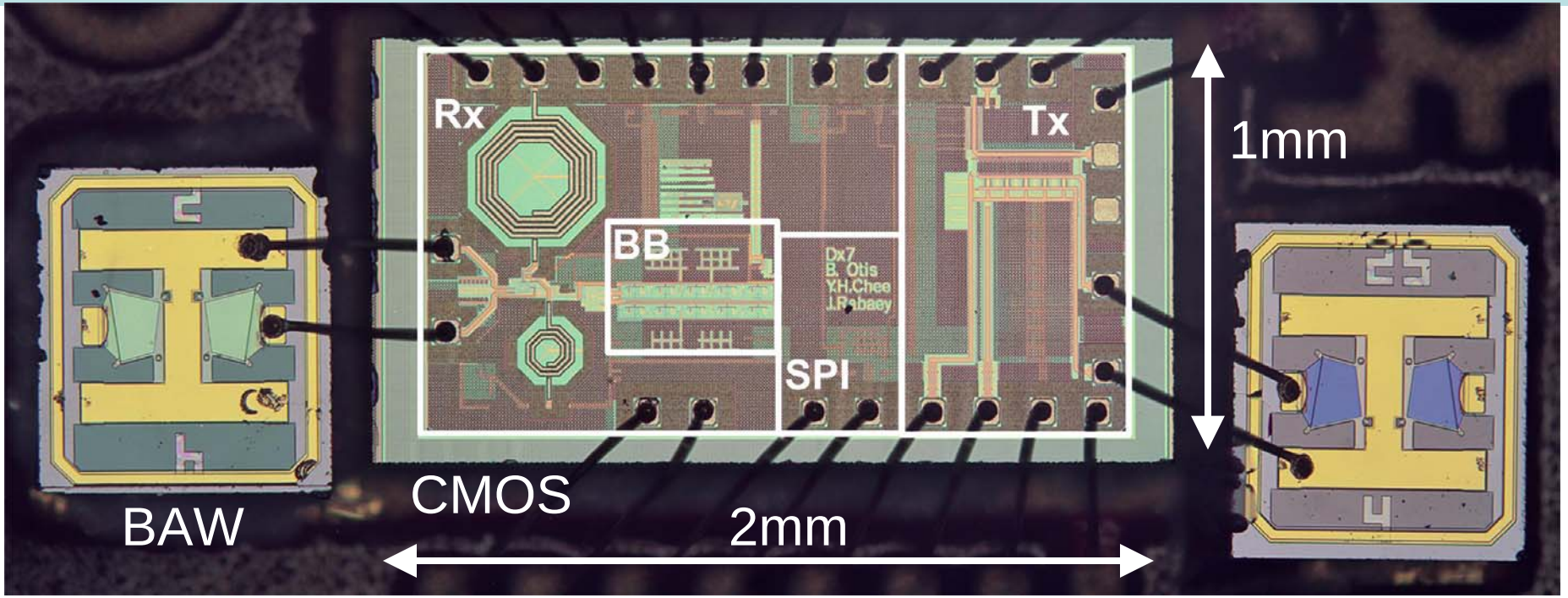




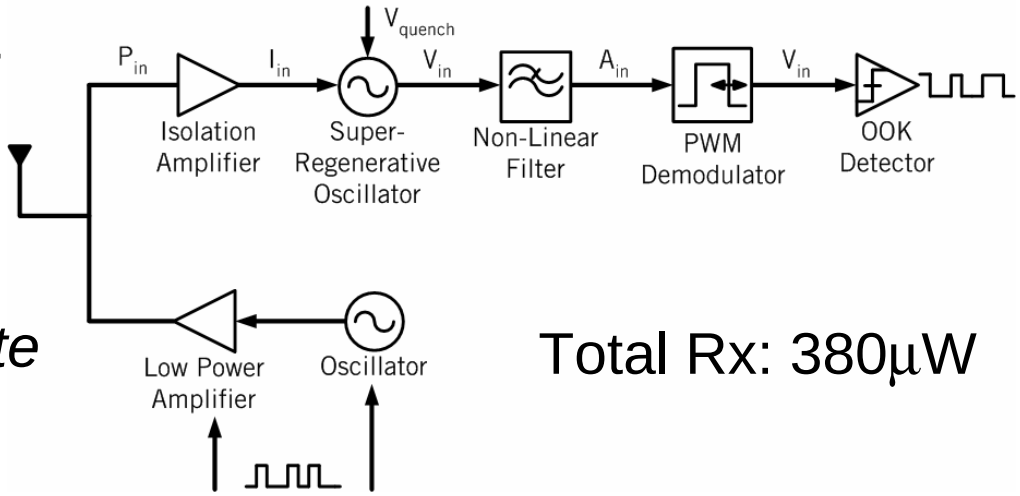
Design Methodology



Sub-mW 2GHz Transceiver



- Super-regenerative transceiver
- Simulation difficult due to high Q, long time constants
- *Simulate circuit blocks, calculate system performance*

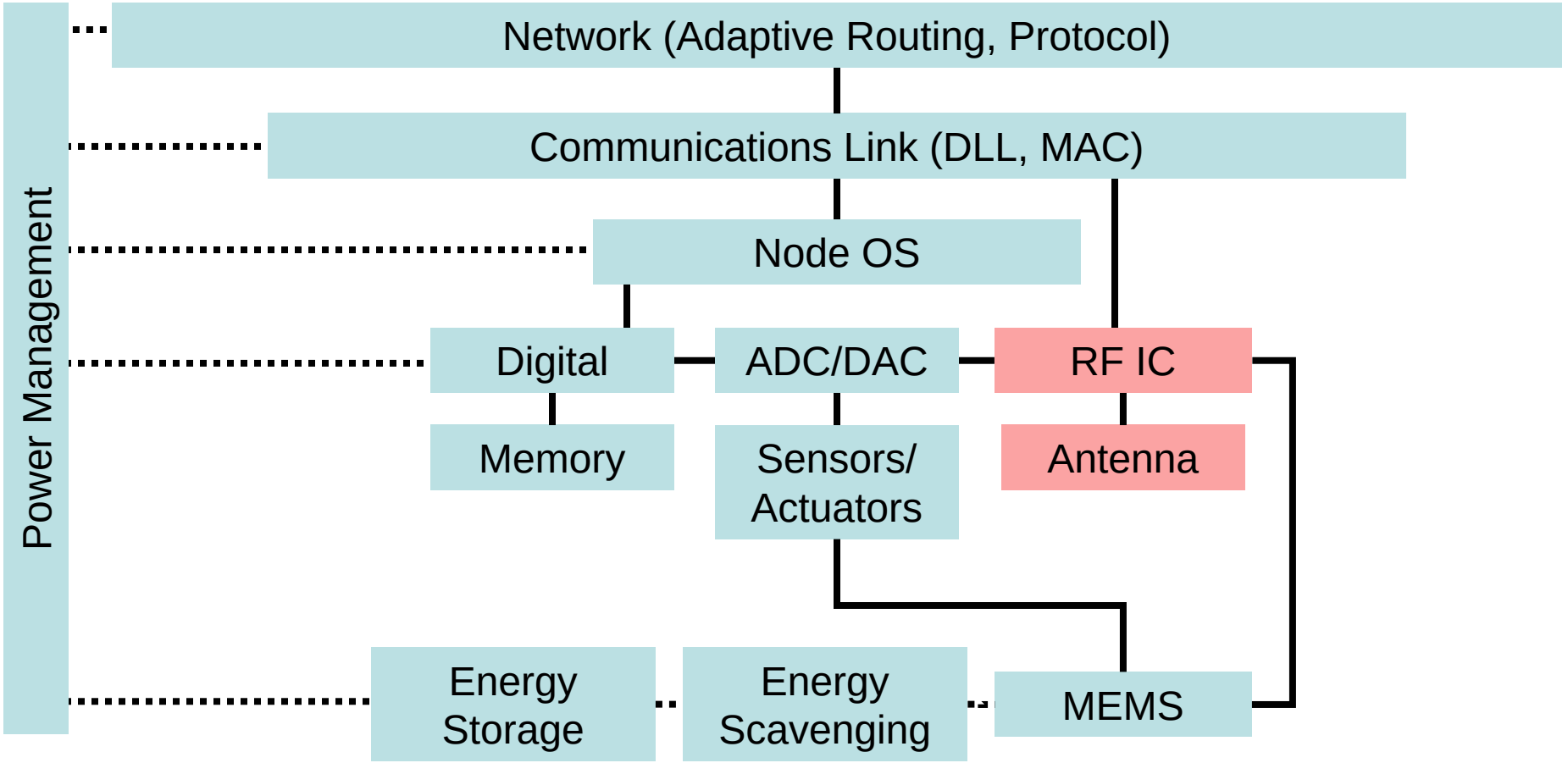


Total Rx: 380μW

Part III Summary:

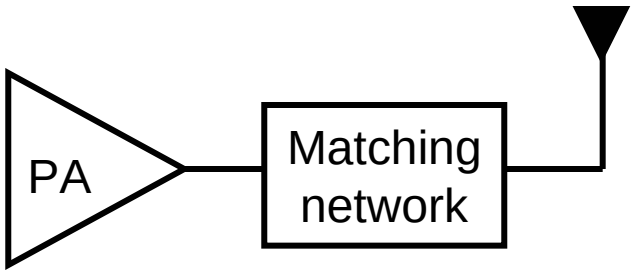
- Silicon MEMS technology will become more pervasive in electronic systems
- Currently, no parametric SPICE models for these components
- RF MEMS devices provide very high f_{osc}* Q products:
  - Allows reduced transceiver power consumption
  - Greatly increases simulation difficulty
- Non-linear super-regenerative receiver difficult to simulate
- Simulating entire receive chain over an entire packet training sequence very time/CPU intensive

Part IV: EM/Circuit Co-design

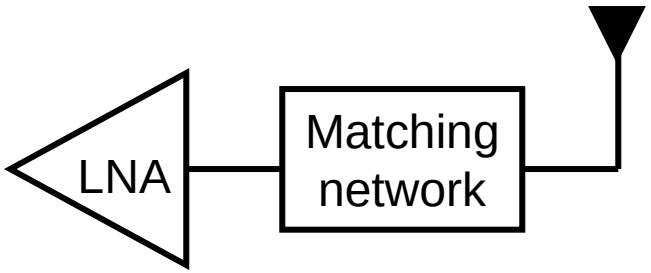


- Eliminate traditional 50Ω interface to increase performance

Antenna-Circuit Co-design



Transmitter

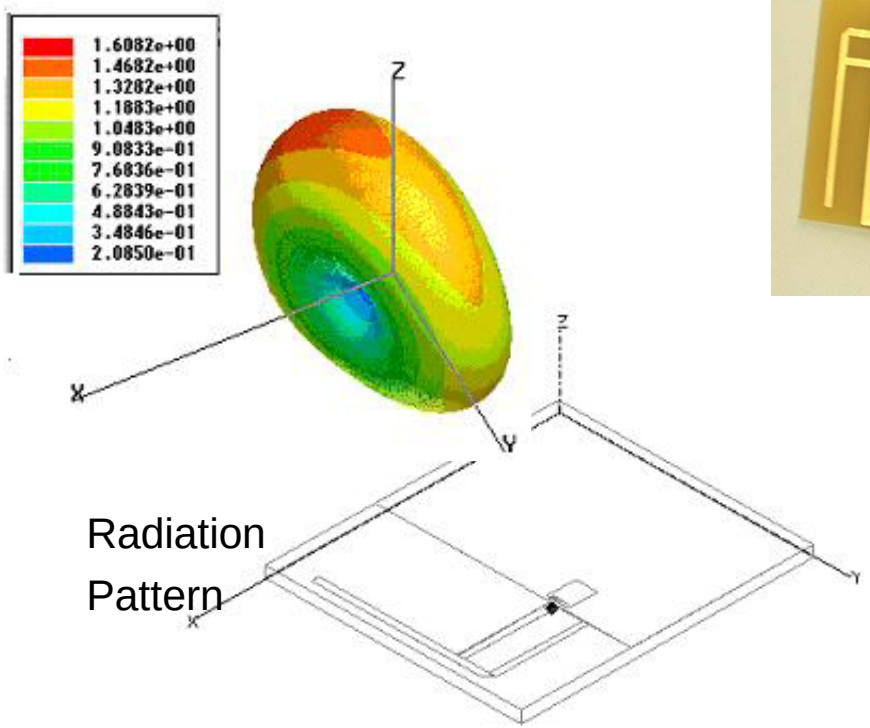


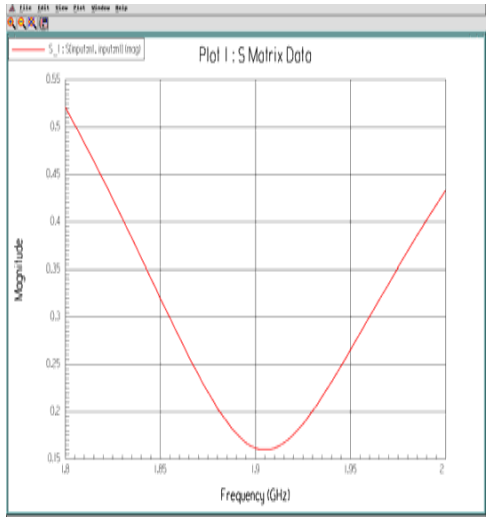
Receiver

- Traditional design assumes 50Ω resistive load.
- Possible to design the antenna together with front-end circuits to eliminate matching networks.
- Antenna design requires solving fields equations but circuit simulator relies on circuit theory.
- No CAD tools support antenna-circuit co-design.

Courtesy: Y. Chee

High Frequency Structure Simulator (HFSS)

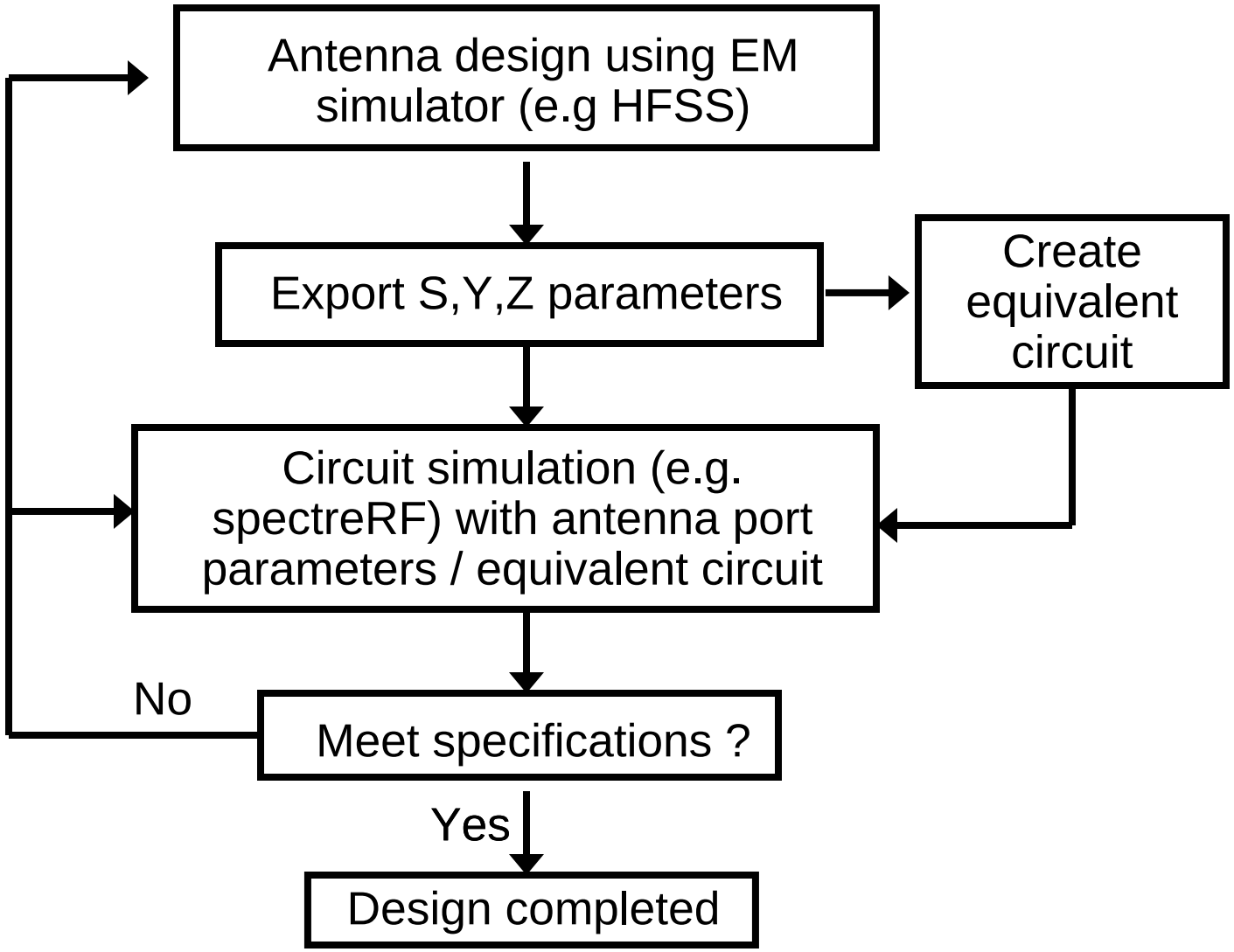




- HFSS is a full 3-D EM simulator.
- Use to simulate antenna input impedance, radiation pattern and efficiency.
- Able to export S, Y or Z port parameters.

Courtesy: Y. Chee

Design Methodology



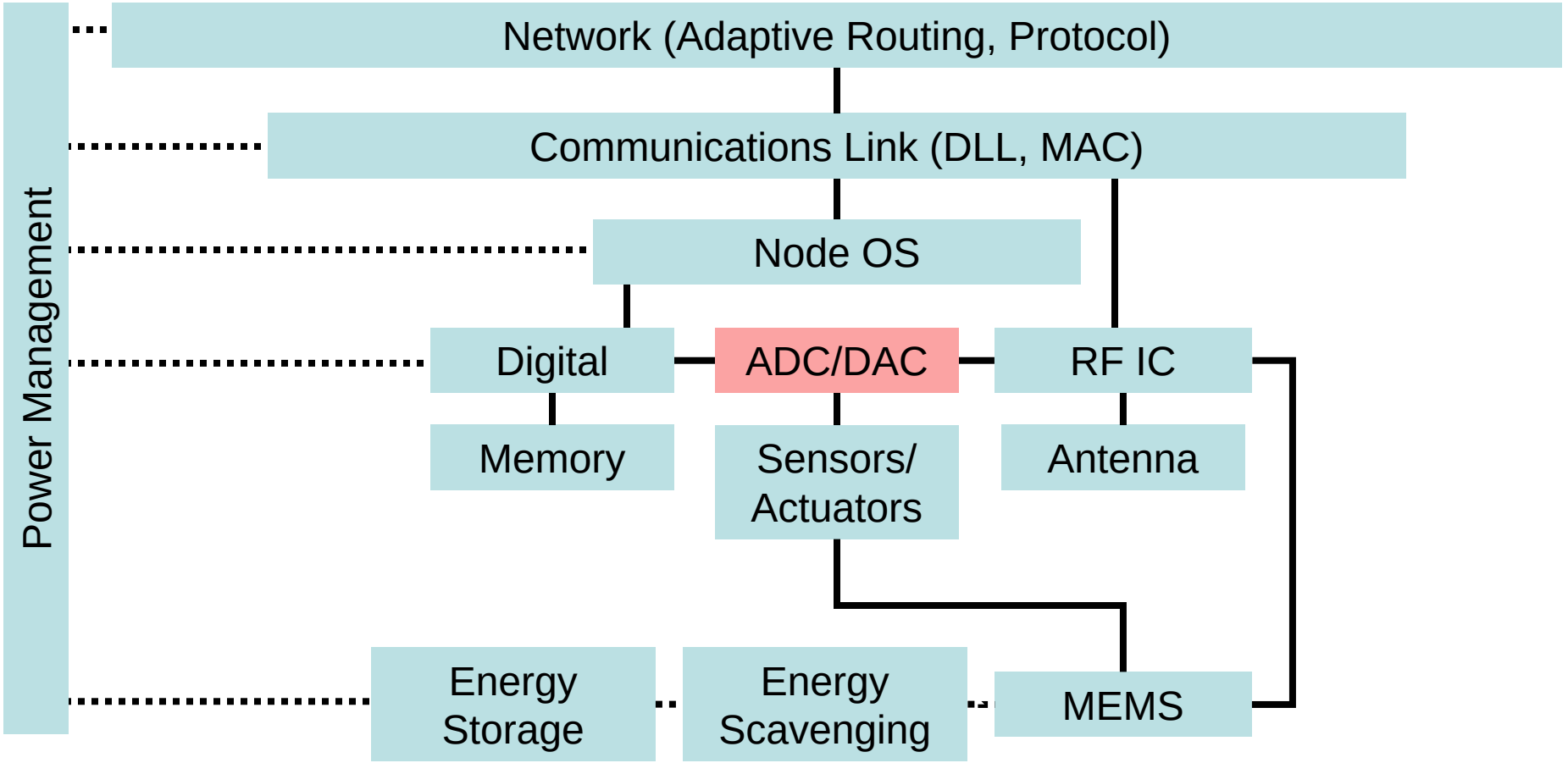
Courtesy: Y. Chee

Part IV Summary:

Typically, there is a clean 50Ω handoff between RF circuit designers and microwave antenna designers

The co-design of electromagnetic transducers and integrated circuits can improve the efficiency of RF links

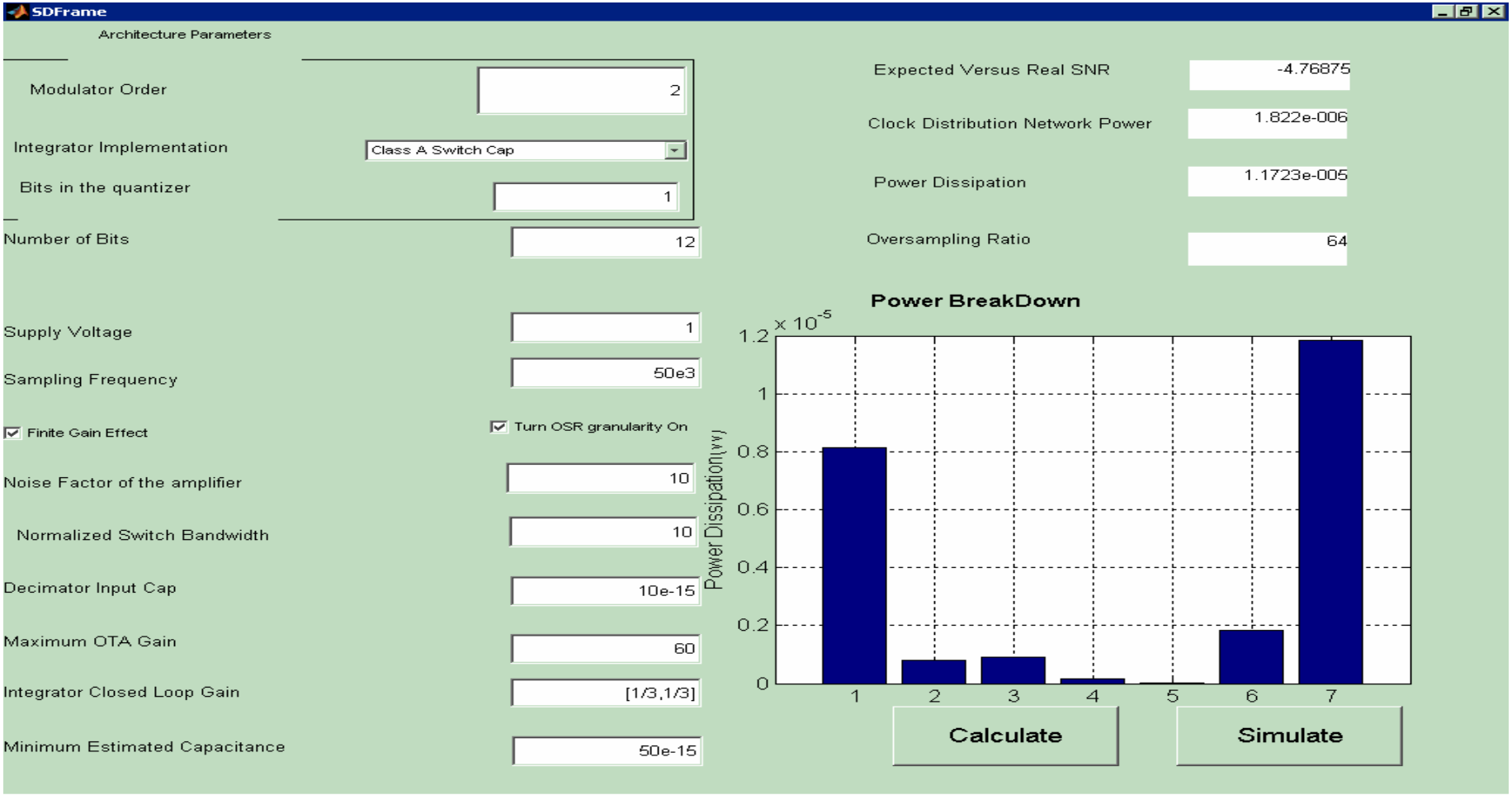
Part V: Low Power A/D Converter



- A/D forms the interface between physical world and abstract algorithms
- Specifications: 75dB DR, 50KS/s,15μW $\Sigma\Delta$ ADC

Σ–Δ ADC design flow: step 1

High-Level, equation-based system exploration to get fast tradeoff estimates (heuristic)



Courtesy: S. Gambini

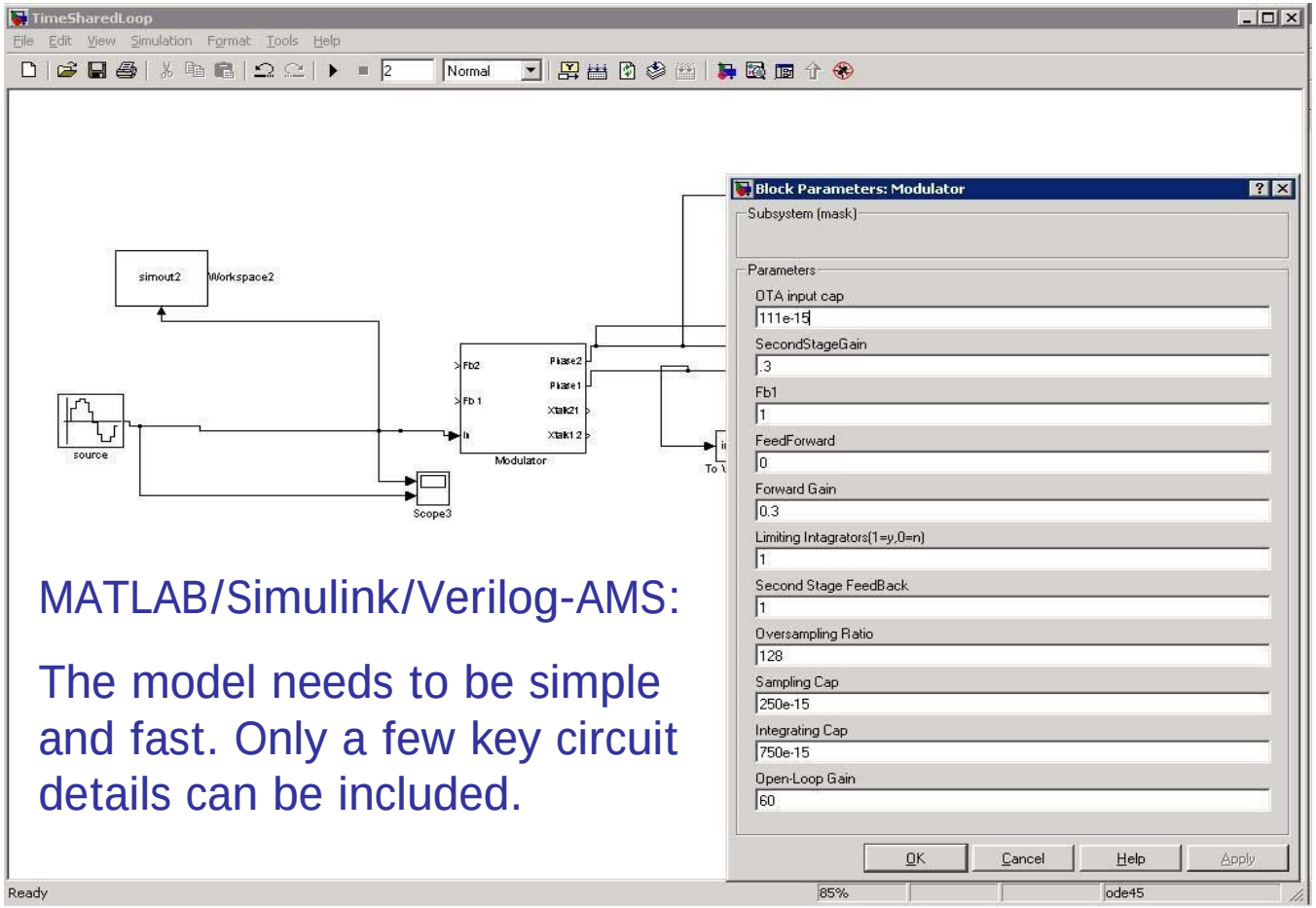
Σ–Δ ADC design flow: step 2

Detailed behavioral simulation

Example:

Second-Order loop

Model: Finite OTA Gain ,finite output swing, non-linearity, noise, incomplete settling.

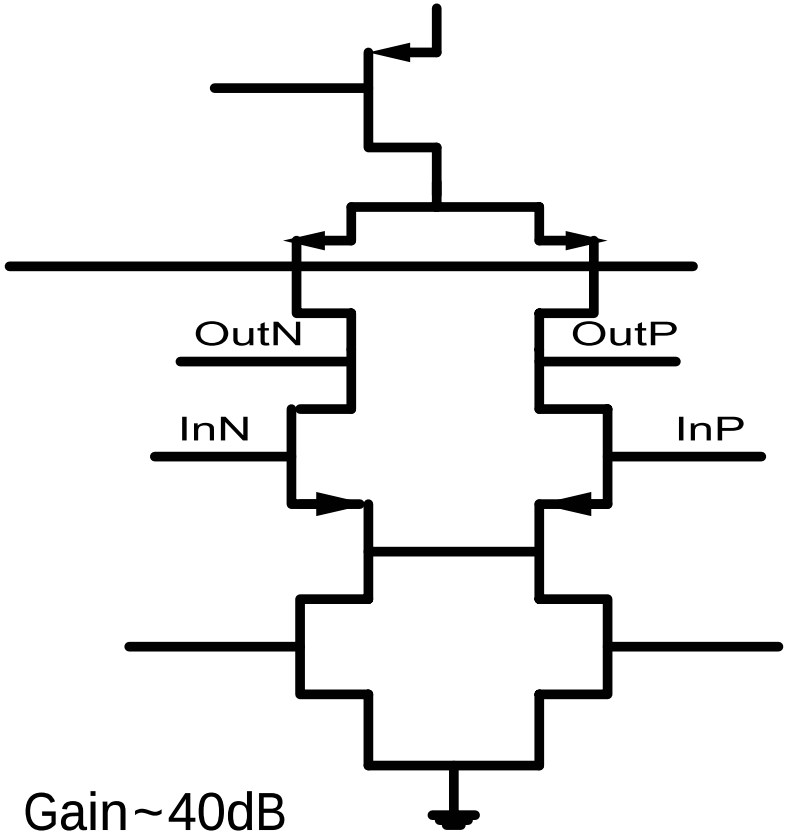


MATLAB/Simulink/Verilog-AMS:

The model needs to be simple and fast. Only a few key circuit details can be included.

Courtesy: S. Gambini

Σ–Δ ADC design flow: step 3



Gain~40dB

GBW/Fs~10

C_{in}~150fF

F_{knee}~10kHz

Design the building blocks

Use SPECTRE/SPICE to verify that block key performances match what assumed in the system simulations.

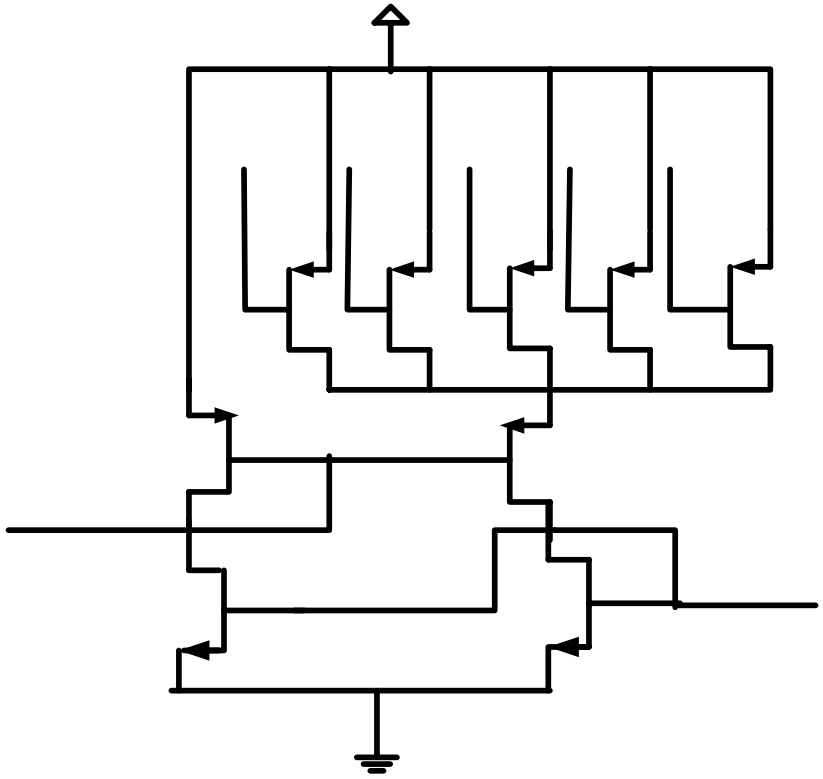
Back-Annotate and iterate

Note: ”Reachability Problem” or how do we know at the previous level what we can do now? No rigorous way-relies on designer skill/understanding of the circuit/system behavior

Courtesy: S. Gambini

Σ–Δ ADC design flow: step 3

- Digital Programmability



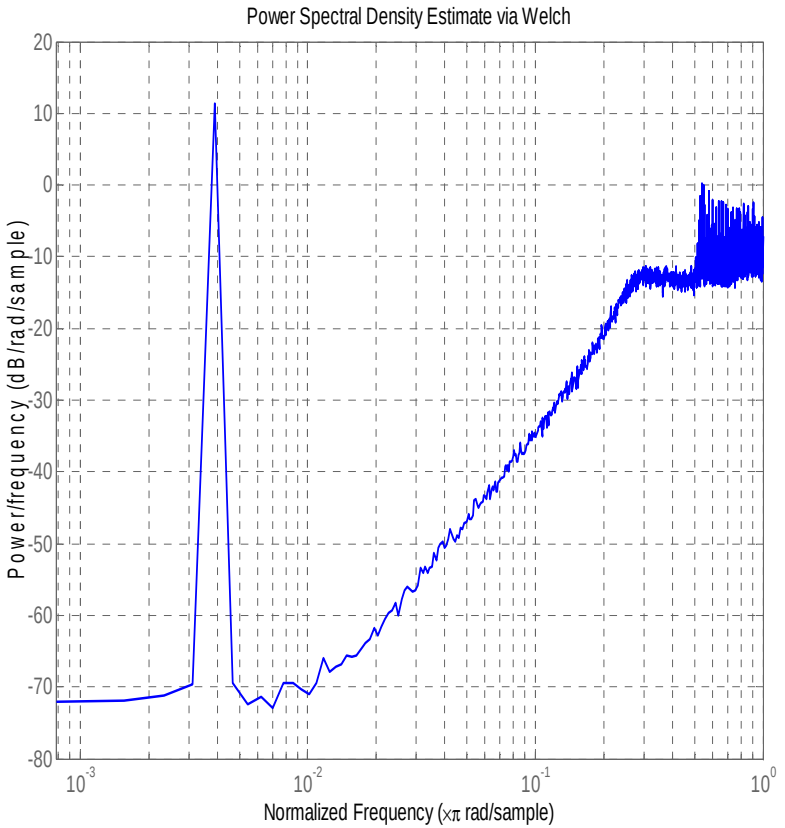
Limit overdesign by adding on-chip programmability

Example: Bias tuning

5-bit tuning range allows compensation for process variation and operation at variable sampling frequency and dynamic range

Courtesy: S. Gambini

Simulated Performance (Simulink)



Signal Bandwidth	50Khz
Oversampling Ratio	128
Dynamic Range	75dB
Power Consumption	15µW
FOM (4KT*DR*Fs/Pd)	700e-6

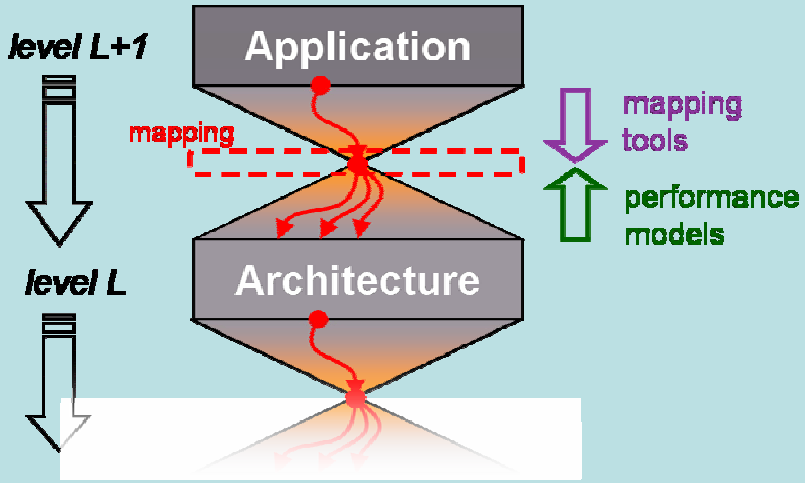
Courtesy: S. Gambini

Part V Summary:

Analog CAD gap is prevalent

System/Circuit design interface requires tremendous designer intuition

Designer intuition/modeling ability are not necessarily related

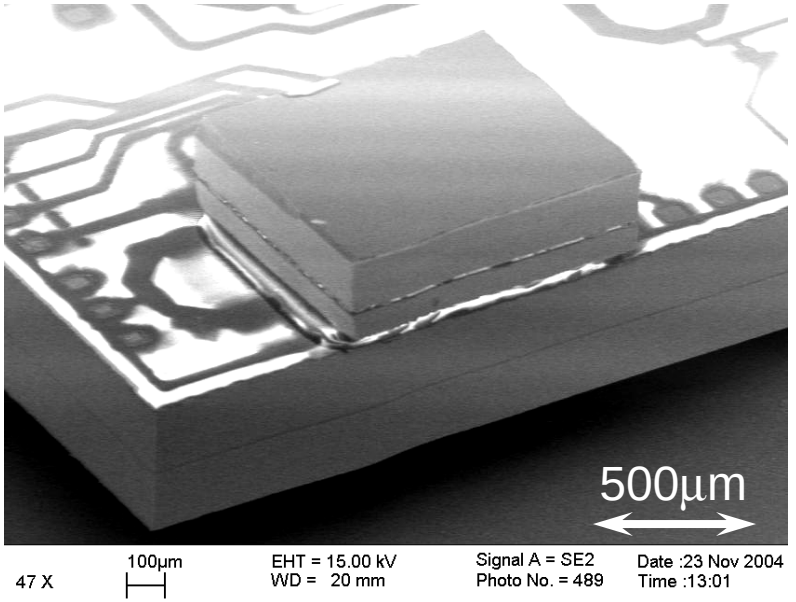


Analog Platform Based Design?

Y. Li, F. De Bernardinis, B. Otis, J. M. Rabaey, and A. Sangiovanni-Vincentelli, *"A Low-Power Mixed-Signal Baseband System Design for Wireless Sensor Networks"* CICC 2005

Conclusions

1. Electronics are becoming vanishingly small and truly ubiquitous



2. The convergence of many different disciplines is needed for ultra-small, low power electronic systems

3. Future chips will include transistors, EM elements, MEMS structures, biological sensors, thin-film batteries, adaptive algorithms.. all designed together

4. Seamless simulation between systems is necessary to allow cross-discipline co-design (and protect against the “Law of Unintended Consequences”)