HDL based Simulation of digital RF Frequency Synthesizers

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Chair of Integrated Analog Circuits

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Outline

- Motivation
- Demonstration Example: All-digital PLL for GSM systems
- Requirements in modeling RF-transceivers
- Design flow overview
- Abstract connectivity modeling for RF applications
- Summary

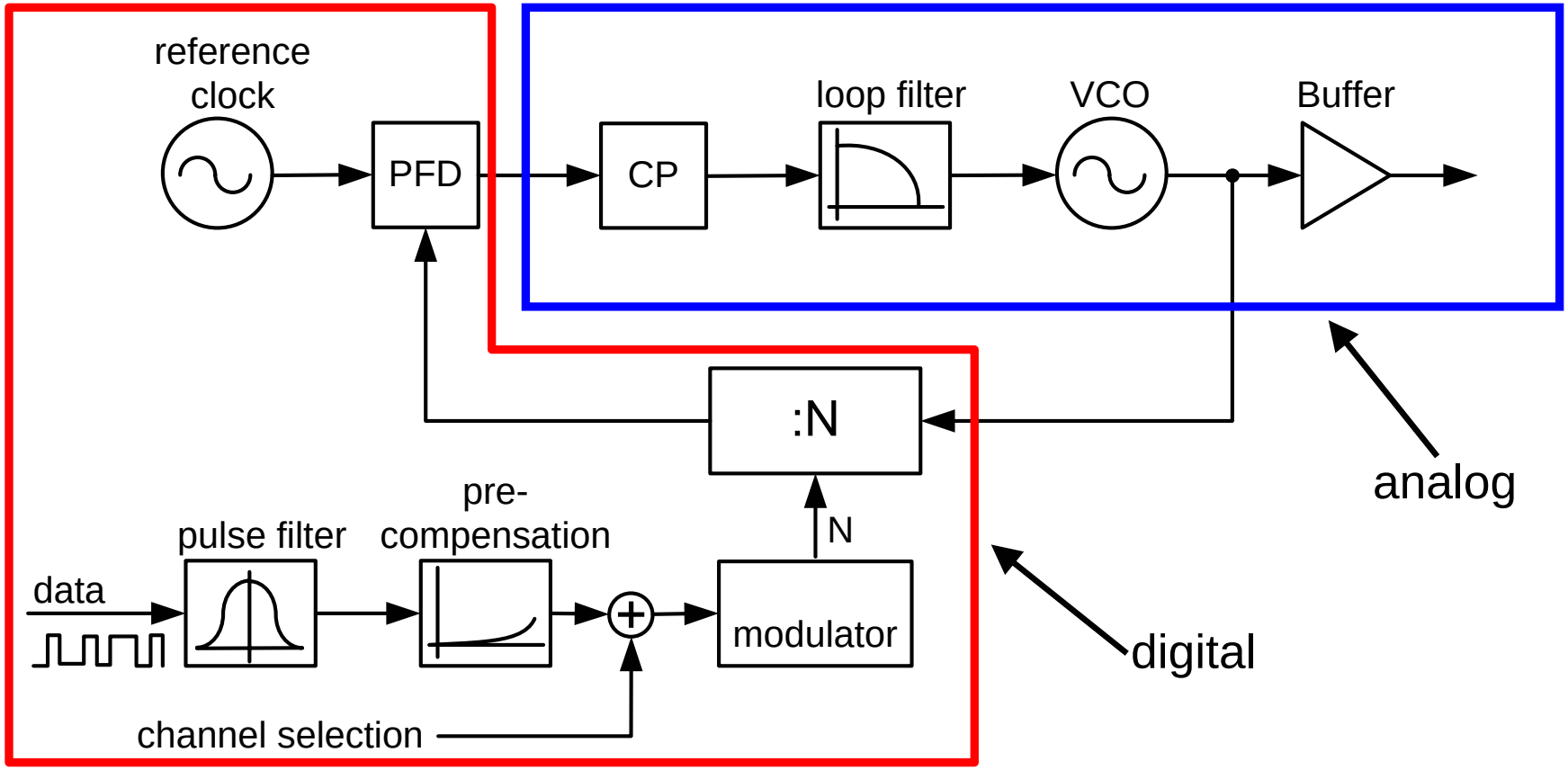
Motivation

- RF CMOS circuit implementation reaches nanometer scale
- Challenges for analog RF CMOS implementation
- Co-integration of digital baseband and analog RF circuits
  - Advanced design and verification tools
  - Advanced modeling techniques
- (Our target) HDL modeling of RF circuits
  - Connectivity verification
  - High performance transient simulation

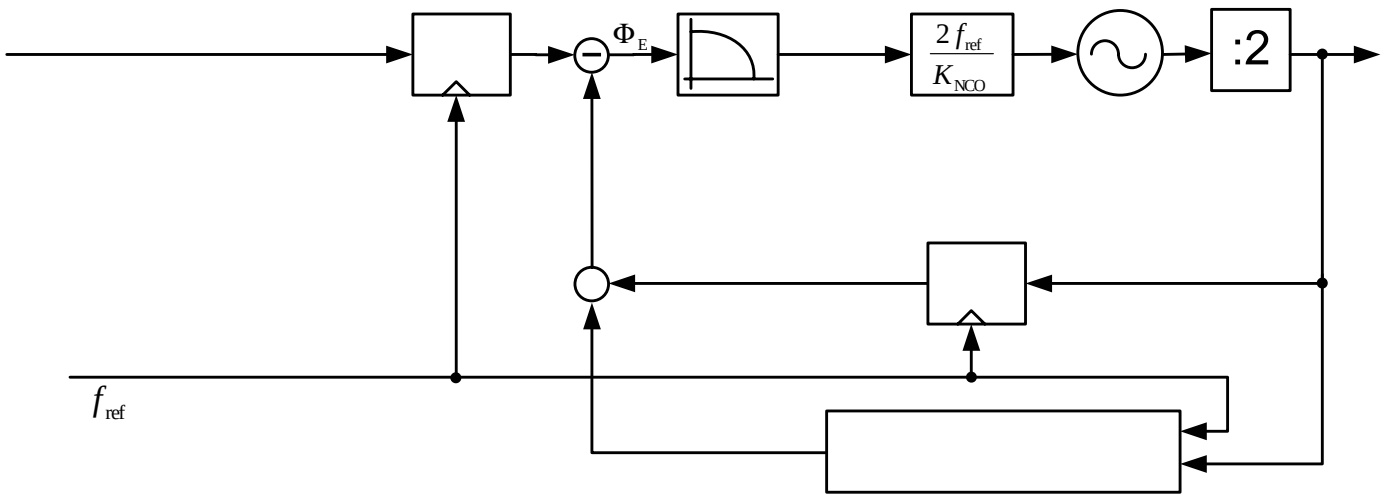
RF Circuits in Nanometer CMOS

- Challenges for analog RF CMOS scaling
  - Limited scaling qualities compared to digital circuits
  - Low voltage headroom
  - Increased non-idealities and manufacturing tolerances
  - Analog signals are sensitive to noise
  - Degraded signal-to-noise ratio
- RF architectures suited nanometer CMOS

Typical Mixed-Signal PLL Architecture



Demonstration Example: All-digital PLL

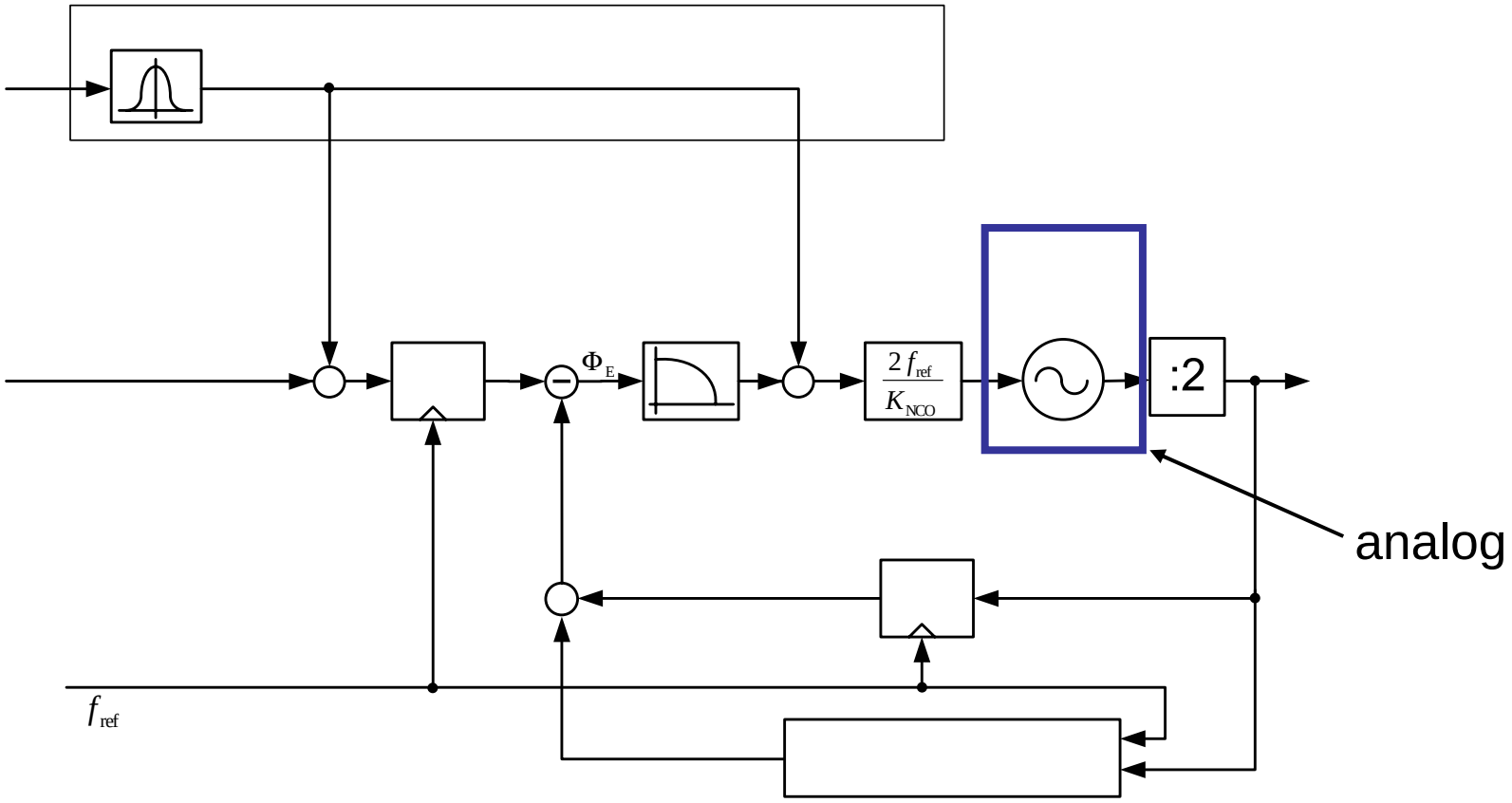


n

pulse filter

data

Demonstration Example: All-digital PLL



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Simulation & Post-Processing

- All-digital PLL implemented as pure VHDL model
- Simulation using two different simulators
  - Event-triggered simulator
  - Mixed-signal simulator
- MATLAB® for post-processing
  - Phase error calculation
  - Eye-diagram
  - PSD calculation

Eyediagram

Parameters:

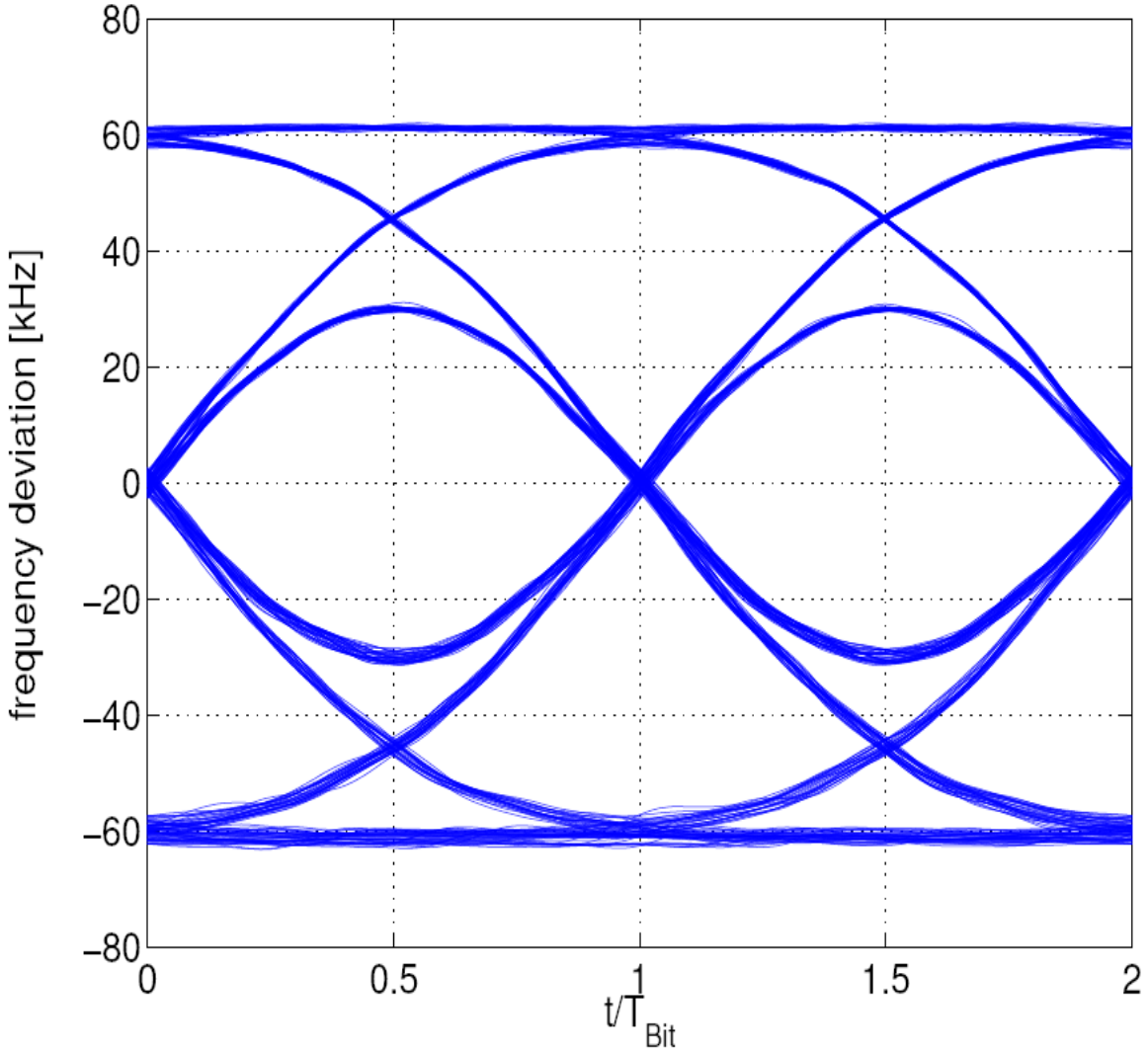
f_{ch} = 1.785 GHz;
f_{ref} = 13 MHz;
ω_n = 5 kHz;

Results:

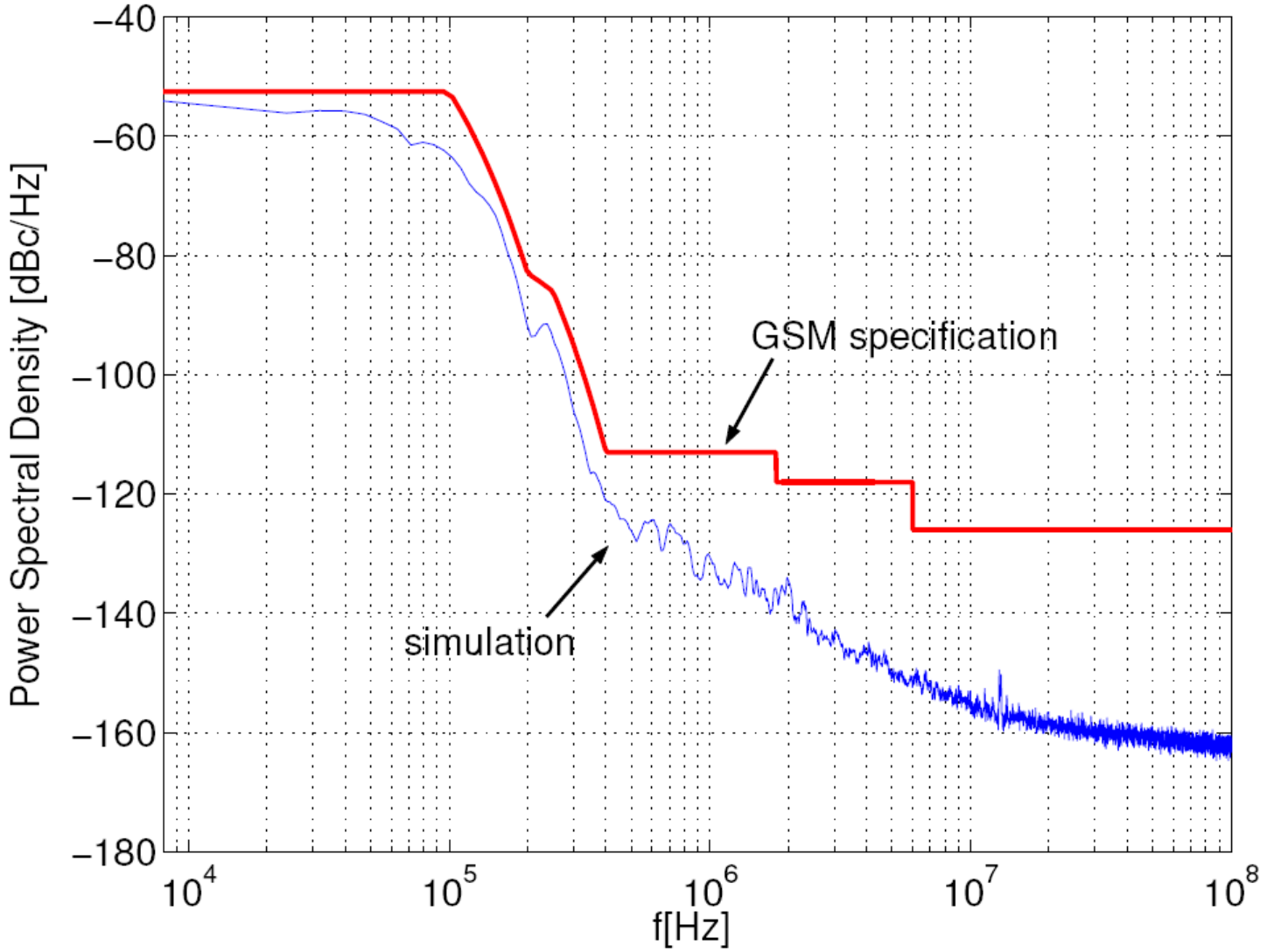
$\Phi_{E,rms}$ = 1.41°
$\Phi_{E,max}$ = 3.97°

Specification:

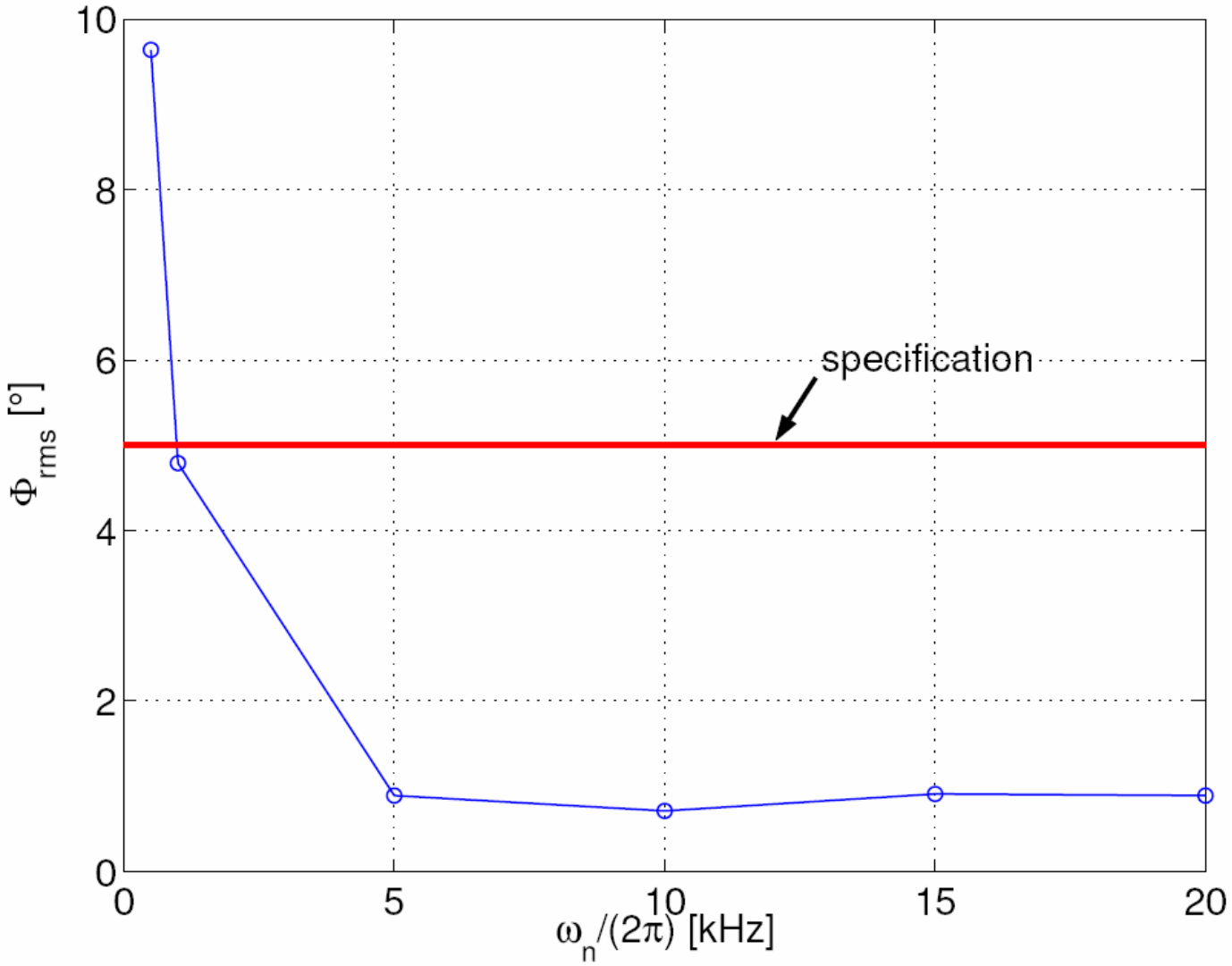
$\Phi_{E,rms,max}$ = 5°
$\Phi_{E,abs,max}$ = 20°



Power Spectral Density



RMS Phase Error vs. Natural Frequency ω_n



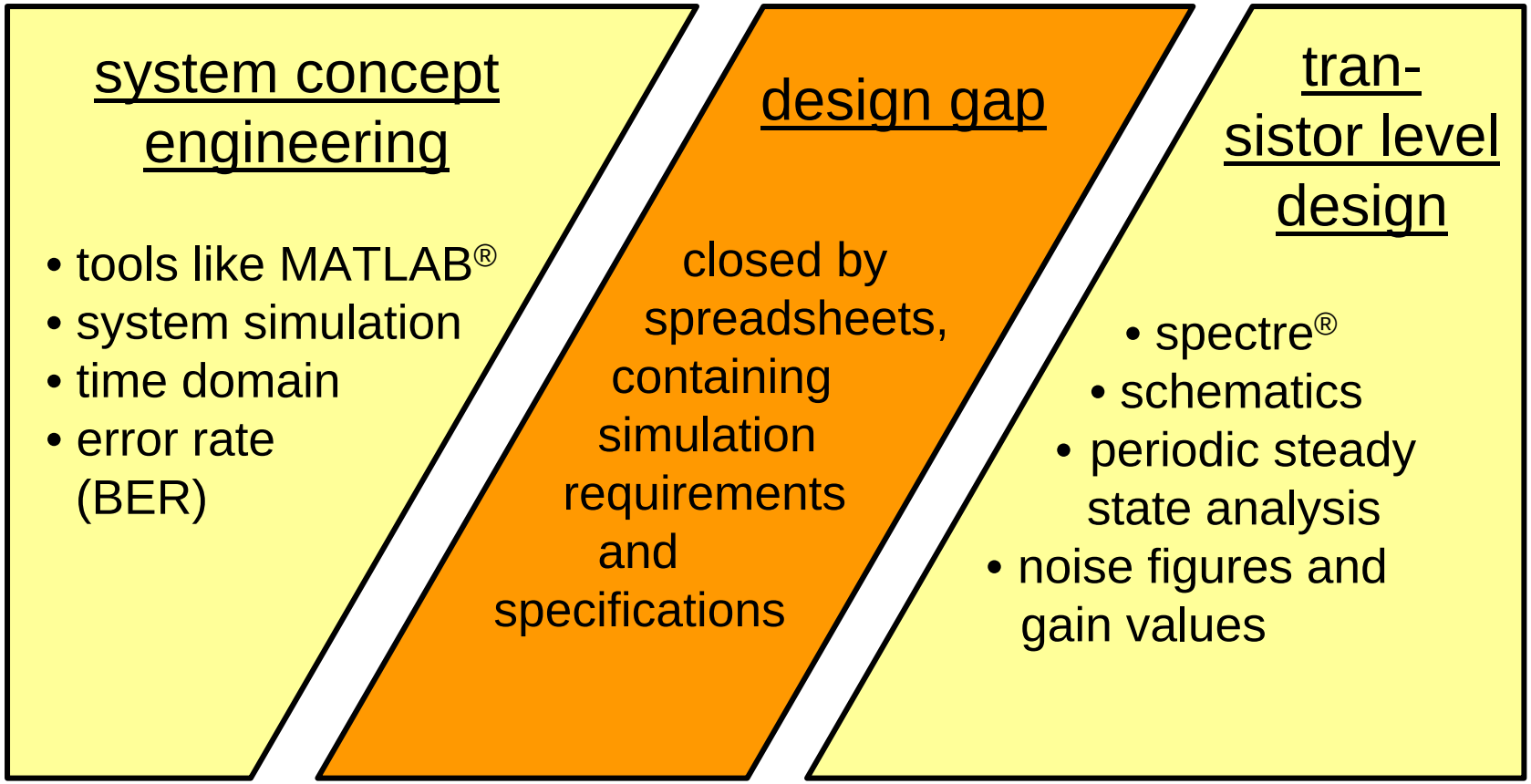
Demonstration Example: Simulation Times

All-digital PLL

Simulator	Simulation Time
digital simulator (event-triggered)	12 min.
mixed-signal simulator with pure digital model	120 min.
mixed-signal simulator and mixed-signal PLL	6 h

transient analysis of 2.2 ms on an Athlon 3200+ CPU

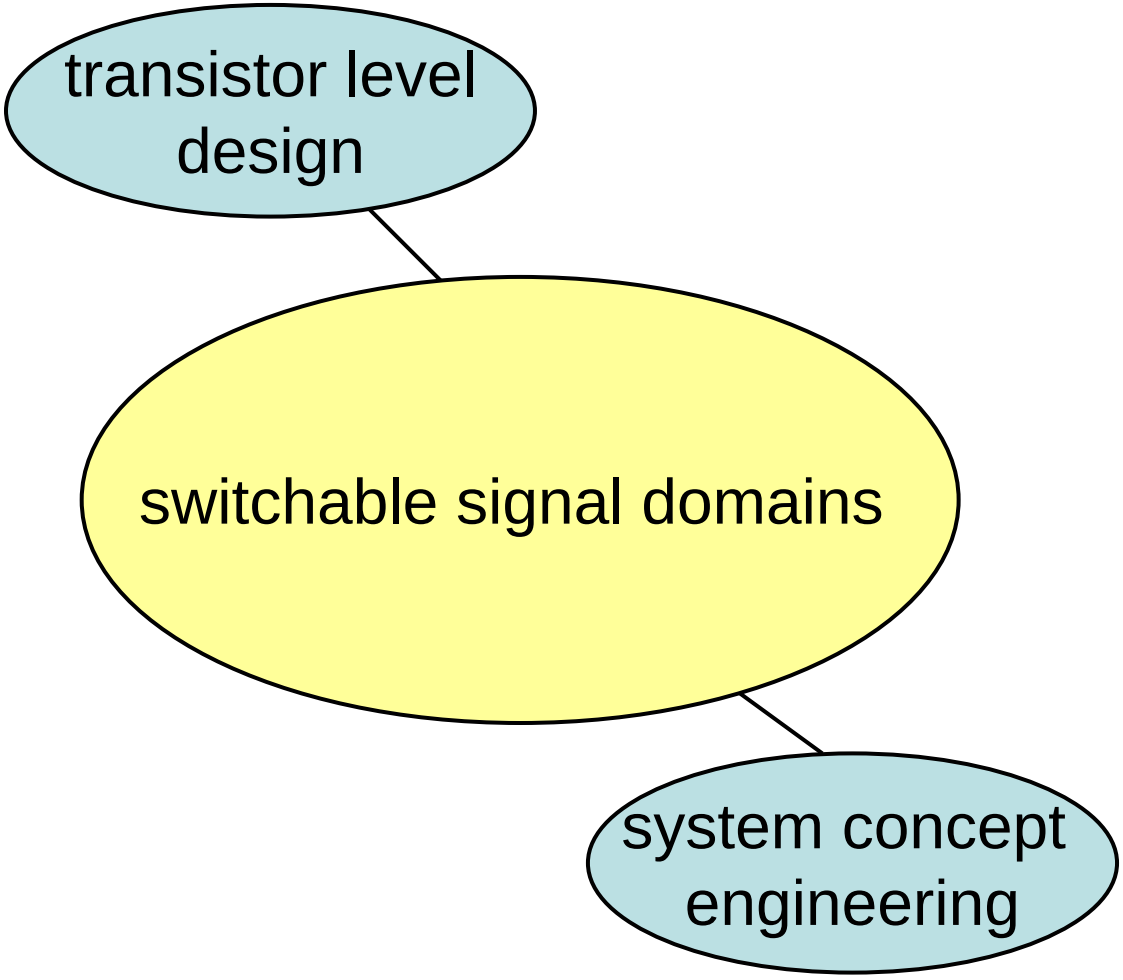
Current RF Design Flow



Requirements in Modelling RF-Transceivers

- Top-down design approach
- Switchable cell views for simulation speed-up
- Functional verification of the tape out database
  - Connectivity verification
  - Different cell views (baseband, transistor level etc.)
  - No manual interaction
- Enhanced post processing

Required Design Flow



- single simulation environment
- same schematics on each signal domain
- periodic steady state analysis for single blocks
- high performance transient analysis for functional verification
- consistent database

Abstract Interface Modelling for RF Applications

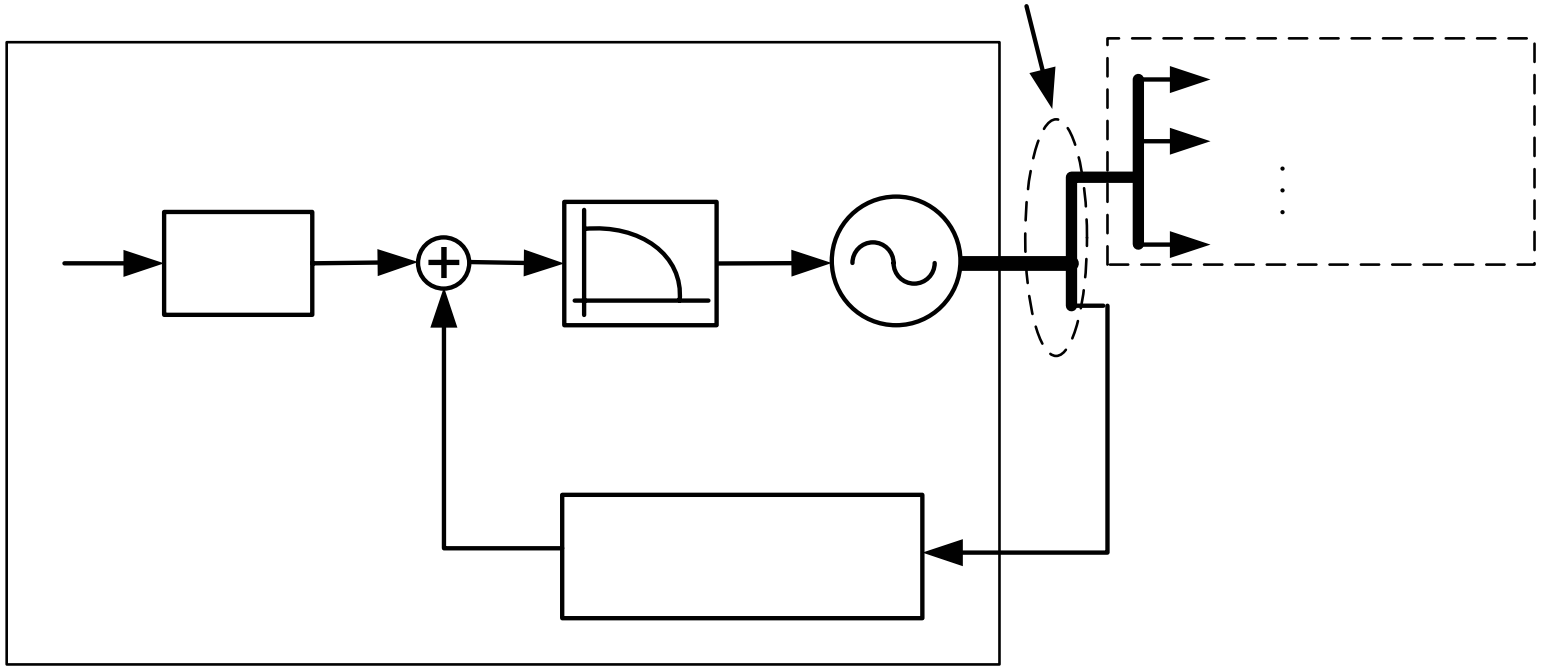
- Abstract data types
- Use of new constructs like ‘struct’ or ‘record’
- Switchable cell views and consistent schematics
  - Same schematics and connections between baseband models and transistor level to ensure connectivity throughout the design process

Companion Paper on this topic:

“Mixed-Mode and Mixed-Domain Modelling and Verification of Radio Frequency Subsystems for SoC-Applications”, Poster by Stefan Joeres on BMAS 2005

Proposed NCO Interface Description

using a struct-/record-data type:



Proposed NCO Interface Declaration

using a struct-/record-datatype:

System-Verilog:

```
typedef struct {
real I, Q;              // in phase, quadrature phase
real frequency;         // channel center frequency
[…]
} complex_signal_t;

typedef struct {  // discrete time interface
complex_signal_t fundamental; // for baseband
[…]
logic rf_out;           // rf_output for loop feedback
} nco_out_t;

module nco (output nco_out_t nco_output,
            input [fcw_length-1:0] fcw);
```

VHDL(-AMS):

```
TYPE complex_signal_t IS RECORD
I, Q : real;            -- in phase, quadrature phase
frequency : real;  -- channel center frequency
[…]
END RECORD;

TYPE nco_out_t IS RECORD
fundamental : complex_signal_t;  -- for baseband
[…]
rf_out : bit;               -- rf_output for loop feedback
END RECORD;

ENTITY nco IS
PORT( fcw :IN bit_vector( fcw_length-1 downto 0);
          nco_output :OUT nco_out_t);
END ENTITY nco;
```

HDL Languages on Schematic Level

- Mixed-Signal-Simulators use Verilog-AMS or Spice as top-level netlist format
  - Only analog nets and logic nets are available
  - No abstract data types supported on top-level
- Abstract data types for interconnections required
  - Supported by System-Verilog(-AMS) or VHDL-AMS
- System-Verilog is coming soon
- No AMS support in System-Verilog

Summary

- Proposing a RF interface modeling approach
  - Abstraction between connectivity and implementation level
- Demonstrated by an All-digital PLL implementation
- Future requirements for RF design tools
  - Better support and integration of HDLs in design flow
  - System-Verilog(-AMS) or VHDL-AMS as netlist format
  - Abstract signal types on schematic level
  - Functional and connectivity verification of the final tape out database for RF applications