A Multiple-Rotating-Clock-Phase Architecture for Digital Data Recovery Circuits using Verilog-A

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Presentation Outline

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- Clock and Data Recovery (CDR) Overview
- Oversampling CDR Architectures
  - Eye-Tracking Data Recovery Architecture
  - Previous Results
- Multiple-Rotating-Clock-Phase Architecture
- Description of Verilog-A Blocks
- Jitter Tolerance Test Bench
  - Simulation Methodology
- Simulation Results
- Conclusion
- Questions

Clock and Data Recovery (CDR) Overview

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- ***2x-oversampling PLL-based CDR circuits***
  - Traditional CDR circuits oversample the NRZ data stream twice per bit.

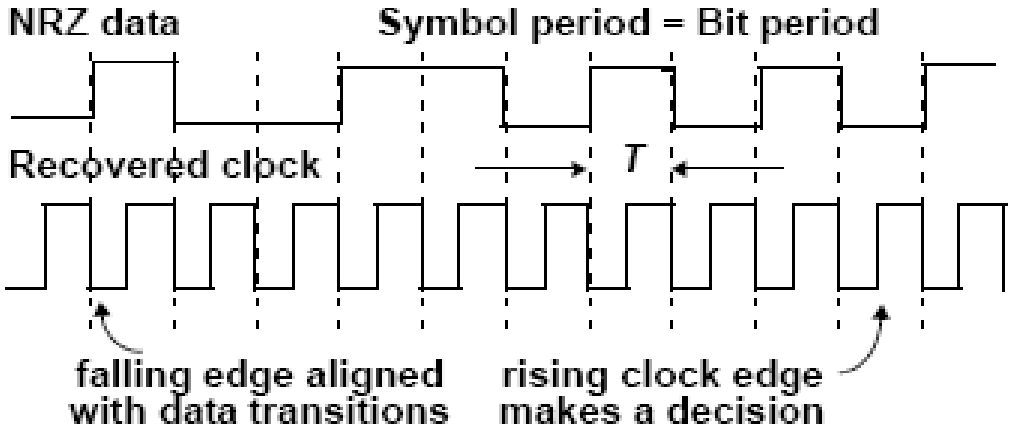


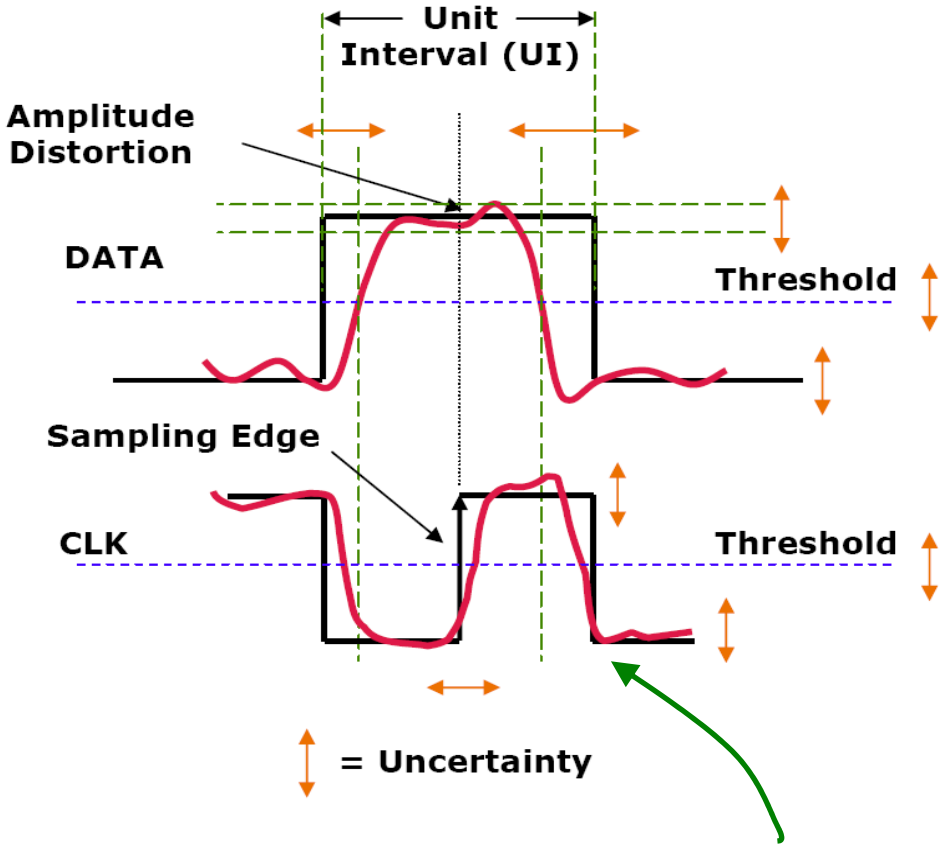
Fig. 1. Conventional 2x-oversampling concept

Ideal waveforms don't exist !

[14] S. I. Ahmed, Tad A. Kwasniewski, "Overview of Oversampling Clock and Data Recovery Circuits," *IEEE CCECE05,* Saskatoon, May 2005

CDR Design Challenges

- **Challenges**
  - Rise/Fall time
  - 50% duty cycle
  - Asymmetric Jitter
  - Threshold variation
  - PVT variations
  - Jitter Tolerance < 0.5 UI-pp $-t_r - t_f$
- **One Possible Solution**
  - *3x*-oversampling Circuits
  - Track both edges



3x-oversampling CDR Circuits

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- **Eye-Tracking Data Recovery Architecture [7]**
  - Tracks the center of the data eye, avoids data edges
  - Samples at the center of the data eye
  - 0.7 UI-pp Jitter Tolerance, 2.5Gb/s, 50 mW/ch, 0.18um-SiGe

All-Digital core

- **Variable Interval Oversampling Edge-Tracking Architecture [8]**
  - Tracks the rising and falling data edges
  - Samples at the center of the two data edges
  - 0.65 UI-pp Jitter Tolerance, 5 Gb/s, ¼ rate, ~500 mW, 0.35um CMOS

Mixed-signal core

- **Blind Oversampling (Phase Picking) Architecture [9], [10]**
  - Oversamples each bit blindly by an odd multiple of baud rate
  - Detect data transitions using an XOR gate / memory
  - Choose the best sample by center-picking or a majority vote
  - ~500 mW/0.35um CMOS/ 6.4 Gb/s

Algorithmic/All-Digital core

Please see references at the end of the paper; the above is a subset of techniques

Eye-Tracking Architecture [7]

- *How efficiently can the data transitions be detected w.r.t. the clock?*

How frequently is the clock position updated?

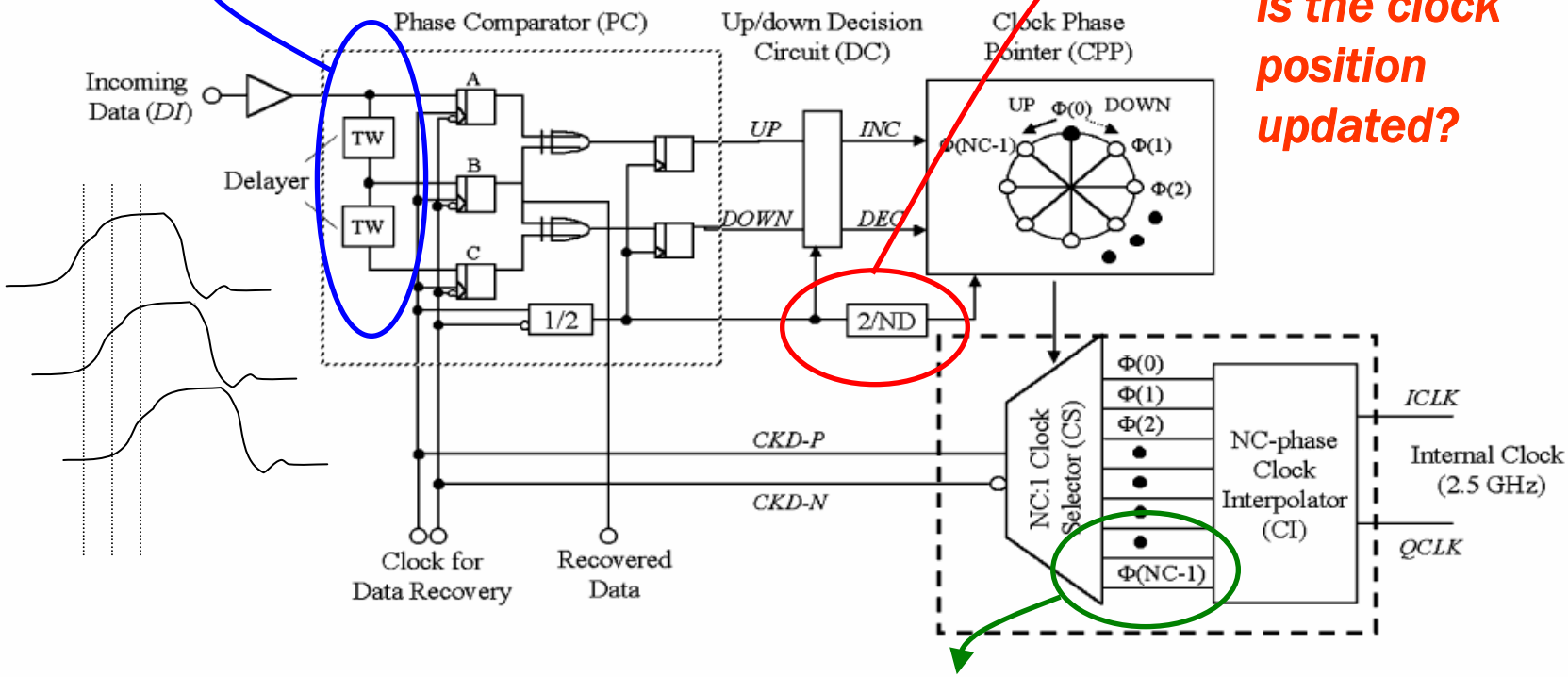


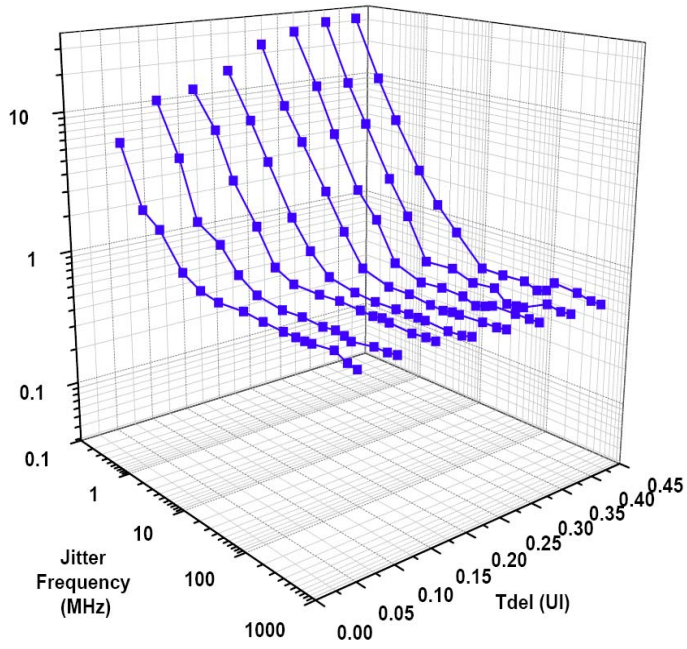
Fig. 1. DR circuit block diagram.

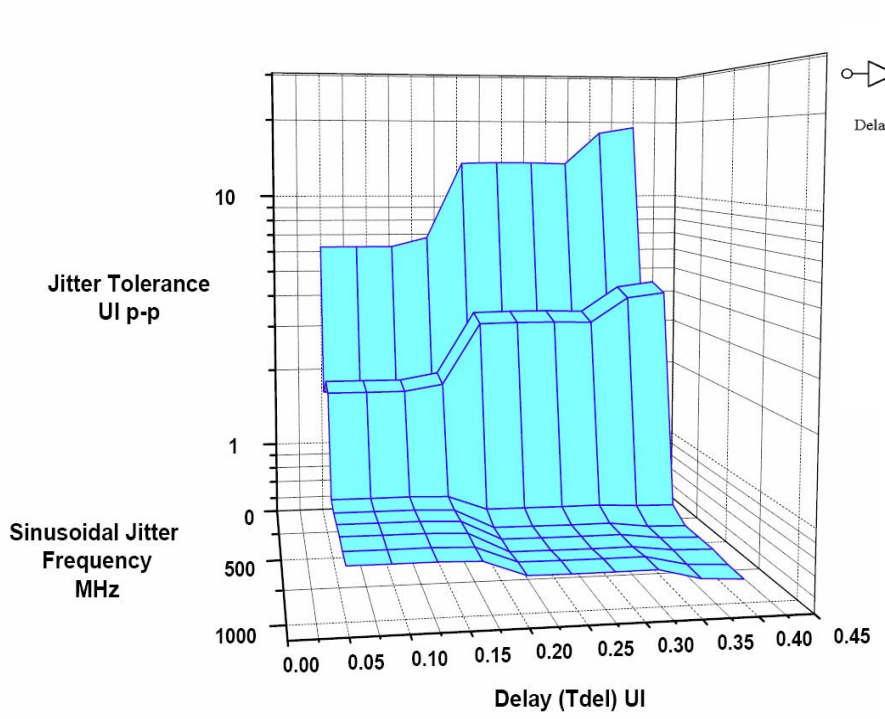
How big is the phase step?

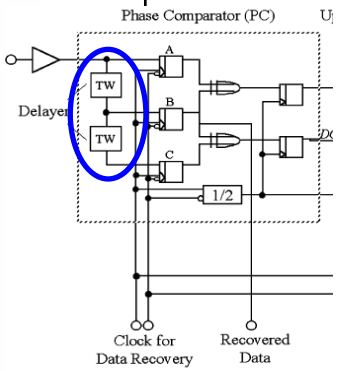
[7] Y. Miki *et. al*, "A 50-mW/ch 2.5-Gb/s/ch Data Recovery Circuit for the SFI-5 Interface with Digital Eye-Tracking," *IEEE J. Solid-State Circuits*, vol. 39, no. 4, Apr. 2004, pp. 613-621

Jitter Tolerance vs. Delay Value in the Bang-Bang Phase Detector Blocks (T_{del})

- Conflicting trend for high-frequency jitter tolerance and low-frequency wander tracking; Need to center the design



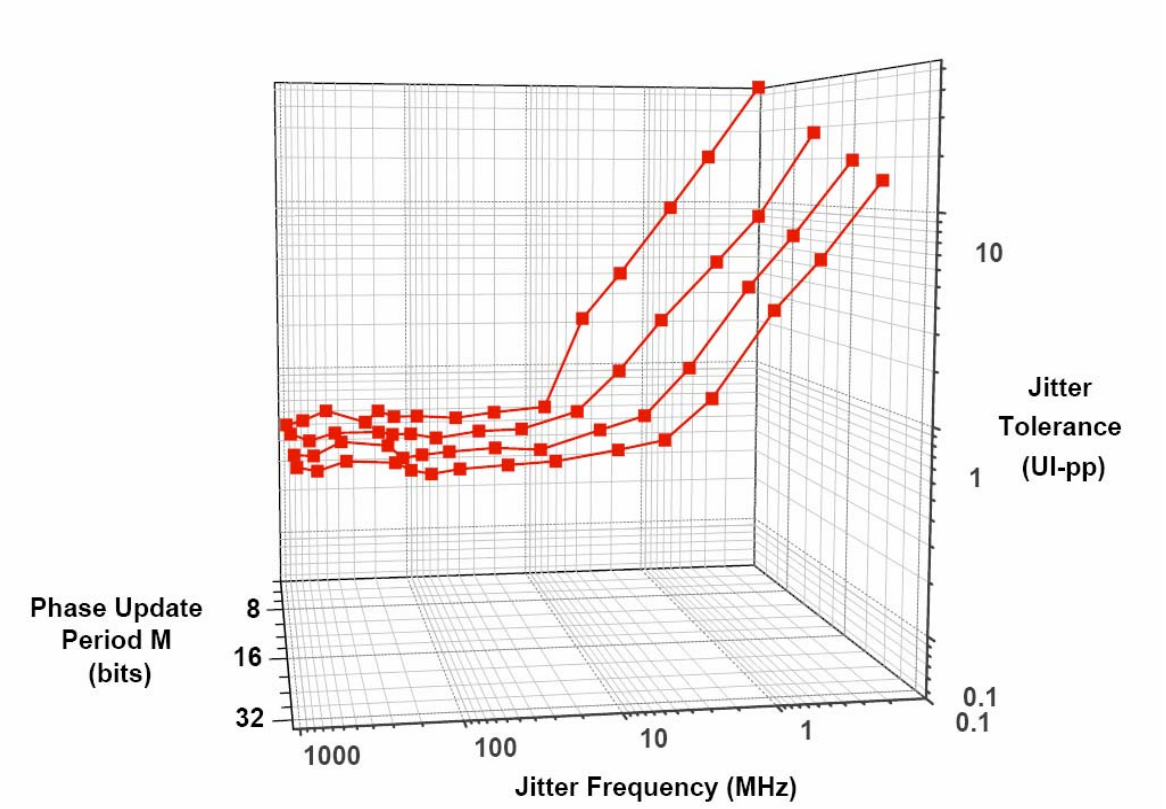


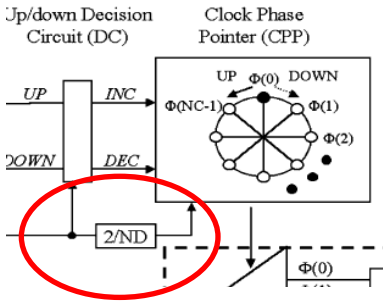


[13] S. I. Ahmed, Tad A. Kwasniewski, "An All-Digital Data Recovery Circuit Optimization Using Matlab/Simulink," *ISCAS 2005,* Kobe Japan, pp. 4485-4488

Jitter Tolerance vs. Phase Update Period (M)

- Faster the update, higher the bandwidth and vice versa

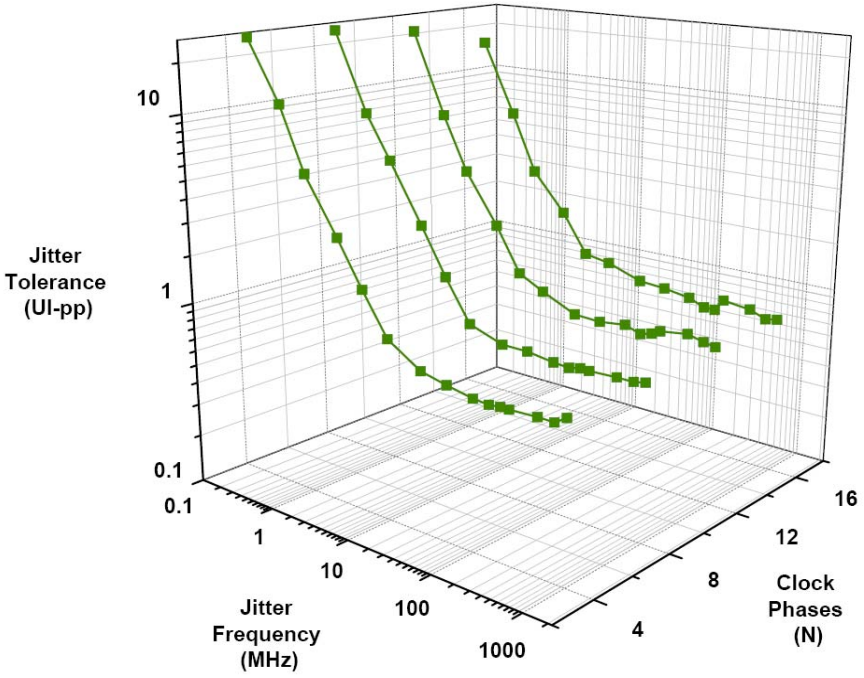


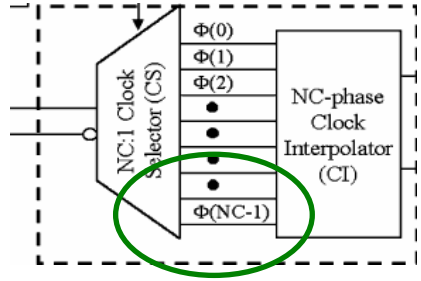


[13] S. I. Ahmed, Tad A. Kwasniewski, "An All-Digital Data Recovery Circuit Optimization Using Matlab/Simulink," *ISCAS 2005,* Kobe Japan, pp. 4485-4488

Jitter Tolerance vs. Number of Clock Phases (N)

- More clock phases = Finer/Smaller Updates for the same Update Period and more power dissipation
- More clock phases may require an analog interpolator !

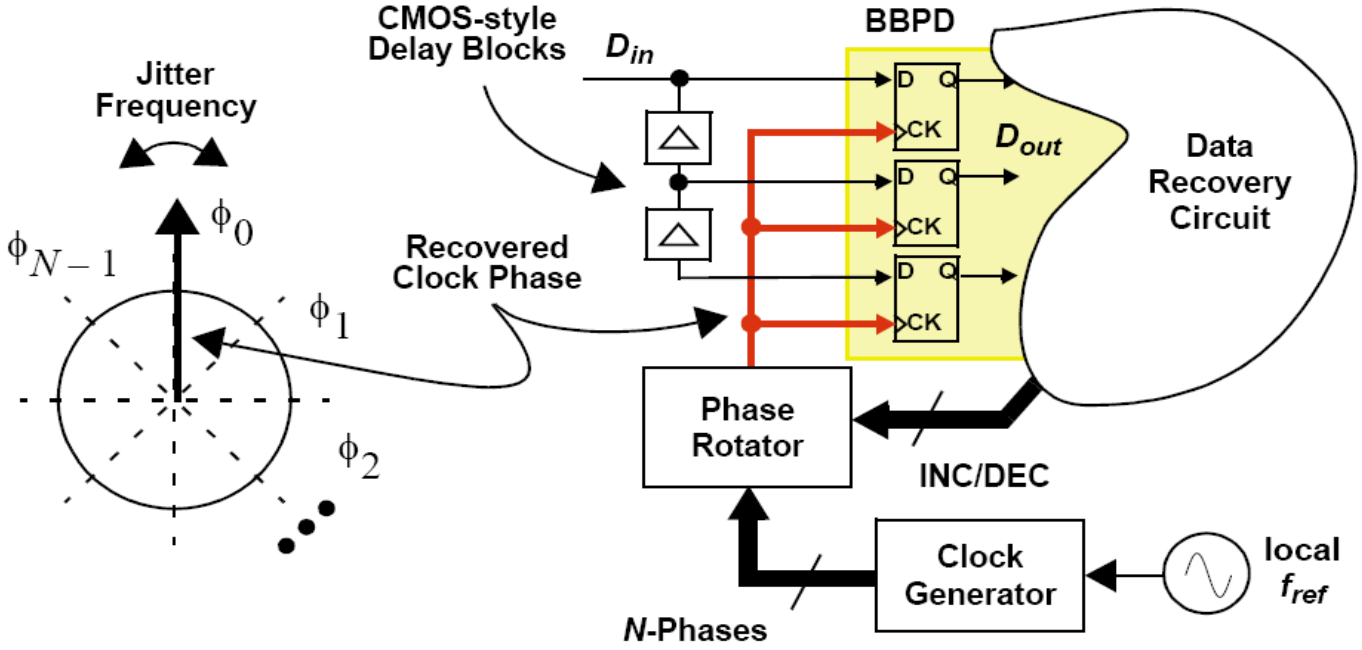




[13] S. I. Ahmed, Tad A. Kwasniewski, "An All-Digital Data Recovery Circuit Optimization Using Matlab/Simulink," *ISCAS 2005,* Kobe Japan, pp. 4485-4488

Eye-Tracking Architecture [7]

- One rotating clock phase
- Three data phases



[7] Y. Miki et. al, "A 50-mW/ch 2.5-Gb/s/ch Data Recovery Circuit for the SFI-5 Interface with Digital Eye-Tracking," IEEE J. Solid-State Circuits, vol. 39, no. 4, Apr. 2004, pp. 613-621

Multiple-Rotating-Clock-Phase Architecture

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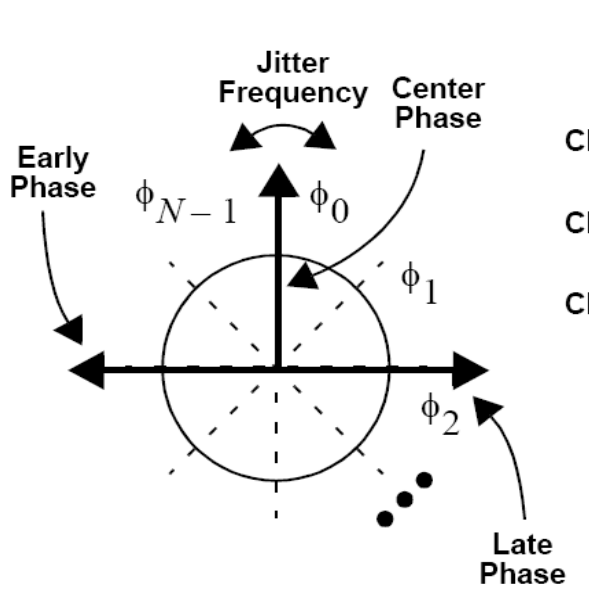
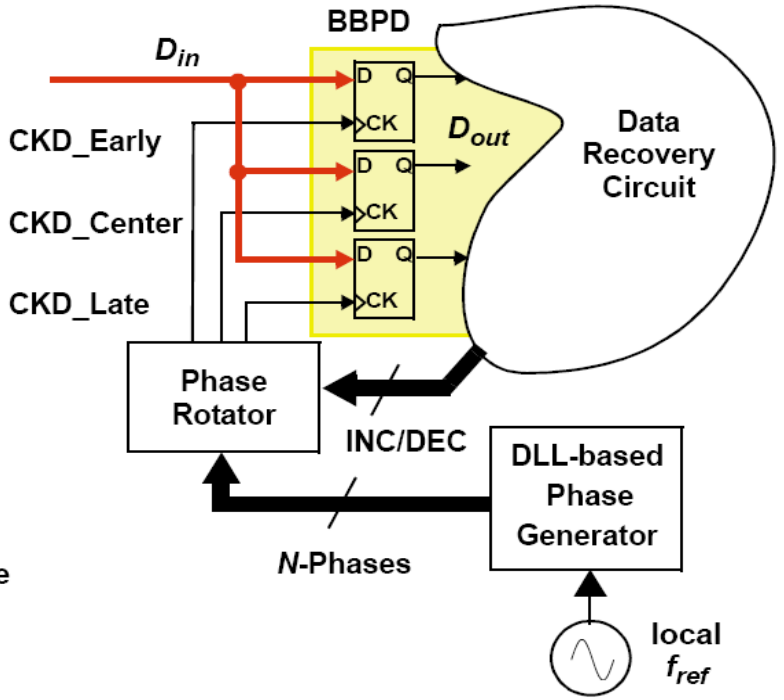
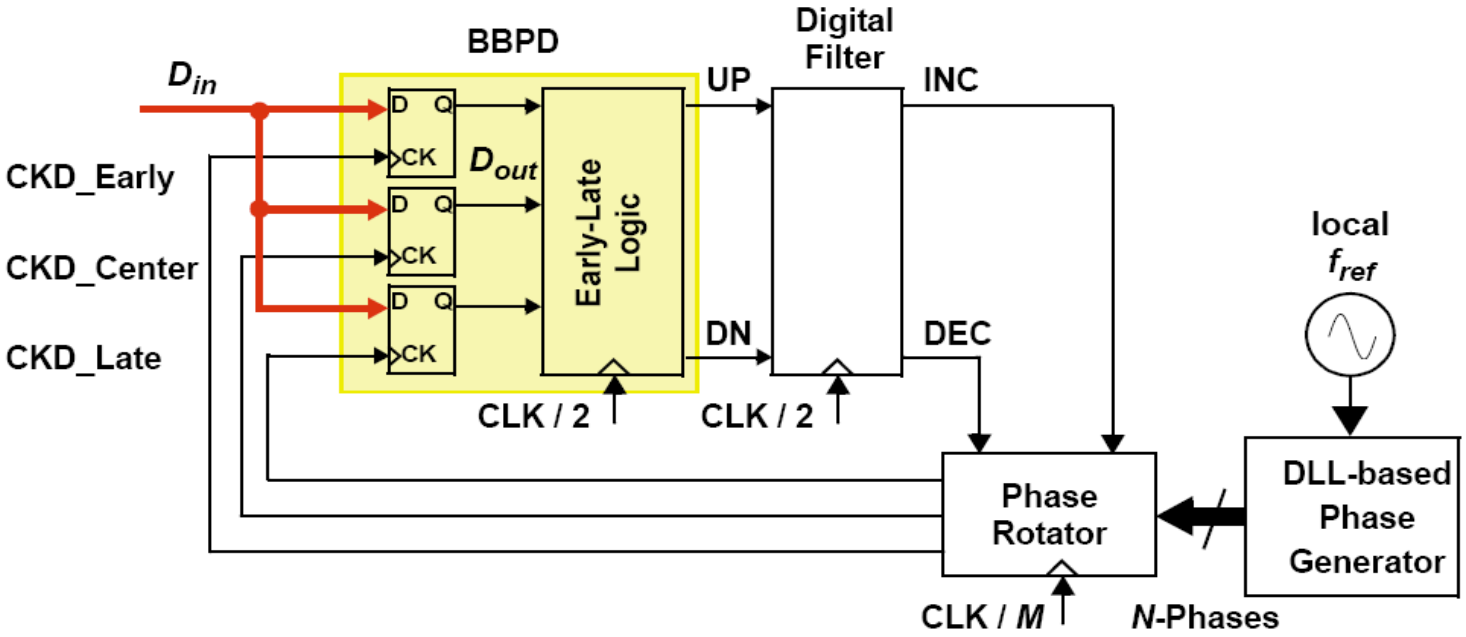
- Three rotating clock phase
- One data phase



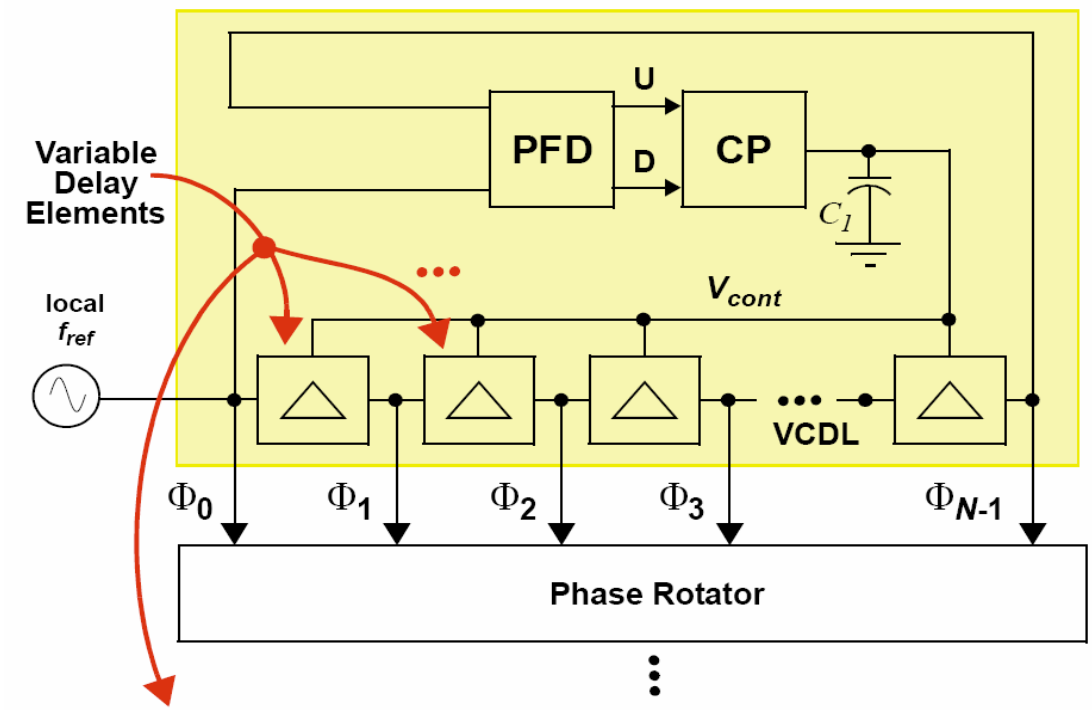


MRCP Architecture Block Diagram

- Since this is a new architecture, how can one model its 'behavior'? The behavior is not really known until a 'circuit' is put together
- Stay close to circuit blocks till the architecture is verified !



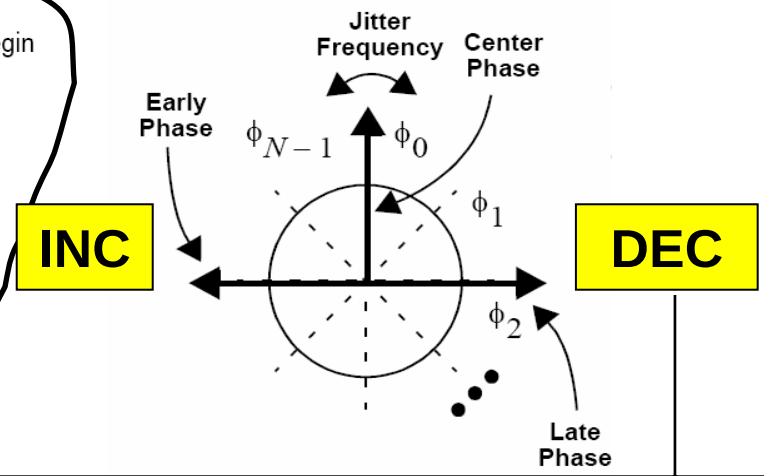
DLL-based Phase Generator



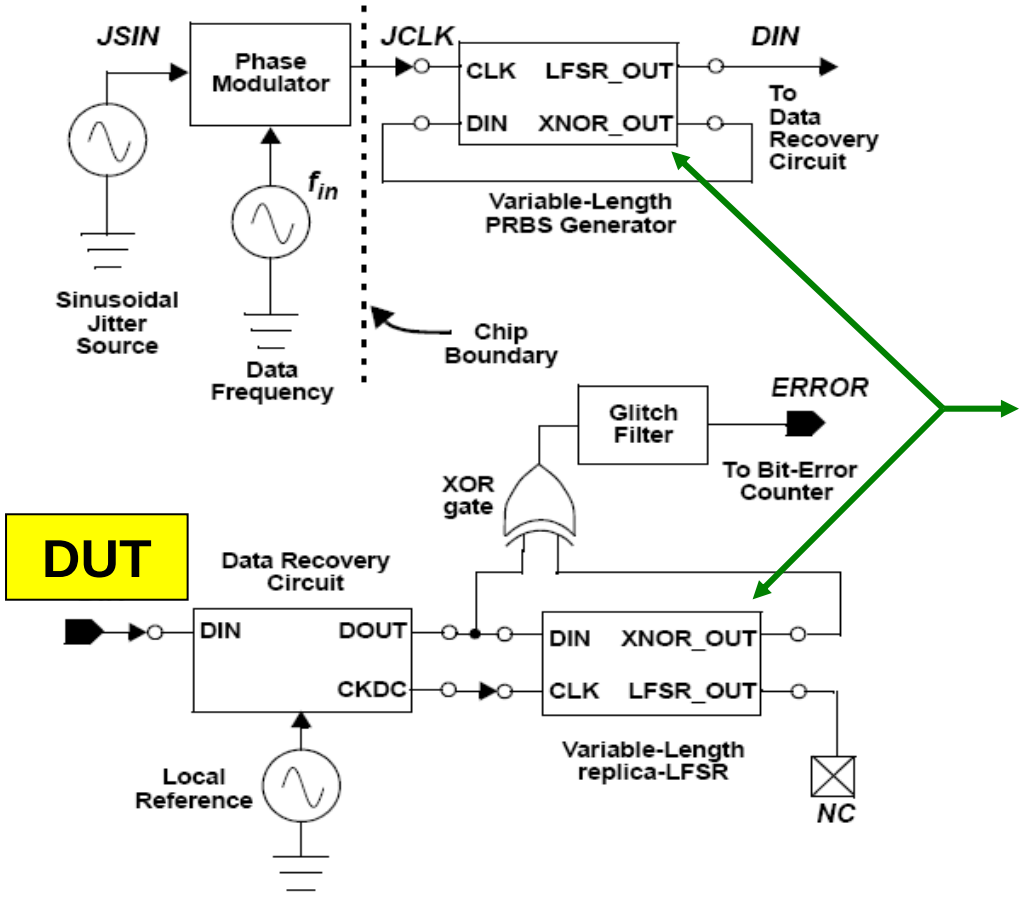

```
// ------------- 'analog' section for a Variable Delay Element
// ------------- vddval=supply voltage, static_offset= parameter, real
analog begin
    td = ( (min_delay - max_delay)/vddval) * V(vcont) + max_delay + static_offset;
      V(vout) <+ absdelay(V(vin), td );
end
```

Phase-Rotator Verilog-A Code

```
@ ( cross(V(clk) - threshold, +1)) begin

    if (V(inc) >= threshold && V(dec) < threshold && V(reset) < threshold) begin
        countl = countl - 1 ;
                if (countl < 1)  begin
                      countl = `MAX_PHASES;
                end
        countc = countc - 1 ;
                if (countc < 1)  begin
                      countc = `MAX_PHASES;
                end
        counte = counte - 1 ;
                 if (counte < 1)  begin
                      counte = `MAX_PHASES;
                 end
    end   // ---------------------------------------- End of INC operation

    else if (V(dec) >= threshold && V(inc) < threshold && V(reset) < threshold) begin
        countl = countl + 1;
                 if (countl > `MAX_PHASES)  begin
                      countl = 1;
                 end
        countc = countc + 1 ;
                 if (countc > `MAX_PHASES)  begin
                      countc = 1 ;
                 end
        counte = counte + 1 ;
                 if (counte > `MAX_PHASES)  begin
                      counte = 1 ;
                 end
    end   // ---------------------------------------- End of DEC operation

    //  ---------- Phase change (decision only) ouputs start here

     V(posc) <+ transition (countc, tdel_rot, tr_rot, tf_rot);
     V(pose) <+ transition (counte, tdel_rot, tr_rot, tf_rot);
     V(posl)  <+ transition (countl, tdel_rot, tr_rot, tf_rot);

end     //  ----------end analog statements
`undef MAX_PHASES
endmodule
```



Jitter Tolerance Test Bench



- Variable-length PRBS Generator
- Encoded in Verilog-A

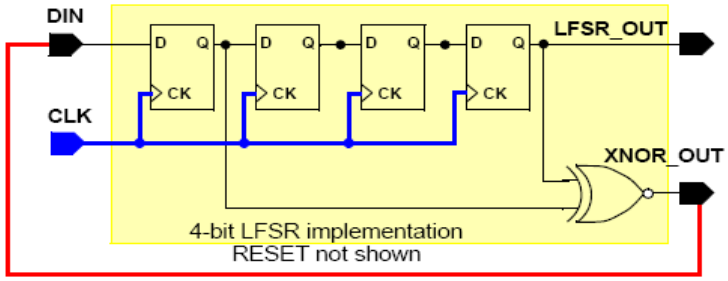
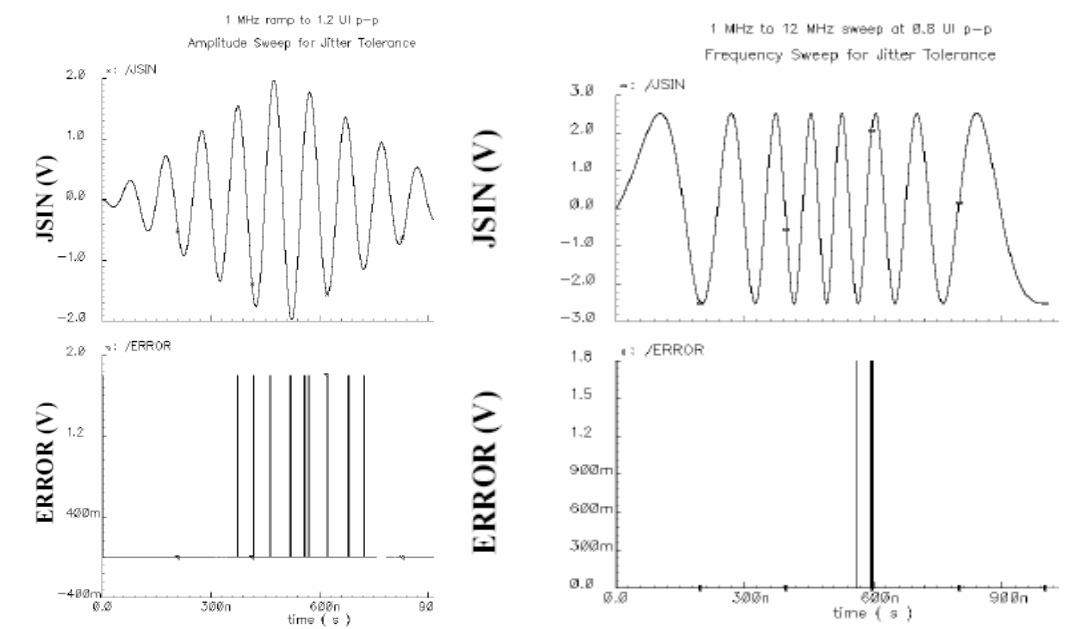


Fig. 1 Linear Feedback Shift Register

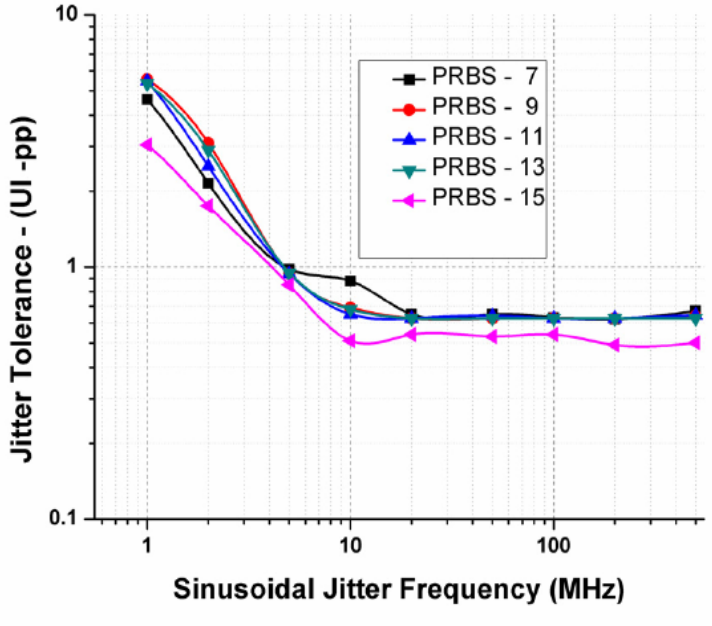
[15] S. I. Ahmed, Kent Orthner, Tad A. Kwasniewski, "Behavioral Test Benches for Digital Clock and Data Recovery Circuits using Verilog-A," *CICC 2005, in press*

Jitter Tolerance Simulation Methodology

- Where is the point of failure? Use an AM/FM sweep on *JSIN*
- This methodology reduces the simulation time significantly



AM Sweep **FM Sweep**



[15] S. I. Ahmed, Kent Orthner, Tad A. Kwasniewski, "Behavioral Test Benches for Digital Clock and Data Recovery Circuits using Verilog-A," *CICC 2005, in press*

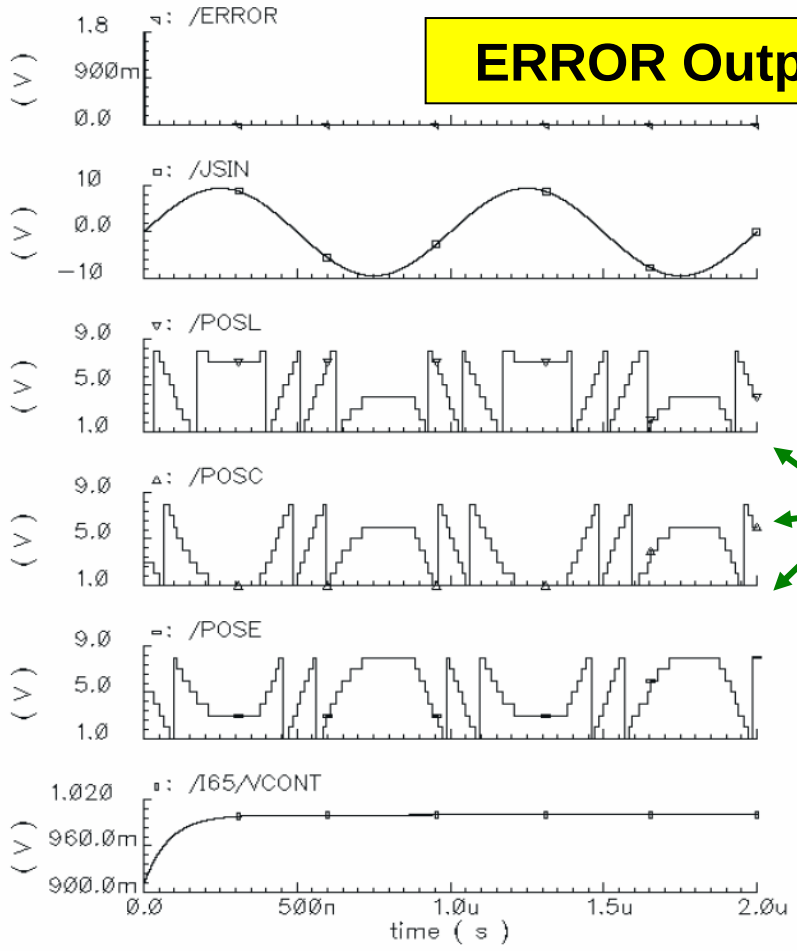
Functional Simulation

Parameters

- PRBS Length = $2^{11} - 1$
- Rise-time/Fall-Time = 100 ps
- CK-Q Delay = 75ps
- Gate Delay = 50 ps
- Number of Phases = 8
- Update period = 16 bits
- Phase Separation = 0.25 UI
- Data Rate = 2.5 Gbps
- Clock Frequency = 2.5 GHz

Techniques

- Top-level variables
- Configurable supplies, voltage swings, variable length PRBS, and patience



ERROR Output

3.0 UI-pp

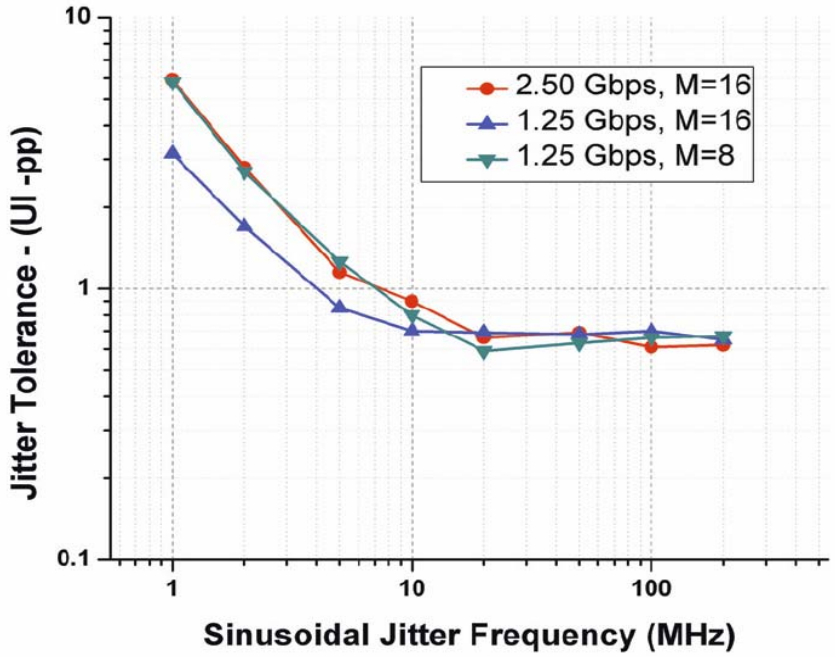
Phase Positions

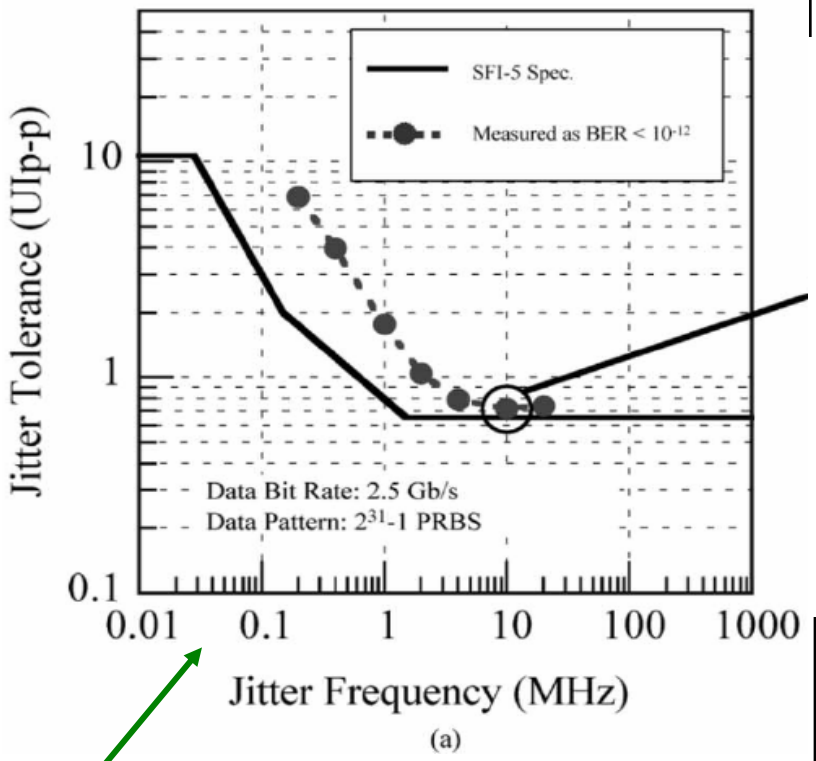
DLL control voltage

[16] for top-level flip-flop and gate parameters, [7] and [13] for DR parameters

Jitter Tolerance – Different Data Rates

… and a comparison with [7] !





[7] Y. Miki *et. al*, "A 50-mW/ch 2.5-Gb/s/ch Data Recovery Circuit for the SFI-5 Interface with Digital Eye-Tracking," *IEEE J. Solid-State Circuits,* vol. 39, no. 4, Apr. 2004, pp. 613-621

Session 4
Paper 4

Effect of Improperly Biased DLL Cells

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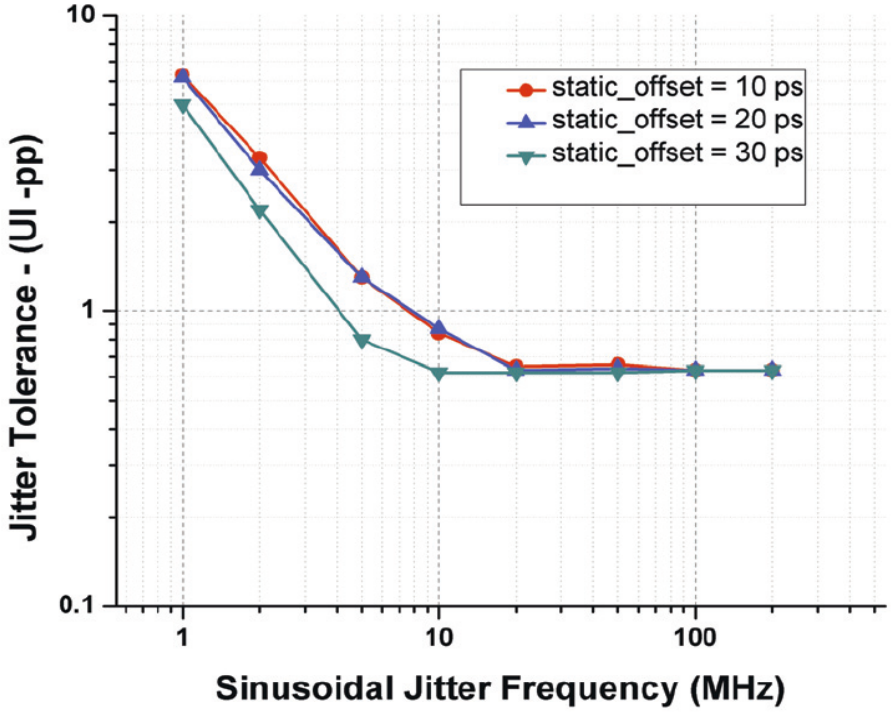
- Since the data detection window is rotating randomly, the effect of improperly biased cells is dithered out to some extent



Local Clock Frequency Deviation

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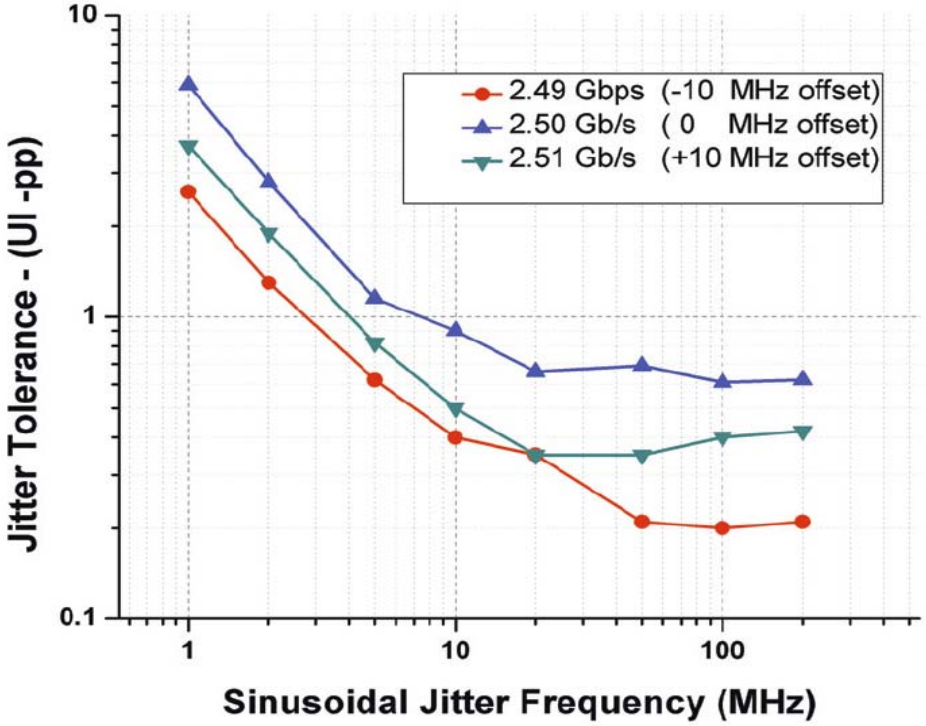
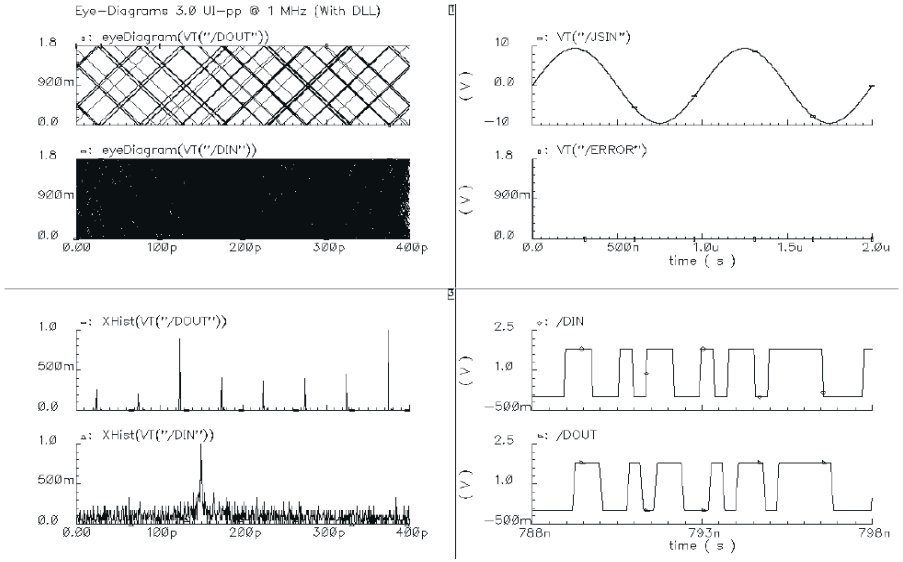
- Think about a long-term drift in the crystal frequency causing a drift in the local clock frequency

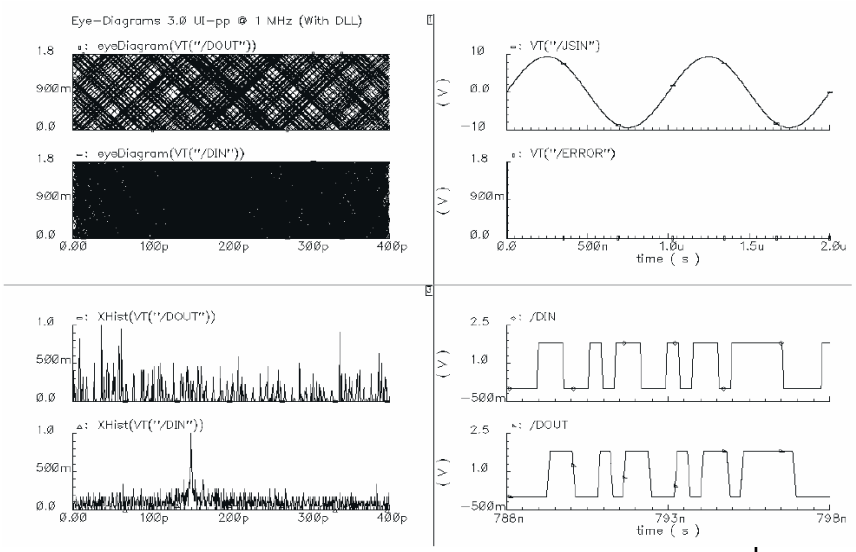


Jitter on Local Frequency Source

- Okay, so a source with 0.1 UI-pp jitter is a bad source !
- Jitter tolerance will be degraded from its nominal value



No jitter on local clock



0.1 UI-pp sinusoidal jitter

[18] Above histograms using 'Calculator Functions' from advICo Microelectronics, GmbH Germany

Conclusions

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- A Multiple-Rotating-Clock-Phase DR Architecture is proposed.
- The architecture is an extension of the eye-tracking architecture
- The data detection interval is set up by three rotating clock phases supplied by a DLL.
- The local clock is free-running and blind to the incoming data.
- The MRCP-DR architecture has a predictable jitter tolerance.
- The MRCP-DR architecture is tolerant of phase skews in the DLL.
- The MRCP-DR architecture is tolerant of jitter on local clock.
- The DR-core is all-digital and hence is portable
- Verilog-A test benches provide the ability to run what-if analyses at the early system-design stage.

Important References

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[6] R. Walker, "Clock and Data Recovery for Serial Digital Communications," *ISSCC Short Course*, Feb. 2002

[7] Y. Miki *et. al*, "A 50-mW/ch 2.5-Gb/s/ch Data Recovery Circuit for the SFI-5 Interface with Digital Eye-Tracking," *IEEE J. Solid-State Circuits,* vol. 39, no. 4, Apr. 2004, pp. 613-621

[8] S-H. Lee, M.-S. Hwang, *et al.*, "A 5-Gb/s 0.25-µm CMOS Jitter-Tolerant Variable-Interval Oversampling Clock/Data Recovery Circuit," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, Dec. 2002, pp. 1822-1830

[9] S. Kim, K. Lee, D-K. Jeong, D. D. Lee, A. G. Nowatzyk, "An 800 Mbps multi-channel CMOS serial link with 3x oversampling," *IEEE Proc. CICC '95,* pp. 451-455

[10] C-K. K. Yang, R. Farjad-Rad, M. A. Horowitz, "A 0.5-µm CMOS 4.0 Gbit/s serial link transceiver with data recovery using oversampling," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, May 1998, pp. 713-722

[11] *Cadence Verilog-A Language Reference,* ver. 5.1, January 2004

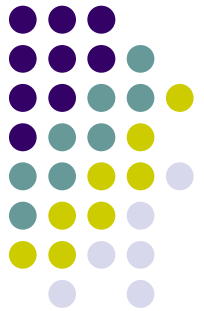
[12] *Matlab User Manuals*, ver. 7.0 R14, 2005, Mathworks Inc.

[13] S. I. Ahmed, Tad A. Kwasniewski, "An All-Digital Data Recovery Circuit Optimization Using Matlab/Simulink," *International Symposium on Circuits & Systems, ISCAS 2005*, May 23-26th, Kobe, Japan

[14] S. I. Ahmed, Tad A. Kwasniewski, "Overview of Oversampling Clock and Data Recovery Circuits," *Canadian Conference on Electrical and Computer Engineering, IEEE CCECE05,* Saskatoon, May 2005

[15] S. I. Ahmed, Kent Orthner, Tad A. Kwasniewski, "Behavioral Test Benches for Digital Clock and Data Recovery Circuits using Verilog-A," *Custom Integrated Circuits Conference, CICC 2005*, Sept. 18-21, 2005, San Jose, California, in press

[16] M. Usama, Tad A. Kwasniewski, "Design and Comparison of CMOS Current Mode Logic Latches," *International Symposium on Circuits & Systems, ISCAS 2004*, vol. 4, pp. 353-356



Thank you for your attention

Questions/Comments

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