Synthesis of CCII+s and CFOAs by manipulation of VFs and CMs

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ABSTRACT

A design automation method is introduced for the synthesis of CMOS positive second generation current conveyors (CCII+s) and current feedback operational amplifiers (CFOAs). The proposed method begins from the generation of basic building blocks such as voltage followers (VFs) and current mirrors (CMs), which are superimposed to synthesize the CCII+. Further, the CFOA is synthesized by cascading a CCII+ with a VF. Finally, it is shown the application of a CMOS CFOA to implement Chua's circuit, for which SPICE simulation results are presented by using CMOS technology of 0.35μm.

Keywords

Analog CAD, circuit synthesis, positive second generation current conveyor, current feedback operational amplifier, CMOS design.

1. INTRODUCTION

Nowadays, electronic design automation tools are going to be more suitable to generate analog circuits by manipulating the interconnection among basic building blocks [1]-[2], namely: current mirrors (CMs), input stages, output stages, etc. Furthermore, new topologies can be generated through the development of new methodologies based on the incorporation of design-knowledge. In this manner, a new synthesis method is proposed to synthesize the positive second generation current conveyor (CCII+) and the current feedback operational amplifier (CFOA) [3]-[5]. The proposed method is focused on the manipulation of voltage followers (VFs) [6]-[7], and CMs. The synthesis of the CCII+ is executed by superimposing two basic building blocks, a VF with a CM, as shown in section 2. In section 3, it is shown that the CFOA can be synthesized by cascading a CCII+ with a VF. The application of a CFOA to implement Chua's diode is shown in section 4. Finally, the conclusions are summarized in section 5.

2. SYNTHESIS OF THE CCII+

The superimposing of subcircuits, as shown in [8], leads us to generate useful circuits. For instance, the superimposing of a VF with a CM, generates the design of a CCII+. However, this procedure has to be realized by considering knowledge-rules to synthesize a circuit accomplishing the desired specifications. Lets consider the basic building block to describe a VF, as shown by Fig. 1(a). This VF has been widely used to design current conveyors, like the one introduced in [3]. Furthermore, other current conveyor topologies arises by choosing either: a different VF, e.g. those ones shown in Fig. 2, and a different CM. Besides, the difference among current conveyors depends on the manner in which current biases are synthesized.

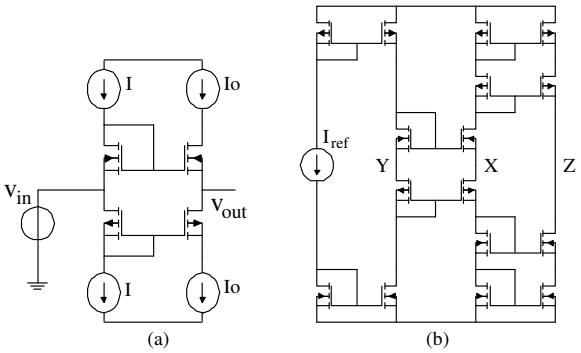

Figure 1: (a) VF biased with ideal current sources, and (b) synthesis of the biases to generate a CCII+

If current biases I and Io in Fig. 1(a), are synthesized by MOSFETs mirroring a current bias reference, then the first generation current conveyor arise, as shown in [3]. On the other hand, if current biases I are synthesized by MOSFETs mirroring a current bias reference, and current biases Io are synthesized by current mirrors whose output current-terminals are joined together, as shown by Fig. 1(b), then the CCII+ is obtained. In fact, the circuit shown in Fig. 1(b) accomplishes the equations modeling the behavior of a CCII+. That is: i_y=0, i_z=i_x, and v_x=v_y.

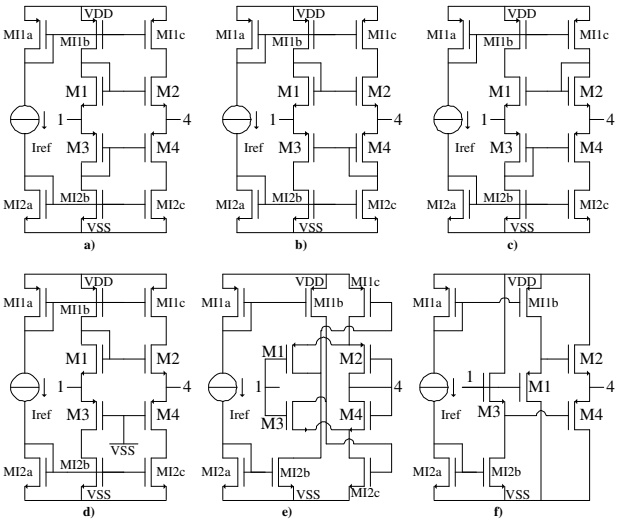

Figure 2: CMOS VFs synthesized from [7].

By selecting a group of VFs, like the ones shown in Fig. 2, new CCII+ topologies can be generated by exploration on their superimposing with a CM. For instance, in Fig. 2 transistors M1-M4 are synthesizing the small-signal VF, while the other MOSFETs are synthesizing the biasing circuitry, so that node 1 denotes the input port, while node 4 denotes the output port. If MOSFETs MI1c and MI2c are replaced by ideal current sources, then the current at the input port equals to zero, so that i_y=0 is accomplished. Now, if the ideal current sources are synthesized by CMs, as it was done for Io in Fig. 1, new CCII+s can be generated by exploration on the synthesis of current biases by any kind of CM. Most important is that after the generation of all possible CCII+ topologies, the best one can be selected by evaluation of its performance. This can be done by encapsulating its dominant behavior into an analytical design equation [9], at a level of abstraction higher than the transistor one. Afterwards, an optimized design can be generated by calculation of the appropriate sizes of the MOSFETs [10].

3. SYNTHESIS OF THE CFOA

As shown by [4], a CFOA can be synthesized by cascading three basic building blocks, a VF coupled to a current follower (CF) by connecting a floating resistor between they, afterwards, a VF is coupled with the CF by connecting a grounded resistor between the CF and VF. However, this topology can be minimized in components, by superimposing a VF with a CM to generate the CCII+ which is cascaded further to a VF, as shown in [5]. In this manner, many CFOA topologies can be generated by cascading all CCII+ topologies generated as shown in section 2, with any kind of VF, as the ones shown in Fig. 2.

By selecting the CCII+ shown in Fig. 1(b), and by selecting again the VF shown in Fig. 1(a), then the cascading of this circuits generates the CFOA shown in Fig. 3(a). Note that Io can be eliminated.

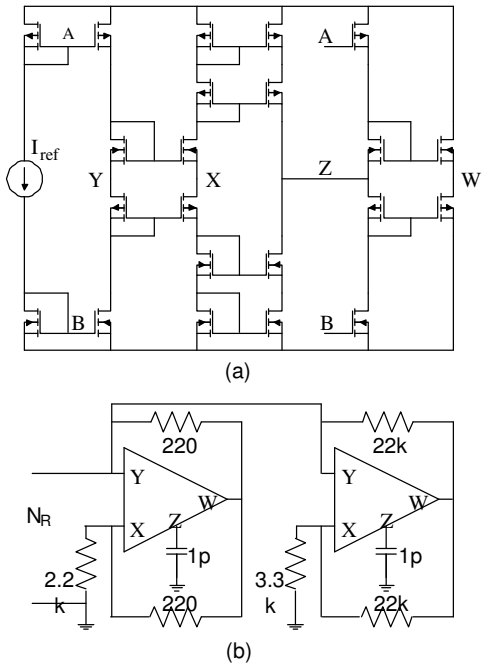

Figure 3: (a) Synthesis of a CFOA by cascading a CCII+ with a VF, and (b) its application to implement Chua's diode.

Other VF topologies can be cascaded to the CCII+ shown in Fig. 1(b). For instance, the terminals of a CFOA are labeled by Y, X, and Z to describe the CCII+, and Z, W to describe the VF. As one sees, the current sources I of the VFs can be synthesized by MOSFETs mirroring the current bias reference. In the same manner, although the current biases I, has been synthesized by simple current mirrors, they can be implemented by any kind of CMs, so that other CFOA topologies arise but by using the same small-signal circuitry for the VFs.

4. CMOS DESIGN AND APPLICATIONS OF THE CFOA

In electronics, a very interesting and simplest autonomous circuit which exhibits bifurcation and chaotic phenomena can be implemented by using one inductor, two capacitors, one linear resistor (R), and one nonlinear resistor (N_R), which is well-known as Chua's diode [11]. This third order autonomous chaotic oscillator has been realized by implementing N_R by using commercially available CFOAs [12], which has the advantage that its performance does not depend on a gain-bandwidth tradeoff, as for the design of operational amplifiers.

By using standard CMOS technology of 0.35μm from AMIS, by setting L=1μm, then all W sizes of all P-channel MOSFETs of the CFOA shown in Fig. 3(a) equal to 92μm, while all N-channel MOSFETs equal to W=85μm. Further, among all possible realizations of Chua's diode (N_R), in Fig. 3(b), it is shown an implementation by using the CFOA shown by Fig. 3(a). The whole CMOS design for N_R is biased by $V_{DD} = 1.2$, $V_{SS} = -1.2$ and $I_{ref} = 20\mu A$. By using SPICE, the I-V characteristic of N_R is shown by Fig. 4, where the slopes and breaking points can be adjusted by setting the appropriate values to the external elements to the CFOAs. Most important is that the piecewise linear I-V characteristic is well performed, where the breaking points are located at +114mV and -114mV, while the negative nonlinear behavior is performed between +400mV and -400mV.

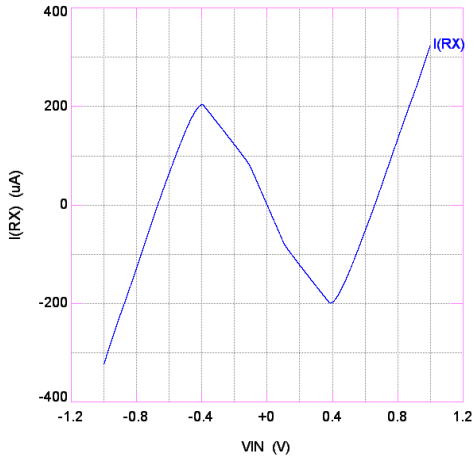

Figure 4: I-V characteristic of N_R implemented as shown by Fig. 3(b).

By using the design of N_R to implement the chaotic oscillator shown in Fig. 5, by setting L=1mH, C_1=450pF, C_2=1.5nF, and R=1650, then by using SPICE the double scroll attractor can be generated.

Other chaotic and bifurcation behaviours can be obtained by varying the value of the linear resistor, R. For

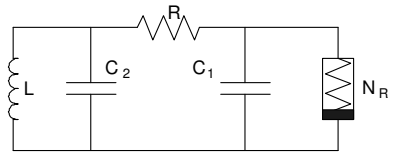

Figure 5: Chua's circuit

instance, by selecting V_{C1} and V_{C2} as state variables, the SPICE simulation result with V(6) associated to V_{C2} and V(1) to V_{C1}, is shown by Fig. 6.

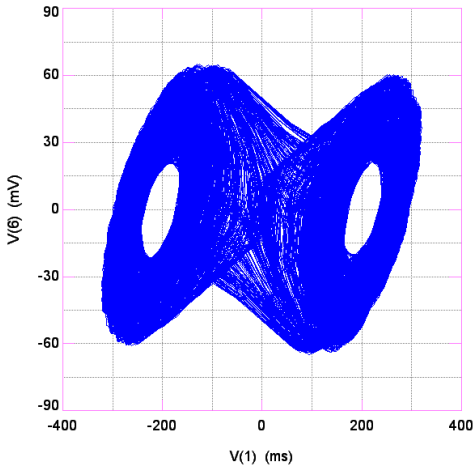

Figure 6: Double-scroll attractor

Although SPICE simulation results show the suitability of the CMOS CFOA shown by Fig. 3(a), to be used to implement N_R in Chua's circuit, better bifurcation and chaotic behaviors can be obtained by either: selection and optimization of another kind of topology for the CFOA, or by searching for the best element-values in Fig. 3(b) and Fig. 5.

5. CONCLUSION

It has been introduced the guidelines to implement an automatic synthesis methodology for CMOS CCII+s and CFOAs. It has been shown that both active devices can be synthesized by manipulation of VFs and CMs. The CCII+ was synthesized from a VF whose current bias sources, at its output port, should be synthesized without mirroring the current bias reference (Iref). The CFOA was synthesized by cascading a CCII+ with a VF, whose current biases can be synthesized by MOSFETs mirroring Iref, and the current biases at its output port can be eliminated.

Finally, it has been shown that a CFOA synthesized by executing the guidelines described along the artlicle, can be used to implement linear and nonlinear applications. For instance, by using SPICE and CMOS technology of 0.35μm, Chua's diode was implemented to simulate a chaotic oscillator generating the double scroll.

6. REFERENCES

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