Statistical Gate Level Simulation via Voltage Controlled Current Source Models

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Abstract

Current source based gate models achieve orders of magnitude of improved accuracy than the previous voltage source and effective load capacitance based gate models. Increasingly significant variability in DSM and nanometer scale VLSI designs calls for statistical analysis and optimization. In this paper, we propose a more efficient statistical gate level simulation method than Monte Carlo simulation based on current source based gate models. We represent a variational voltage waveform of any shape by a time domain statistical variable, and compute variational gate output voltage waveform by time domain integration of statistical variables which takes into account input voltage waveform variation and process variations with their correlations. Our experiments show that our statistical gate level simulation achieves over $20\times$ *efficiency improvement with an average of* 4.1%*(*22.3%*) accuracy loss for the means (standard deviations) of gate delay compared with* $1000\times$ *Monte Carlo simulation based on current source based gate models.*

1 Introduction

Traditional transistor level time domain analysis (e.g., as in SPICE) provides the most accurate circuit analysis, while efficient VLSI design analysis has been based on higher level of abstraction, e.g., table lookup based gate level delay calculation, and frequency domain model order reduction techniques [10] for on-chip interconnects of passive components (e.g., resistors, capacitors, and inductors).

CMOS transistors are essentially voltage controlled current sources, e.g., as in Alpha power law model [15]. CMOS gates therefore need to be modeled as voltage controlled current sources with intrinsic capacitor(s). E.g., a lookup table gives gate current for given input and output gate voltages, and a transient analysis gives the gate output voltage waveform [1]. Such current based gate models achieve orders of magnitude of improved accuracy than previous voltage source and effective load capacitance based CMOS gate models.

On the other hand, aggressive technology scaling introduced increased variability in VLSI designs. Lithography limitations of VLSI manufacturing equipments result in increased variations on transistor channel length, interconnect width. Chemical mechanical polishing (CMP) process affects interconnect thickness. Ion implantation atmosphere pressure affects doping density and transistor threshold voltage. Circuit runtime temperature and power/ground supply voltages are also observed to have increased variability. As a result, variational or statistical analysis and optimization techniques have been increasing important for VLSI designs.

Such techniques need to be enabled by statistical manufacturing process variability extraction, and principle component analysis (PCA) -like techniques can be applied to reduce the variabilities to a minimum set of independent statistical variables. VLSI statistical timing analysis takes into account the above mentioned variabilities extracted from manufacturing process, and propagate in a netlist signal arrival time distributions which are represented in probability density functions. In this paper, we consider gate level statistical simulation, which takes into account various physical aspects of variabilities (with their correlations in several signal integrity effects) and forms the basis of statistical timing analysis.

Statistical gate level simulation has been mainly based on Monte Carlo simulation, which is accurate yet non-efficient. Efficient statistical gate level simulation faces several challenges. (1) Input signal and process parameter variations and their correlations need to be taken into consideration. (2) A functional relationship between a gate input and a gate output needs to be extracted efficiently for (a) arbitrary input signal waveforms, and (b) arbitrary output load interconnect configurations. (3) Time domain integration computation in current-based gate models is very sensitive to input waveform variation, and small inaccuracy in input waveform characterization results in significant output waveform mismatch. Statistical simulation via current source based gate models need to address these challenges.

In this paper, we propose statistical gate level simulation (e.g., for delay calculation and noise analysis) via voltage controlled current source based gate models. We represent an input voltage waveform of any shape by a time domain statistical variable, and include process variations and input signal waveform variations as well as their correlations in statistical gate level delay calculation and noise analysis. We perform time domain integration of statistical variables for gate output voltage waveform, and achieve over $20\times$ improved efficiency with an average of 4.1 (22.3%) accuracy loss for the means (stadard deviations) of gate delay compared with $1000\times$ Monte Carlo simulation. The techniques applied here, e.g., correlation computation without the presence of a closed form funtional relationship, could be leveraged in solving the large extend of statistical timing analysis problem.

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The rest of the paper is organized as follows. We present the background of current based gate models and statistical analysis of VLSI circuits in section 2. We present our problem formulation and present our method to statistical gate level simulation in Section 3. We present our experimental results in Section 4 and conclude in Section 5.

2 Background

2.1 Current Source Based Gate Modeling

Traditional gate delay calculation is based on table lookup with input signal transition time and load capacitance indices. In deep submicron domain, load interconnects are distributed RLC networks. Effective capacitance [2] is proposed to approximate a distributed load interconnect such that the traditional table lookup method for gate delay calculation can still be applied. In this method, the gate model includes a voltage source which gives a ramp voltage, and a constant gate output resistance. Significant inaccuracy is observed in some cases in gate delay and output signal transition time calculation when using this model.

One source of inaccuracy is the increasingly complex signal waveforms in VLSI designs which increasingly deviate from ramp function. Another fundamental problem is that such gate models are inconsistent with MOS transistor physics, which says that a MOS transistor is a voltage-controlled current source in essence. A voltage-controlled current source based transistor model implies a voltage-controlled current source based gate model. We give detailed description as follows.

A MOSFET model is typically current-based, for example, the alpha-power law MOSFET model is as follows [15].

$$I_{DS} = \begin{cases} 0 & V_{GS} < V_T \\ \frac{W}{L_{eff}} \frac{P_C}{P_V} (V_{GS} - V_T)^{\alpha/2} & V_{DS} < P_V (V_{GS} - V_T)^{\alpha} \\ \frac{W}{L_{eff}} P_C (V_{GS} - V_T)^{\alpha} & V_{DS} > P_V (V_{GS} - V_T)^{\alpha} \end{cases} \quad (1)$$

where I_{DS} is the source-drain current, V_{DS} the source-drain voltage, V_{GS} the gate-source voltage, V_T the threshold voltage, W the channel width, L the channel length, P_C and P_V are parameters, α is typically between 1 and 2 to capture nanometer transistor effects.

For a simple inverter, such a transistor model gives a current-based gate model. For a complex gate, an equivalent inverter marcomodel can be constructed for each input combination [9], and gives a similar current-based gate model, e.g., for the worst case input combination for static timing analysis. Such current-based gate models better capture transistor physics and provide significant accuracy improvement compared with voltage-based gate models.

A simple current source based gate model includes a 2-D lookup table $I_o(V_i, V_o)$ which gives gate output current for a pair of gate input and output voltages, and a voltage-controlled capacitor C_g at the gate output (Fig. 1).[1] A transient analysis is applied to compute the gate output voltage,

[1] More complex gate models include various numbers of voltage controlled current sources, intrinsic capacitors, resistors, and inductors, which achieve improved accuracy, e.g., for radio frequency noise analysis.

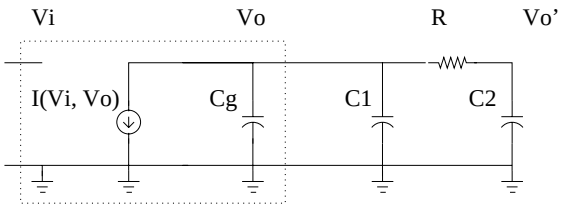

Figure 1. A current source based gate model which consists of a voltage-controlled current source $I(V_i, V_o)$ and an intrinsic gate output capacitor C_g, which drives a Pi-model load interconnect of resistor R, near end ground capacitor C_1, and far end ground capacitor C_2. An input voltage V_i gives near end voltage V_o and far end voltage V_o' of the load interconnect.

e.g., at each time step, the gate output current is given by the 2-D lookup table, and the gate output voltage variation is computed, e.g., by a nonlinear solver which applies Newton-Raphson or secant iteration [1]. Algorithm 1 describes the transient analysis process for a current-based gate model.

Algorithm 1: Transient Analysis with a Current Source Based Gate Model

Input: Input waveform $V_i(t)$, lookup table $I_o(V_i, V_o)$, intrinsic gate capacitance C_g, load interconnect of a RLC network
Output: Output waveform $V_o(t)$

1. Reduce the load RLC network, e.g., to a Pi-model
2. For each time step t
3. Find $V_i(t)$ and $V_o(t)$
4. Find $I_o(V_i, V_o)$ by table lookup
5. Compute $V_o(t + \Delta t)$

2.2 Statistical Analysis

Traditional VLSI analysis focuses on inter-die variations. As technology scales down, intra-die variations become increasingly significant, which include variations of a number of manufacturing process parameters, e.g., transistor threshold voltage, transistor channel length, gate oxide layer thickness, interconnect width and thickness, etc., as well as several circuit runtime parameters, e.g., power/ground supply voltages and on-chip temperature. Traditional best/worst case based timing analysis captures only inter-die variations, which provides only loose bounds in the presence of significant intra-die variations. It is expensive if not prohibitive to enumerate or sampling a large number of combinations of variations, e.g., in Monte Carlo simulation. Statistical timing analysis represents signal arrival time distributions in probability density functions and propagates such probability density functions in a netlist [7, 11, 16]. The resultant timing yield, or the probability for a chip to meet its timing requirements, gives more accurate evaluation for a chip.

Process variations include manufacturing process induced systematic variations and physical process induced purely random variations. E.g., a manufacturing process parameter p can be decomposed into its nominal value p_0, global or inter-chip variation ε_1, spatially correlated variation ε_2, and

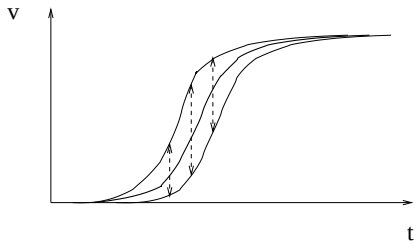

Figure 2. A variational voltage waveform represented by a time domain statistical variable $\tilde{v}(t)$ of mean $\mu_{v(t)}$, standard deviation $\sigma_{v(t)}$, and covariance $cov_{v(t_1),v(t_2)}$.

purely uncorrelated variation ε_3 as follows [3, 12, 14].

$$p = p_0 + \varepsilon_1 + \varepsilon_2 + \varepsilon_3 \tag{2}$$

Correlations exist in the global and the spatially correlated variation components. These correlations need to be addressed by either computation of a sufficient subset of higher-order correlations and higher-order moments of the variations, or by symbolic analysis techniques, e.g., affine arithmetics [8], probabilistic interval analysis [13], etc.

Early statistical timing analysis is based on Gaussian distribution assumption for the signal arrival times. A generic polynomial of statistical variables is proposed for a signal arrival time distribution, where the statistical variables are extracted from manufacturing process or via principle component analysis [5]. In this paper, we propose a different representation.

3 Statistical Gate Level Simulation

3.1 Time Domain Statistical Variations

We represent an arbitrary shape variational signal waveform by a time domain statistical variable $\tilde{x}(t)$, which has its means $\mu_{x(t)}$, standard deviations $\sigma_{v(t)}$, and higher-order moments for each time step t, as well as covariances $cov_{x(t_1),x(t_2)}$ between every two time steps t_1 and t_2, and other higher-order covariances. Figure 2 illustrates such a representation for a variational voltage waveform.

3.2 Problem Formulation

We present our statistical gate level simulation method in this section. Our problem is formulated as follows.

Problem 1 (Statistical Gate Level Simulation) Given

1. *variational input signal voltage waveform $\tilde{V}_i(t)$ of mean $\mu_{V_i(t)}$ and standard deviation $\sigma_{V_i(t)}$,*[2]
2. *current based gate model which includes*[3]
   (a) *input voltage controlled current source $I(V_i, V_o)$,*
   (b) *gate intrinsic output capacitance C_g, and*
   (c) *process variation induced gate current variation $\tilde{r}$ of mean μ_r and standard deviation σ_r,*

find *variational output signal voltage waveform $\tilde{V}_o(t)$ of mean $\mu_{V_o(t)}$ and standard deviation $\sigma_{V_o(t)}$.*

3.3 Method

Our method is based on time domain integration of statistical variables. We compute a variational function $\tilde{y} = f(\tilde{x})$ for a given variational variable $\tilde{x}$ (Fig. 2). For a current based gate model, the variational input voltage causes a variational gate output current at each time step, and results in a variational gate output voltage at each time step.

We present each step in details as follows.

3.4 Statistical Gate Current

We apply linear interpolation to the gate current lookup table and approximate $I(V_i, V_o)$ in a piecewise linear function of V_i and V_o as follows.[4]

$$I(t) = a_0 + a_1 V_i(t) + a_2 V_o(t) \tag{3}$$

The mean and the standard deviation of gate current $\tilde{I}(t)$ are given by

$$\begin{aligned} \mu_{I(t)} &= a_0 + a_1 \mu_{V_i(t)} + a_2 \mu_{V_o(t)} \\ \sigma^2_{I(t)} &= a_1^2 \sigma^2_{V_i(t)} + a_2^2 \sigma^2_{V_o(t)} + 2 a_1 a_2 cov_{\tilde{V}_i(t),\tilde{V}_o(t)} \end{aligned} \tag{4}$$

3.5 Statistical Gate Output Voltage

For a single capacitor load $C_L = C_g + C_l$, the gate output voltage is given by

$$V_o(t) = \int_0^t \frac{I(t)}{C_L} dt \tag{5}$$

Or, in its differential form,

$$\Delta V_o(t) = V_o(t + \Delta t) - V_o(t) = \frac{I(t)\Delta t}{C_L} \tag{6}$$

Therefore, $\Delta\tilde{V}_o(t)$ is given by

$$\begin{aligned} \mu_{\Delta V_o(t)} &= \frac{\mu_{I(t)}\Delta t}{C_L} \\ \sigma_{\Delta V_o(t)} &= \frac{\sigma_{I(t)}\Delta t}{C_L} \end{aligned} \tag{7}$$

And $\tilde{V}_o(t + \Delta t)$ is given by

$$\begin{aligned} \mu_{V_o(t+\Delta t)} &= \mu_{V_o(t)} + \mu_{\Delta V_o(t)} \\ \sigma^2_{V_o(t+\Delta t)} &= \sigma^2_{V_o(t)} + \sigma^2_{\Delta V_o(t)} + 2 cov_{\tilde{V}_o(t),\Delta\tilde{V}_o(t)} \end{aligned} \tag{8}$$

[2] Such input statistics are achieved either by statistical computaion for the previous stage, or by user specification for the primary inputs.

[3] We take a simple gate model for statistical delay calculation, while the same technique can be applied to more complex gate models, e.g., for noise analysis.

[4] In case that a higher order of polynomial approximation or other form of closed form approximation is applied, as long as an inverse function $V_i = \tilde{f}(I, V_o)$ is available, we can derive $\tilde{I}$ statistical gate current's probability density function for a given input variable x's probability density function.

3.6 Covariances

We compute covariances $cov_{\tilde{V}_i(t),\tilde{V}_o(t)}$ in (4) and $cov_{\tilde{V}_o(t),\Delta\tilde{V}_o(t)}$ in (8) to achieve $\sigma_{V_o(t)}$.

From statistics, we have

$$\begin{aligned} cov_{\tilde{V}_i(t),\tilde{V}_o(t)} &= \mu_{\tilde{V}_i(t)\tilde{V}_o(t)} - \mu_{V_i(t)}\mu_{V_o(t)} \\ cov_{\tilde{V}_o(t),\Delta\tilde{V}_o(t)} &= \mu_{\tilde{V}_o(t)\Delta\tilde{V}_o(t)} - \mu_{V_o(t)}\mu_{\Delta V_o(t)} \end{aligned} \quad (9)$$

where

$$\mu_{\tilde{V}_o(t)\Delta\tilde{V}_o(t)} = \mu_{\tilde{V}_o(t)I(t)}\frac{\Delta t}{C_L} \quad (10)$$

for a single load capacitance C_L.

Initially, we have $I(t=0)=0$, $V_i(t=0)$ and $V_o(t=0)$ are constant 0 or 1, so that all covariances are zero.

$$cov_{\tilde{V}_i(t=0),\tilde{V}_o(t=0)} = cov_{\tilde{V}_o(t=0),\Delta\tilde{V}_o(t=0)} = 0 \quad (11)$$

For covariances at the next time step $t+\Delta t$, we find the means of all the quadratic products of $V_i(t)$, $V_o(t)$, and $I(t)$ at current time step t. We have $\mu_{V_i^2(t+\Delta t)}$ given, and

$$\begin{aligned} \mu_{V_o^2(t+\Delta t)} &= \mu_{V_o^2(t)} + \mu_{V_o(t)I(t)}\frac{\Delta t}{C_L} + \mu_{I^2(t)}\frac{(\Delta t)^2}{C_L^2} \\ \mu_{V_i(t+\Delta t)V_o(t+\Delta t)} &= \mu_{V_i(t)V_o(t)} + \mu_{V_i(t)I(t)}\frac{\Delta t}{C_L} \\ &\quad + \mu_{\Delta V_i(t)V_o(t)} + \mu_{\Delta V_i(t)I(t)}\frac{\Delta t}{C_L} \end{aligned} \quad (12)$$

where

$$\begin{aligned} \mu_{V_i(t)I(t)} &= a_o\mu_{V_i(t)} + a_1\mu_{V_i^2(t)} + a_2\mu_{V_i(t)V_o(t)} \\ \mu_{V_o(t)I(t)} &= a_o\mu_{V_o(t)} + a_1\mu_{V_i(t)V_o(t)} + a_2\mu_{V_o^2(t)} \\ \mu_{I^2(t)} &= a_o + a_1^2\mu_{V_i^2(t)} + a_2^2\mu_{V_o^2(t)} + 2a_oa_1\mu_{V_i(t)} \\ &\quad + 2a_0a_2\mu_{V_o(t)} + 2a_1a_2\mu_{V_i(t)V_o(t)} \end{aligned} \quad (13)$$

Note that $\Delta V_i(t)$ is independent on $V_o(t)$ and $I(t)$, so that

$$\begin{aligned} \mu_{\Delta V_i(t)V_o(t)} &= \mu_{\Delta V_i(t)}\mu_{V_o(t)} \\ \mu_{\Delta V_i(t)I(t)} &= \mu_{\Delta V_i(t)}\mu_{I(t)}. \end{aligned} \quad (14)$$

3.7 Delay Variation

Gate delay D_g is given by the time t_d for the output voltage to reach $0.5V_{dd}$ and the time t_0 for the input voltage to reach $0.5V_{dd}$.

$$D_g = t_d - t_0 \quad (15)$$

Given the mean $\mu_{V_o}(t)$ and the standard deviation $\sigma_{V_o(t)}$ of the statistical gate output voltage waveform $\tilde{V}_o(t)$, assuming $\tilde{V}_o(t)$ in a Gaussian distribution, we compute the probability for the (rising) gate output voltage to reach the delay threshold voltage of $0.5V_{dd}$ at time t as follows.

$$\begin{aligned} Pr(V_o(t) > 0.5V_{dd}) &= 1 - cdf(V_o(t)) \\ &= \frac{1}{2}(1 - erf(\frac{0.5V_{dd} - \mu_{V_o(t)}}{\sigma_{V_o(t)}\sqrt{2}})) \end{aligned} \quad (16)$$

The probability for $t_d = t$, i.e., for the gate output voltage to reach $0.5V_{dd}$ for the first time at time t is given by

$$Pr(t_d = t) = Pr(V_o(t) > 0.5V_{dd}) - Pr(V_o(t-dt) > 0.5V_{dd}) \quad (17)$$

where dt is the time step.

Given t_d's probability density distribution in (17), we can compute the mean and the standard deviation of t_d. Similarly, we compute the mean and the standard deviation of t_0, i.e., the time for the gate input voltage to reach $0.5V_{dd}$. The mean and the standard deviation of gate delay are given as follow.

$$\begin{aligned} \mu_{D_g} &= \mu_{t_d} - \mu_{t_0} \\ \sigma_{D_g}^2 &= \sigma_{t_d}^2 - \sigma_{t_0}^2 \end{aligned} \quad (18)$$

3.8 Overall Algorithm

We summarizes our method in Algorithm 2.

Algorithm 2: Statistical Gate Level Simulation with a Current-Based Gate Model

Input: Variational input $\tilde{V}_i(t)$, gate model $I_o(V_i,V_o)$, C_g, $\tilde{r}$
Load capacitance C_L
Output: Variational output $\tilde{V}_o(t)$

1. For each time step t
2. Apply linear interpolation of $I(V_i,V_o)$ for (3)
3. Apply (4) for $\mu_{I(t)}$ and $\sigma_{I(t)}$
4. Apply (7) for $\mu_{\Delta V_o(t)}$, $\sigma_{\Delta V_o(t)}$
5. Apply (8) for $\mu_{V_o(t+\Delta t)}$, $\sigma_{V_o(t+\Delta t)}$
6. Apply (12) for $\mu_{V_o^2(t+\Delta t)}$, $\mu_{V_i(t+\Delta t)V_o(t+\Delta t)}$
7. Apply (13) for $\mu_{V_i(t+\Delta t)I(t+\Delta t)}$, $\mu_{V_o(t+\Delta t)I(t+\Delta t)}$, $\mu_{I^2(t+\Delta t)}$
8. Apply (9) for $cov_{V_i(t+\Delta t)V_o(t+\Delta t)}$, $cov_{V_o(t+\Delta t)\Delta V_o(t+\Delta t)}$
9. Apply (16), (17), and (18) for μ_{D_g} and σ_{D_g}

3.9 Application Notes

Our proposed statistical gate level simulation is fully integrated in transient analysis via time domain integration of statistical variables, which leads to preserved accuracy and efficiency. We achieve orders of magnitude of improved efficiency as is shown in our experiments.

One of the complexity of gate level analysis for DSM and nanometer VLSI designs are load interconnects, which need to take into account with their driver gates for simulation. However, load interconnects are of arbitrary configuration. They can be reduced by model order reduction techniques, e.g., to Pi-model circuits or s-domain transfer functions. Pattern matching and table lookup then can be applied, and interpolation can be applied to estimate a load interconnect, for efficiency improvement, much in a similar way to those in layout parasitic parameter extraction.

4 Experiment

We implement the statistical gate delay calculation via a current source based gate model in C++. We find the piecewise linear approximation of gate current by applying linear interpolation to the gate current lookup table and computing its derivatives. We compute the means and the standard deviations for the gate output voltage as well as the gate delay.

Table 1. Gate delay calculation by (1) statistical gate level simulation, and (2) Monte Carlo simulation via current source based gate models.

Cell name	T_r (ps)	C (fF)	$\mu_{D_g}(1)$ (ps)	$\sigma_{D_g}(1)$ (ps)	CPU(1) (s)	$\mu_{D_g}(2)$ (ps)	$\sigma_{D_g}(2)$ (ps)	CPU(2) (s)
Inv-x4	10.0	20.0	55.82	2.52	0.50	55.88	2.39	12.10
Inv-x4	10.0	50.0	135.87	6.50	0.50	135.94	5.51	12.00
Inv-x4	10.0	100.0	269.39	16.82	0.51	269.46	11.02	11.97
Inv-x4	100.0	20.0	81.36	16.72	0.51	87.39	24.44	12.55
Inv-x4	100.0	50.0	159.44	17.06	0.51	161.86	18.96	12.34
Inv-x4	100.0	100.0	291.94	18.38	0.52	292.97	17.58	12.26
Inv-x8	10.0	20.0	30.91	2.00	0.51	30.97	1.64	12.24
Inv-x8	10.0	50.0	71.15	3.76	0.51	71.11	2.88	12.16
Inv-x8	10.0	100.0	138.00	8.82	0.52	137.87	5.57	12.12
Inv-x8	100.0	20.0	56.95	16.70	0.50	66.75	27.52	12.47
Inv-x8	100.0	50.0	103.06	16.78	0.50	108.03	22.54	12.30
Inv-x8	100.0	100.0	173.05	17.23	0.52	175.32	18.08	12.22
Inv-x16	10.0	20.0	15.94	1.72	0.50	16.14	1.78	12.37
Inv-x16	10.0	50.0	35.84	1.99	0.51	35.91	1.82	12.13
Inv-x16	10.0	100.0	69.16	3.00	0.51	69.21	2.87	12.03
Inv-x16	100.0	20.0	34.59	16.82	0.49	48.02	30.24	12.86
Inv-x16	100.0	50.0	60.45	16.72	0.49	68.92	26.77	12.45
Inv-x16	100.0	100.0	94.19	16.75	0.50	99.20	23.09	12.30
Nand2-x8	10.0	20.0	29.16	1.84	0.50	29.25	1.70	12.62
Nand2-x8	10.0	50.0	69.14	2.96	0.51	69.19	2.87	12.18
Nand2-x8	10.0	100.0	135.85	6.46	0.55	135.93	5.52	12.13
Nand2-x8	100.0	20.0	51.36	16.62	0.49	60.64	27.47	12.49
Nand2-x8	100.0	50.0	93.60	16.65	0.50	98.45	22.97	12.30
Nand2-x8	100.0	100.0	159.07	16.89	0.52	161.42	18.90	12.22

We validate our proposed statistical gate delay calculation by comparing with 1000× Monte Carlo simulation via current source based gate models. Such current source based gate models have been verified to achieve within 4.6%(8.6%) gate delay mean (standard deviation) estimation with orders of maginitude of runtime speedup compared with SPICE simulation [4]. We base our experiments on a set of simple logic gates in Berkeley Predictive Technology Model of 70nm technology. We assume $0.1V_{dd}$ standard deviation for the gate input voltage, and no correlation for the gate input voltage at two different time spots. We take 10000 time steps before the gate output voltage reaches V_{dd} in transient analysis. Our experimental results in Table 1 show that our statistical gate delay calculation approximates Monte Carlo simulation results with an average of 4.1% (22.3%), and a maximum of 28.0% (58.3%) accuracy loss for the means (standard deviations) of gate delay with over 20× speedup.

5 Conclusion

We propose an efficient statistical gate level simulation method based on current source based gate models. We represent variational gate input voltage waveforms of any shape in time domain statistical variables, and perform time domain integration for variational gate output voltage waveforms, while taking into account process variations and input voltage waveform variations and their correlations. Our experimental results show that our method achieves over 20× efficiency improvement with an average of 4.1% (22.3) accuracy loss for the means (standard deviations) of gate delay compared with 1000× Monte Carlo simulation based on current based gate models.

Our statistical gate delay calculation method serves as one of the fundamental operations in statistical timing analysis, and faces some of the same challenges, e.g., computation of correlations. Techniques applied here may be leveraged in a larger extend of statistical timing analysis scenario. Our ongoing research effort includes consideration of an extensive set of variational process parameters and extension to more complex gate models.

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