Statistical Gate Level Simulation via Voltage Controlled Current Source Models

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Outline

- Background: Gate Modeling, SSTA
- Problem Formulation
- Statistical Gate Level Simulation: Method
- Experiments
- Conclusion
Traditional Gate Models

- **K-factor lookup tables**
  1. $D_g = f(C_{load}, T_r)$
  2. $T_{out} = g(C_{load}, T_r)$

- **Effective capacitance $C_{eff}$ for distributed load capacitance**
  - To achieve *identical gate delay* (and *output signal transition time* at the same time!)
  - E.g., by going through an iteration to achieve the same average gate output current

- May not converge
- No equivalent gate delay and Trout at the same time
- Waveforms are not ramp functions!
MOSFET is a voltage-controlled current source, e.g., as in the alpha-power-law model.

\[
Id_s = \begin{cases} 
0 & Vgs < Vt \\
\frac{W}{L_{eff}} \frac{P_c}{P_v} (Vgs - Vt)^{\alpha/2} & Vds < PV(Vgs - Vt)^\alpha \\
\frac{W}{L_{eff}} P_c(Vgs - Vt)^\alpha & Vds < PV(Vgs - Vt)^\alpha
\end{cases}
\]

For a simple inverter, gate output current is given by one of the transistors.

An equivalent inverter macro-model for an inverting complex gate.

→ current-based gate modeling
Current-Based Gate Modeling

- Consists of a lookup table $I(V_i, V_o)$ and $C(V_i, V_o)$

- Transient analysis for output signal waveform

Voltage-Based

Current-Based
Current Source Gate Model Based Transient Analysis

- **Input:** $V_i(t)$, $I(V_i, V_o)$, $C_g$, load interconnect
- **Output:** $V_o(t)$

1. *Reduce load interconnect, e.g., to a Pi model*
2. *For each time step $t$*
3. *Find $V_i(t)$ and $V_o(t)$*
4. *Find $I(V_i, V_o)$ by take lookup*
5. *Compute $V_o(t+1)$ with load interconnect*
VLSI Variability

- Increased variability in nanometer VLSI designs
  - Process:
    - OPC $\rightarrow$ Lgate
    - CMP $\rightarrow$ thickness
    - Doping $\rightarrow$ Vth
  - Environment:
    - Supply voltage $\rightarrow$ transistor performance
    - Temperature $\rightarrow$ carrier mobility $\mu$ and $V_{th}$

- These (PVT) variations result in circuit performance variation

![Diagram showing PVT parameter distributions and gate/net delay distribution](image)
Timing Analysis

- Min/Max-based
  - Inter-die variation
  - Pessimistic

- Corner-based
  - Intra-die variation
  - Computational expensive

- Statistical
  - pdf for delays
  - Reports timing yield
Represent signal arrival times as random variables

- **Block-based**
  - Each timing node has an arrival time distribution
  - Static worst case analysis
  - Efficient for circuit optimization

- **Path-based**
  - Each timing node *for each path* has an arrival time distribution
  - Corner-based or Monte Carlo analysis
  - Accurate for signoff analysis
Gate Level Statistical Simulation

- **SSTA** needs to take into account a number of effects:
  - Multiple input switching
  - Crosstalk aggressor alignment
  - Power/ground supply voltage degradation

- **Gate level statistical simulation** provides a new level of accuracy improvement opportunity

- Improved efficiency compared with **Monte Carlo SPICE simulation**
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Statistical Gate Level Simulation

- Given
  - Variational input $V_i(t)$
  - Current source gate model of $I(V_i, V_o)$, $C_g$
- Find variational output signal waveform $V_o(t)$
Variational Input Waveform

- A time domain statistical variable $V_i(t)$, for each time step $t$
  - Mean $\mu_{V_i(t)}$
  - Standard variation $\sigma_{V_i(t)}$
  - Skewness and other higher order moments
  - Covariances $\text{cov}_{V_i(t1), V_i(t2)}$
  - Higher order covariances
Stochastic Process

- Deterministic
  - Given an internal point, the rest of the process is predictable
  - In case that there is no process variation in the gate model of $I(V_i, V_o)$ and $C_g$, and there is only, e.g., delay or transition time variation for the input

- Our problem is an un-deterministic stochastic process
Output voltage \( V_o(t) \) is given by time domain integration of gate output current \( I(V_i, V_o) \)

\[
V_o(t) = \int_{0}^{t} \frac{I(t)}{C_L} dt
\]
Statistical Gate Current

- Gate current $I(V_i, V_o)$ is well approximated by a quadratic polynomial.
- We approximate $I(V_i, V_o)$ by a linear function for small variations.
- Input and output voltage variations give gate current variation.

$$I(t) = a_0 + a_1 V_i(t) + a_2 V_o(t)$$

$$\mu_{I(t)} = a_0 + a_1 \mu_{V_i(t)} + a_2 \mu_{V_o(t)}$$

$$\sigma_{I(t)}^2 = a_1^2 \sigma_{V_i(t)}^2 + a_2^2 \sigma_{V_o(t)}^2 + 2a_1 a_2 \text{cov}_{V_i(t), V_o(t)}$$
Gate current variation gives $\Delta V_o(t)$ variation

Accumulation of $\Delta V_o(t)$ gives output voltage $V_o(t)$

\[
\Delta V_o(t) = \frac{I(t)\Delta t}{C_L}
\]

\[
\mu_{\Delta V_o(t)} = \frac{\mu_{I(t)}\Delta t}{C_L}
\]

\[
\sigma_{\Delta V_o(t)} = \frac{\sigma_{I(t)}\Delta t}{C_L}
\]

\[
\mu_{\Delta V_o(t+\Delta t)} = \mu_{V_o(t)} + \mu_{\Delta V_o(t)}
\]

\[
\sigma^2_{\Delta V_o(t+\Delta t)} = \sigma^2_{V_o(t)} + \sigma^2_{\Delta V_o(t)} + 2\text{cov}_{V_o(t),\Delta V_o(t)}
\]
**Statistical Gate Delay**

- Given mean $\mu_{V_0(t)}$ and standard deviation $\sigma_{V_0(t)}$ of output voltage $V_0(t)$, assuming $V_0(t)$ in a Gaussian distribution, the probability for $V_0(t)$ to reach $0.5V_{dd}$ is:

\[
Pr(V_0(t) > 0.5V_{dd}) = 1 - cdf(V_0(t)) = 0.5(1 - erf\left(\frac{0.5V_{dd} - \mu_{V_0(t)}}{\sqrt{2}\sigma_{V_0(t)}}\right))
\]

- Probability for $V_0(t) = 0.5V_{dd}$ for the first time at $t$:

\[
Pr(t_d = t) = Pr(V_0(t) > 0.5V_{dd}) - Pr(V_0(t - \Delta t) > 0.5V_{dd})
\]

- Gate delay prob:

\[
D_g = t_d - t_0 \\
\mu_{D_g} = \mu_{t_d} - \mu_{t_0} \\
\sigma_{D_g} = \sigma_{t_d} - \sigma_{t_0}
\]
**Statistical Gate Level Simulation**

- **Input**: Variational input $V_i(t)$,
  
  gate model $I(V_i, V_o)$, $C_g$, load interconnect

- **Output**: $V_o(t)$

<table>
<thead>
<tr>
<th>1. For each time step</th>
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<tbody>
<tr>
<td>2. Compute gate current variation</td>
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<td>3. Compute gate output voltage variation</td>
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<td>4. Compute gate delay variation</td>
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Experiments

- BPTM 70nm technology cell library
- Single load capacitance
- $\sigma_{V_i(t)} = 0.1$ V
- No correlation
- No process variation in the gate model
- 10,000 time steps in transient analysis
- Compare statistical computation with 1000 X Monte Carlo SPICE simulation
Our method gives an average of 4.1%(22.3%) and a maximum of 28.0%(58.3%) inaccuracy for mean (standard deviation) estimate of gate delay with over 20X speedup compared with Monte Carlo SPICE simulation.

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<th>Inv-x4</th>
<th>Our Method</th>
<th>Monte Carlo SPICE</th>
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<tr>
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<td>( T_r )</td>
<td>( C )</td>
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<td>10.0</td>
<td>20.0</td>
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<td>( T_r )</td>
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Summary

- **Gate level statistical simulation** is much needed to bridge
  - Monte Carlo SPICE simulation and
  - circuit level statistical timing analysis

for a new level of accuracy-efficiency tradeoff

- We present a moments and correlations based time domain statistical computation method based on current source gate models
Ongoing Research

- Extensions
  - More effective Input waveform representation
  - More process variations in the gate model
  - Correlation consideration

- Accuracy improvement
  - Is the moments and correlations based statistical computation the right choice?
  - Or is Monte Carlo simulation the ultimate effective method for statistical simulation?
Thank you!
Applications

- More accuracy, arbitrary waveform
- Efficiency advantage over SPICE simulation
- Gate delay calculation for
  - Long interconnects
  - Cross-coupling interconnects
  - Supply voltage drop effect
- Supply current calculation
- Noise calculation
Supply Voltage Variation Effect on Gate Delay Calculation

- There exists an equivalent inverter macro-model for each input combination for any (inverting) complex gate.
- Adjust input and output voltages for \( I(V_i, V_o) \) table lookup for a falling input signal, but not for a rising input signal.

\[
I' = I(V'_i, V'_o) \\
V'_i = V_i + \Delta V \\
V'_o = V_o + \Delta V
\]
Polynomial Regression of $I(V_i, V_o)$

- **A priori** knowledge:
- Approximate $I(V_i, V_o)$ by a quadratic polynomial
- 9+1 coefficients in a limited range
Polynomial Regression of $I(V_i, V_o)$

$$I(V_i, V_o) = a_{00} + a_{01} V_o + a_{02} V_o^2$$
$$+ a_{10} V_i + a_{11} V_i V_o + a_{12} V_i V_o^2$$
$$+ a_{20} V_i^2 + a_{21} V_i^2 V_o + a_{22} V_i^2 V_o^2$$

$I(0,0) > 0$
$I(0,1) = 0$
$I(1,0) = 0$
$I(1,1) < 0$
$$\frac{\partial}{\partial V_i} I(V_i, V_o) < 0$$
$$\frac{\partial}{\partial V_o} I(V_i, V_o) < 0$$

$a_{00}, a_{20} > 0$
$a_{01}, a_{02}, a_{10} < 0$
$a_{00} + a_{01} + a_{02} = 0$
$a_{00} + a_{10} + a_{20} = 0$
$a_{01} + a_{11} + a_{21} < 0$
$a_{10} + a_{11} + a_{12} < 0$