Statistical Gate Level Simulation via Voltage Controlled Current Source Models

Bao Liu and Andrew Kahng

UC San Diego

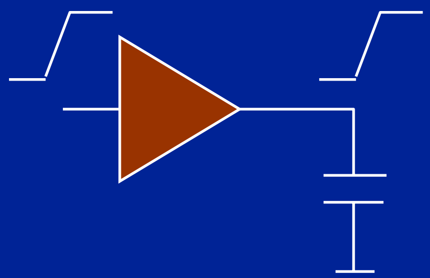
http://vlsicad.ucsd.edu/~bliu

Outline

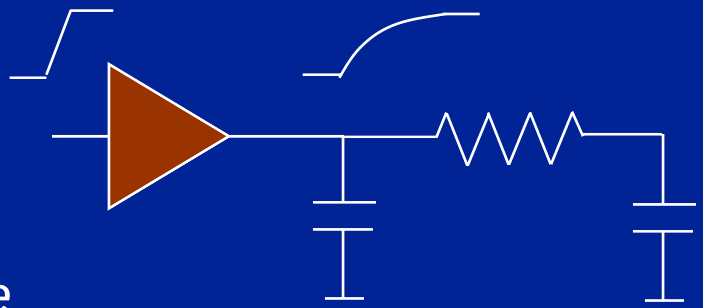
- Background: Gate Modeling, SSTA
- Problem Formulation
- Statistical Gate Level Simulation: Method
- Experiments
- Conclusion

Traditional Gate Models

- K-factor lookup tables
  1. *Dg = f(Cload, Tr)*
  2. *Tr_{out} = g(Cload, Tr)*



- *Effective capacitance Ceff* for *distributed load capacitance*
  - To achieve *identical gate delay* (and *output signal transition time* at the same time!)
  - E.g., by going through an iteration to achieve the same average gate output current

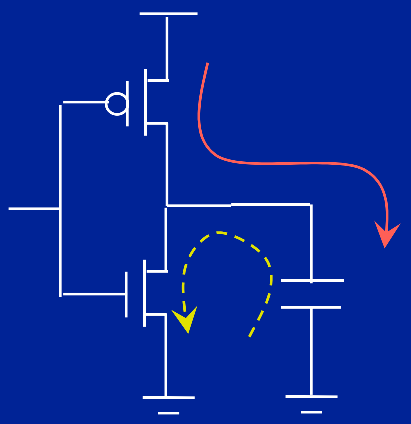


- ✓ May not converge
- ✓ No equivalent gate delay and Trout at the same time
- ✓ Waveforms are not ramp functions!

Current-Based Transistor Model

- MOSFET is a voltage-controlled current source, e.g., as in the alpha-power-law model

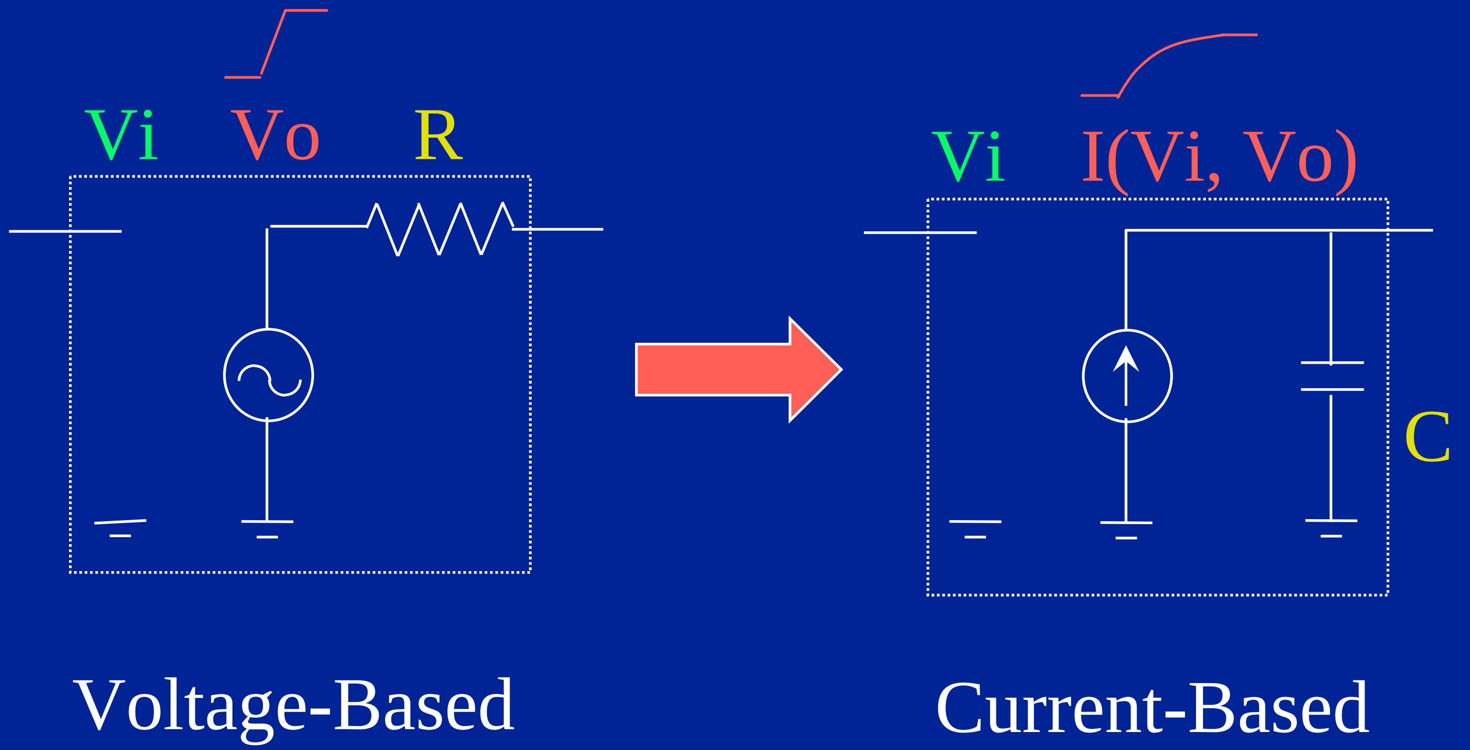
$$Ids = \begin{cases} 0 & Vgs < Vt \\ \dfrac{W}{Leff}\dfrac{Pc}{Pv}(Vgs - Vt)^{\alpha/2} & Vds < Pv(Vgs - Vt)^{\alpha} \\ \dfrac{W}{Leff}Pc(Vgs - Vt)^{\alpha} & Vds < Pv(Vgs - Vt)^{\alpha} \end{cases}$$



- For a simple inverter, gate output current is given by one of the transistors
- An equivalent inverter macro-model for an inverting complex gate
- → current-based gate modeling

Current-Based Gate Modeling

- Consists of a lookup table I(Vi, Vo) and C(Vi, Vo)

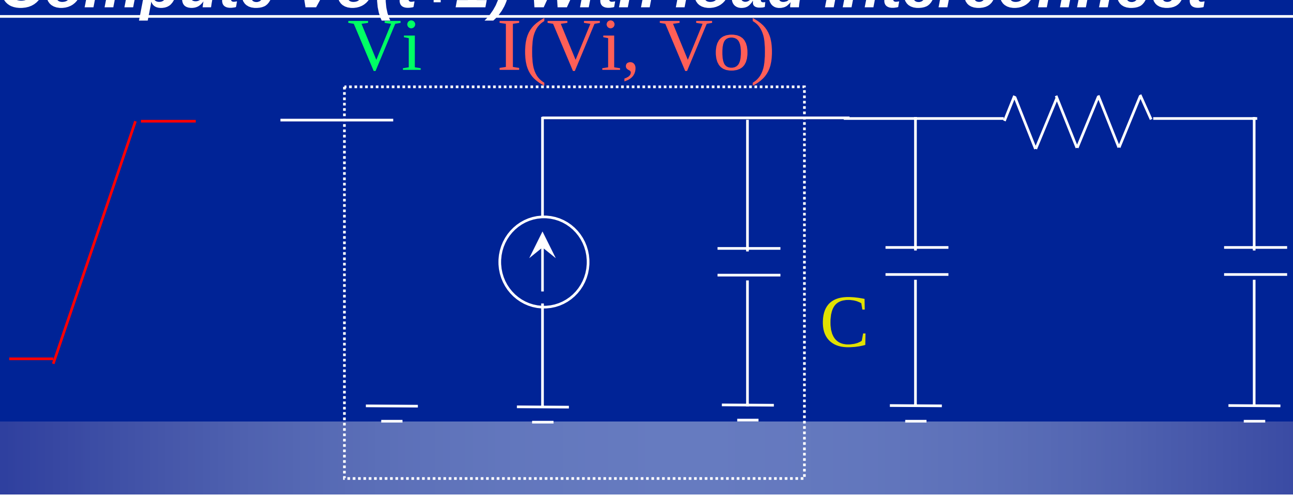


- Transient analysis for output signal waveform

Current Source Gate Model Based Transient Analysis

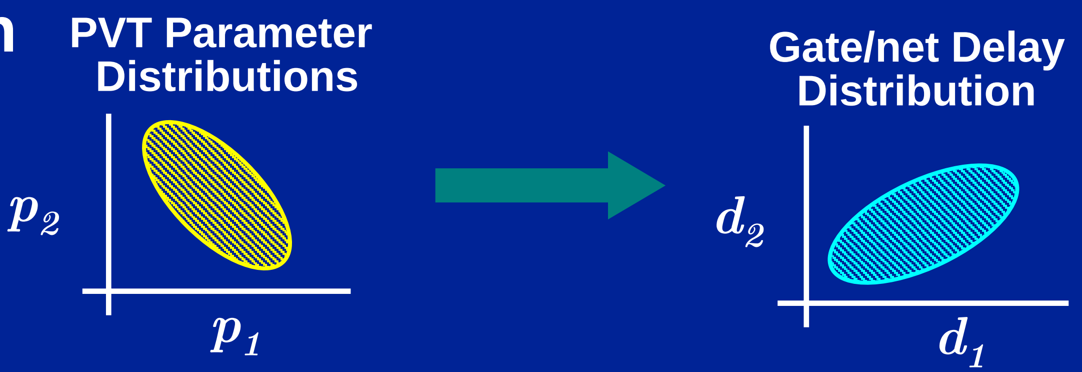
- *Input: Vi(t), I(Vi, Vo), Cg, load interconnect*
- *Output: Vo(t)*

1. *Reduce load interconnect, e.g., to a Pi model*
2. *For each time step t*
3. *Find Vi(t) and Vo(t)*
4. *Find I(Vi, Vo) by take lookup*
5. *Compute Vo(t+1) with load interconnect*



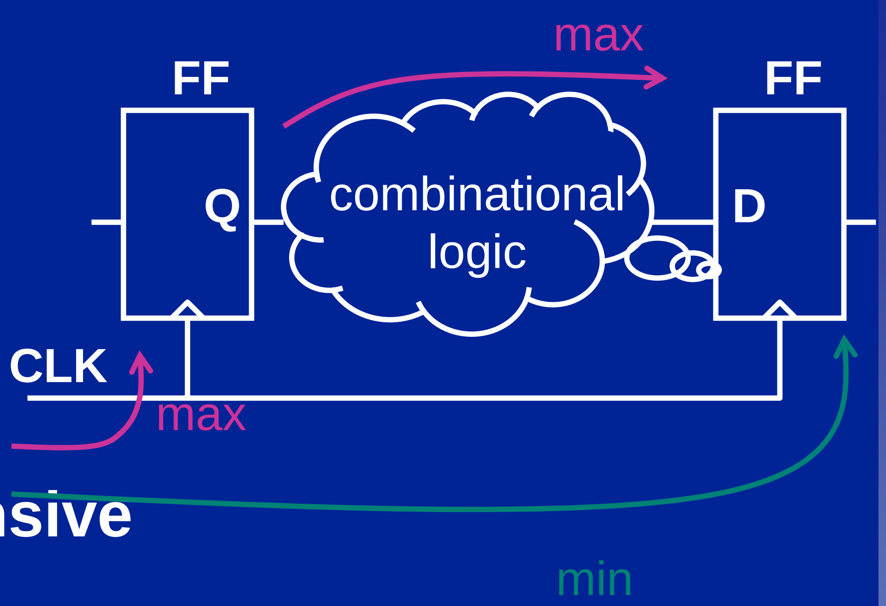
VLSI Variability

- Increased variability in nanometer VLSI designs
  - Process:
    - OPC → Lgate
    - CMP → thickness
    - Doping → Vth
  - Environment:
    - Supply voltage → transistor performance
    - Temperature → carrier mobility μ and Vth
- These (PVT) variations result in circuit performance variation



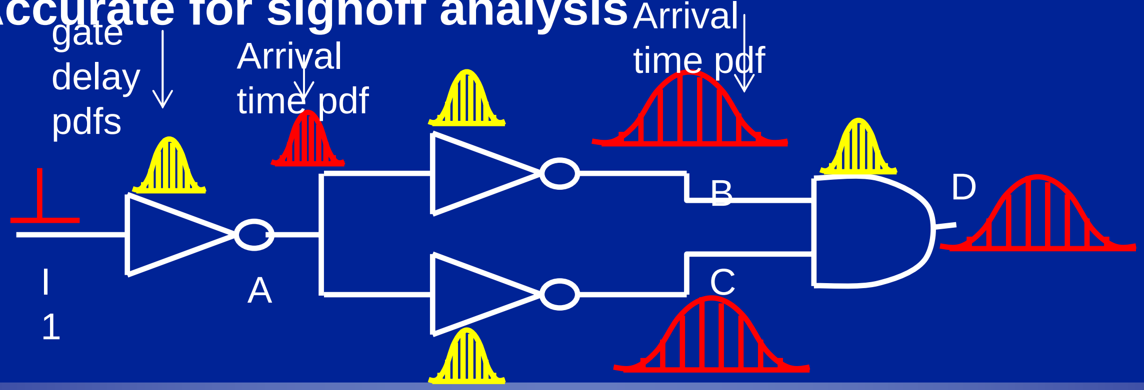
Timing Analysis

- Min/Max-based
  - Inter-die variation
  - Pessimistic
- Corner-based
  - Intra-die variation
  - Computational expensive
- Statistical
  - pdf for delays
  - Reports timing yield



SSTA

- **Represent signal arrival times as random variables**
  - **Block-based**
    - **Each timing node has an arrival time distribution**
    - **Static worst case analysis**
    - **Efficient for circuit optimization**
  - **Path-based**
    - **Each timing node *for each path* has an arrival time distribution**
    - **Corner-based or Monte Carlo analysis**
    - **Accurate for signoff analysis**



Gate Level Statistical Simulation

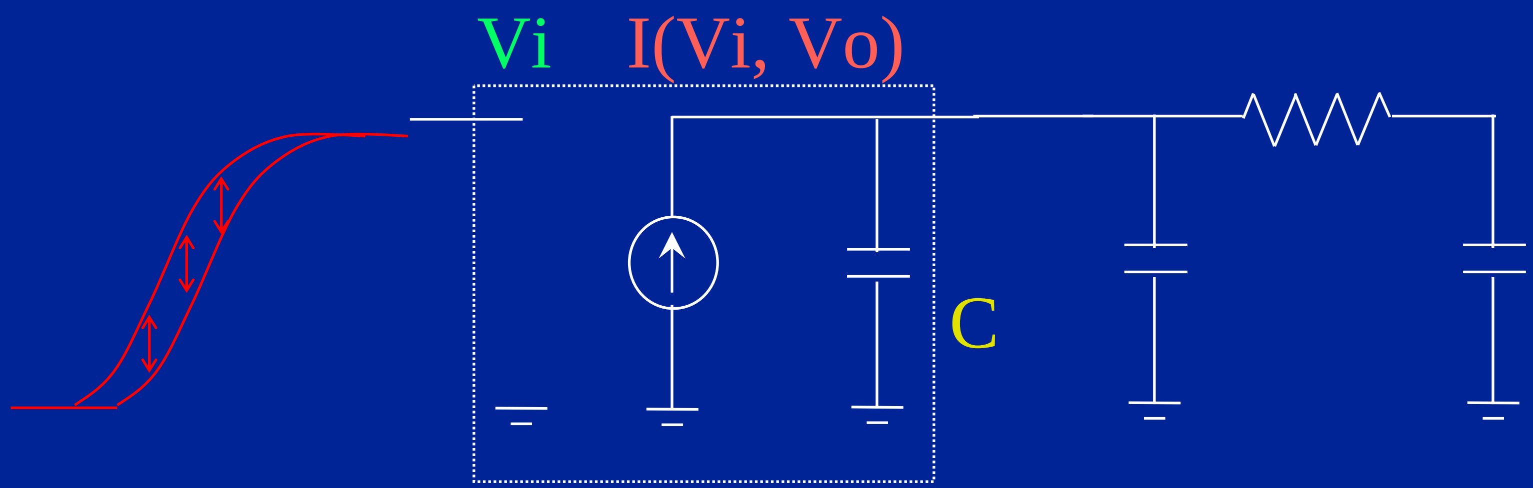
- SSTA needs to take into account a number of effects:
  - Multiple input switching
  - Crosstalk aggressor alignment
  - Power/ground supply voltage degradation
- Gate level statistical simulation provides a new level of accuracy improvement opportunity
- Improved efficiency compared with Monte Carlo SPICE simulation

Outline

- Background: Gate Modeling, SSTA
- Problem Formulation
- Statistical Gate Level Simulation: Method
- Experiments
- Conclusion

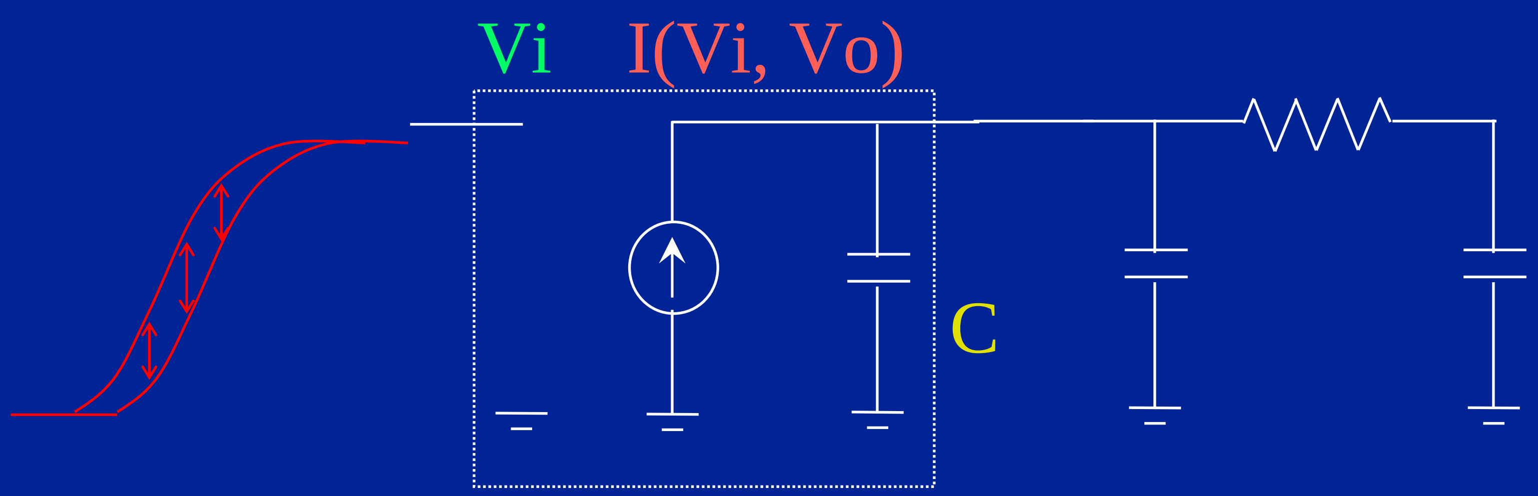
Statistical Gate Level Simulation

- Given
  - Variational input Vi(t)
  - Current source gate model of I(Vi, Vo), Cg
- Find variational output signal waveform Vo(t)



Variational Input Waveform

- A time domain statistical variable Vi(t), for each time step t
  - Mean $\mu_{Vi(t)}$
  - Standard variation $\sigma_{Vi(t)}$
  - Skewness and other higher order moments
  - Covariances $cov_{Vi(t1), Vi(t2)}$
  - Higher order covariances



Stochastic Process

- Deterministic
  - Given an internal point, the rest of the process is predictable
  - In case that there is no process variation in the gate model of I(Vi, Vo) and Cg, and there is only, e.g., delay or transition time variation for the input
- Our problem is an un-deterministic stochastic process

Statistical Time Domain Integration

- Output voltage Vo(t) is given by time domain integration of gate output current I(Vi, Vo)

$$V_o(t) = \int_0^t \frac{I(t)}{C_L} dt$$

Statistical Gate Current

- Gate current I(Vi,Vo) is well approximated by a quadratic polynomial
- We approximate I(Vi, Vo) by a linear function for small variations
- Input and output voltage variations give gate current variation

$$I(t) = a_0 + a_1 V_i(t) + a_2 V_o(t)$$

$$\mu_{I(t)} = a_0 + a_1 \mu_{Vi(t)} + a_2 \mu_{Vo(t)}$$

$$\sigma_{I(t)}{}^2 = a_1{}^2 \sigma_{Vi(t)}{}^2 + a_2{}^2 \sigma_{Vo(t)}{}^2 + 2a_1 a_2 \operatorname{cov}_{Vi(t),Vo(t)}$$

Statistical Gate Output Voltage

- Gate current variation gives ΔVo(t) variation
- Accumulation of ΔVo(t) gives output voltage Vo(t)

$$\Delta V_o(t) = \frac{I(t)\Delta t}{C_L}$$

$$\mu_{\Delta V_o(t)} = \frac{\mu_{I(t)}\Delta t}{C_L}$$

$$\sigma_{\Delta V_o(t)} = \frac{\sigma_{I(t)}\Delta t}{C_L}$$

$$\mu_{\Delta V_o(t+\Delta t)} = \mu_{V_o(t)} + \mu_{\Delta V_o(t)}$$

$$\sigma^2{}_{\Delta V_o(t+\Delta t)} = \sigma^2{}_{V_o(t)} + \sigma^2{}_{\Delta V_o(t)} + 2\,\mathrm{cov}_{V_o(t),\Delta V_o(t)}$$

Statistical Gate Delay

- Given mean $\mu_{Vo(t)}$ and standard deviation $\sigma_{Vo(t)}$ of output voltage $V_o(t)$, assuming $V_o(t)$ in a Gaussian distribution, the probability for $V_o(t)$ to reach $0.5V_{dd}$

$$\Pr(Vo(t) > 0.5Vdd) = 1 - cdf(Vo(t)) = 0.5(1 - erf(\frac{0.5Vdd - \mu_{Vo(t)}}{\sqrt{2}\sigma_{Vo(t)}}))$$

- Probability for Vo(t) = 0.5Vdd for the first time at t

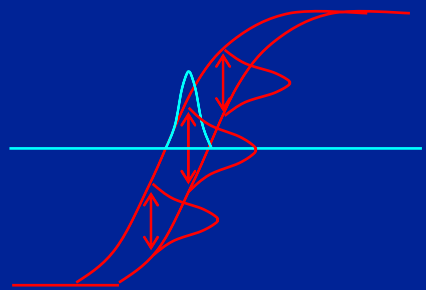
$$\Pr(t_d = t) = \Pr(Vo(t) > 0.5Vdd) - \Pr(Vo(t - \Delta t) > 0.5Vdd)$$

- Gate delay prob

$$D_g = t_d - t_0$$

$$\mu_{D_g} = \mu_{t_d} - \mu_{t_0}$$

$$\sigma_{D_g} = \sigma_{t_d} - \sigma_{t_0}$$



Statistical Gate Level Simulation

- *Input: Variational input Vi(t),*

  gate model I(Vi, Vo), Cg, load interconnect
- *Output: Vo(t)*

1. *For each time step*
2. *Compute gate current variation*
3. *Compute gate output voltage variation*
4. *Compute gate delay variation*

Outline

- Background: Gate Modeling, SSTA
- Problem Formulation
- Statistical Gate Level Simulation: Method
- Experiments
- Conclusion

Experiments

- BPTM 70nm technology cell library
- Single load capacitance
- $\sigma_{Vi(t)} = 0.1$ V
- No correlation
- No process variation in the gate model
- 10,000 time steps in transient analysis
- Compare statistical computation with 1000 X Monte Carlo SPICE simulation

Experiments

- **Our method gives an average of 4.1%(22.3%) and a maximum of 28.0%(58.3%) inaccuracy for mean (standard deviation) estimate of gate delay with over 20X speedup compared with Monte Carlo SPICE simulation**

Inv-x4		*Our Method*			*Monte Carlo SPICE*		
T_r	*C*	μ_{Dg}	σ_{Dg}	*CPU*	μ_{Dg}	σ_{Dg}	*CPU*
10.0	*20.0*	*55.8*	*2.5*	*0.5*	*55.9*	*2.4*	*12.1*
10.0	*50.0*	*135.8*	*6.5*	*0.5*	*135.9*	*5.5*	*12.0*
10.0	*100.0*	*269.4*	*16.8*	*0.5*	*269.5*	*11.0*	*11.9*
Nand2-x8		*Our Method*			*Monte Carlo SPICE*		
T_r	*C*	μ_{Dg}	σ_{Dg}	*CPU*	μ_{Dg}	σ_{Dg}	*CPU*
100.0	*20.0*	*51.4*	*16.6*	*0.5*	*60.6*	*27.5*	*12.5*
100.0	*50.0*	*93.6*	*16.5*	*0.5*	*98.4*	*23.0*	*12.3*
100.0	*100.0*	*159.1*	*16.9*	*0.5*	*161.4*	*18.9*	*12.2*

Summary

- Gate level statistical simulation is much needed to bridge
  - Monte Carlo SPICE simulation and
  - circuit level statistical timing analysis

  for a new level of accuracy-efficiency tradeoff
- We present a moments and correlations based time domain statistical computation method based on current source gate models

Ongoing Research

- **Extensions**
  - **More effective Input waveform representation**
  - **More process variations in the gate model**
  - **Correlation consideration**
- **Accuracy improvement**
  - **Is the moments and correlations based statistical computation the right choice?**
  - **Or is Monte Carlo simulation the ultimate effective method for statistical simulation?**

Thank you !

Applications

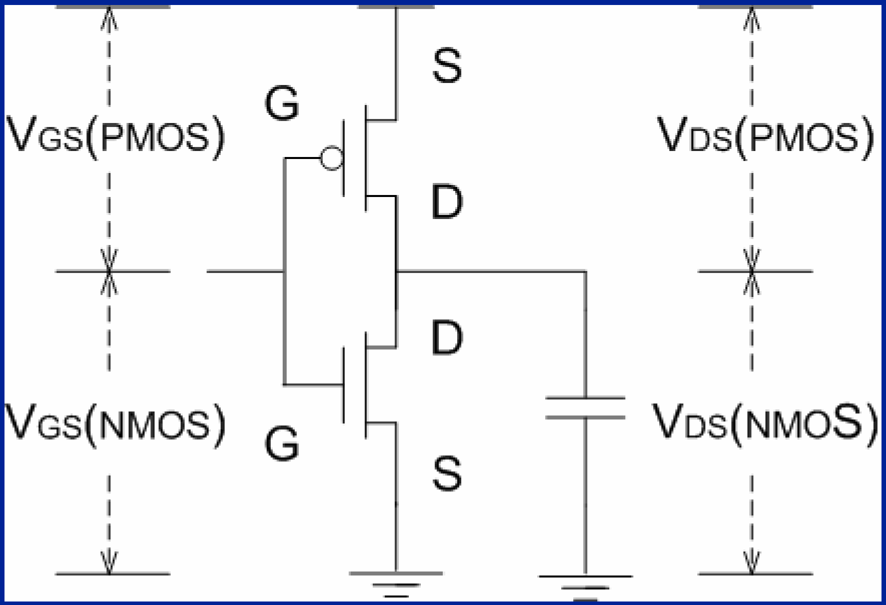
- More accuracy, arbitrary waveform
- Efficiency advantage over SPICE simulation
- Gate delay calculation for
  - Long interconnects
  - Cross-coupling interconnects
  - Supply voltage drop effect
- Supply current calculation
- Noise calculation

Supply Voltage Variation Effect on Gate Delay Calculation

$$I' = I(V_i', V_o')$$

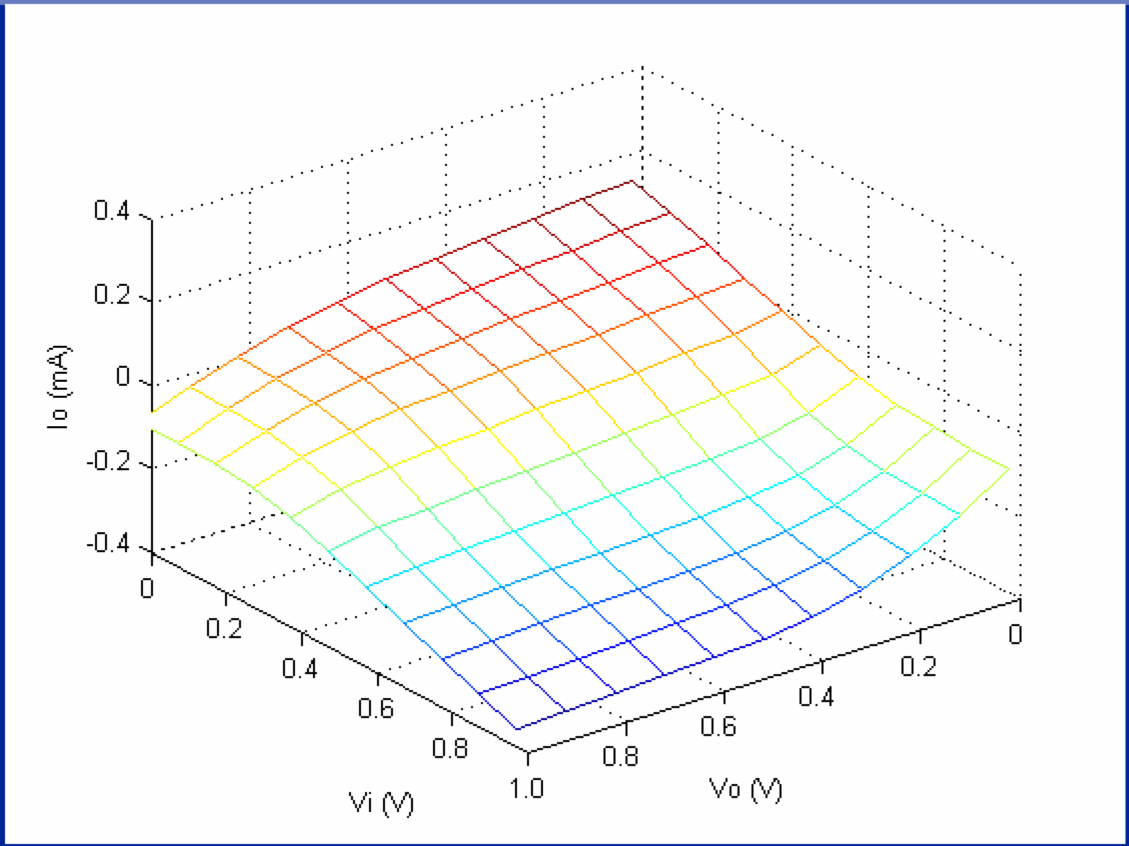
$$V_i' = V_i + \Delta V$$

$$V_o' = V_o + \Delta V$$



- **There exists an equivalent inverter macro-model for each input combination for any (inverting) complex gate**
- **Adjust input and output voltages for I(Vi, Vo) table lookup for a falling input signal, but not for a rising input signal**

Polynomial Regression of I(Vi,Vo)



- *A priori* knowledge:
- Approximate I(Vi, Vo) by a quadratic polynomial
- 9+1 coefficients in a limited range

Polynomial Regression of I(Vi,Vo)

$$I(V_i,V_o) = a_{00} + a_{01}V_o + a_{02}V_o^{\,2}$$
$$+ a_{10}V_i + a_{11}V_iV_o + a_{12}V_iV_o^{\,2}$$
$$+ a_{20}V_i^{\,2} + a_{21}V_i^{\,2}V_o + a_{22}V_i^{\,2}V_o^{\,2}$$

$I(0,0)$	$>$	0
$I(0,1)$	$=$	0
$I(1,0)$	$=$	0
$I(1,1)$	$<$	0
$\frac{\partial}{\partial Vi} I(V_i,V_o)$	$<$	0
$\frac{\partial}{\partial Vo} I(V_i,V_o)$	$<$	0

$\Rightarrow$

a_{00}, a_{20}	$>$	0
a_{01}, a_{02}, a_{10}	$<$	0
$a_{00} + a_{01} + a_{02}$	$=$	0
$a_{00} + a_{10} + a_{20}$	$=$	0
$a_{01} + a_{11} + a_{21}$	$<$	0
$a_{10} + a_{11} + a_{12}$	$<$	0