A New Approach for Modeling the Non linearity of Analog to Digital Converters Based on Spectral Components

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ABSTRACT

"*The non-linearity of an ADC is modeled using a linear combination of Chebyshev polynomials. A Fast Fourier Transform (FFT) processes the output of the ADC. The harmonics extracted render the coefficients of the Chebyshev polynomials*."

Outline

- Introduction
- ADC Terminology
- ADC Modeling Approaches
- Proposed Technique
  - Chebyshev Test
  - Modeling the INL
  - Model Implementation
- Simulation Results
- Conclusion
- Future Work

Introduction

- The focus of this work is to present a new efficient modeling technique for high resolution analog to digital converters.
- An accurate model of an ADC should imitate the real circuit showing the deviation of the real device from an ideal response.
- Our main focus was to model the non linearity of the converter.

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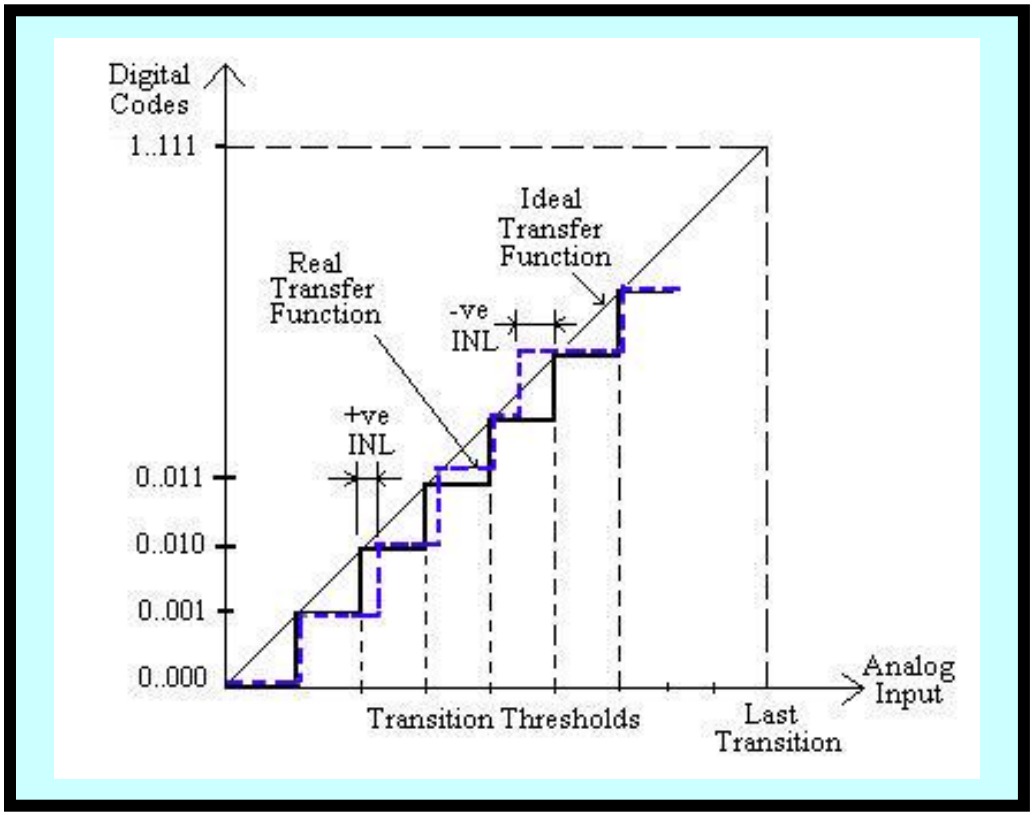
ADC Terminology

- One basic term in the world of converters whether ADCs or DACs is the INL.
- INL: Integral Non Linearity
- It is deviation of the actual transfer function of the ADC from the ideal straight line.
- INL represents the nonlinearity of the ADC.
- The transition thresholds show the different input analog ranges that give different digital codes.



ADC Terminology

- Another well known term is the “Quantization”
- This quantization is due to the approximation or “rounding“ effect in the converters.
- The quantization error is the difference between the original input and the digitized output.

$$Q = \text{Input Full scale}/2^N$$

$$\text{Quantization Noise Power} = Q^2/12$$

Input full scale: is the maximum applicable voltage to the ADC input.

N:ADC resolution in bits.

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ADC Modeling Approaches

- **Structural Modeling:**

  Building blocks of the converter are modeled separately. Each individual block contributes to the overall non ideality of the converter.

  Close to real circuits but can be very slow in case of high resolution bits.

- **Example:**

  Flash ADCs ,Pipelined ADCs,……

ADC Modeling Approaches

- **Modeling the ADC as a transfer function:**
  - **To model the imperfections, some of these models need thousands of parameters for high resolution bits.**
  - **Other models generate a random error based on a maximum given by the user. These models are computationally extensive and sometimes do not reflect a proper level of accuracy.**

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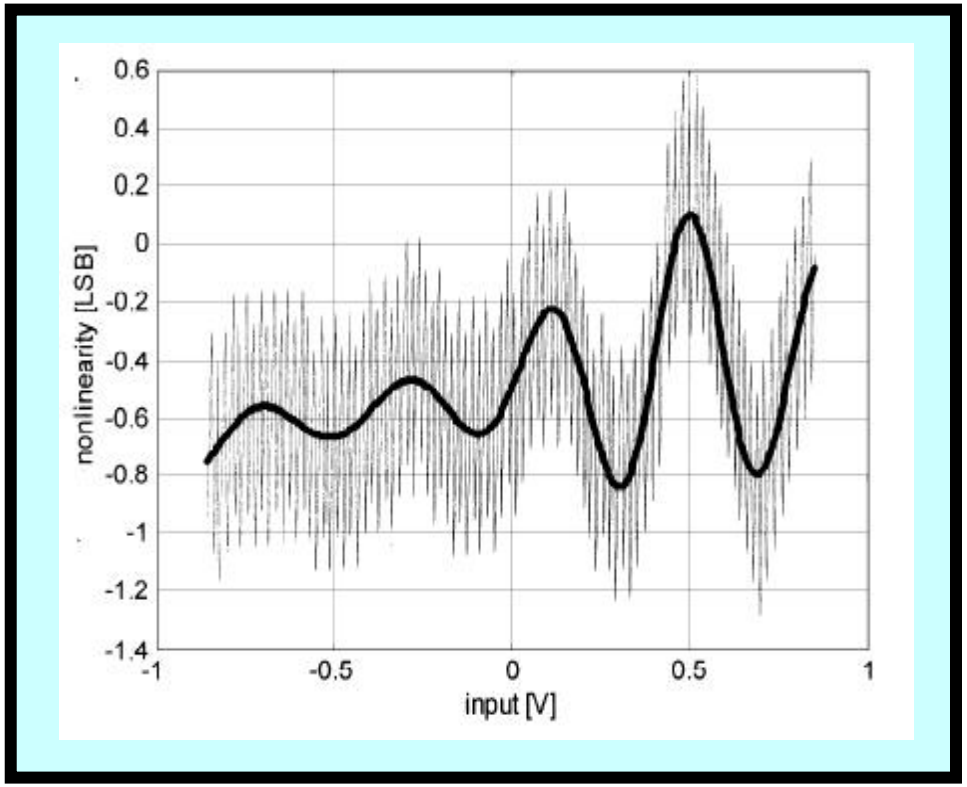
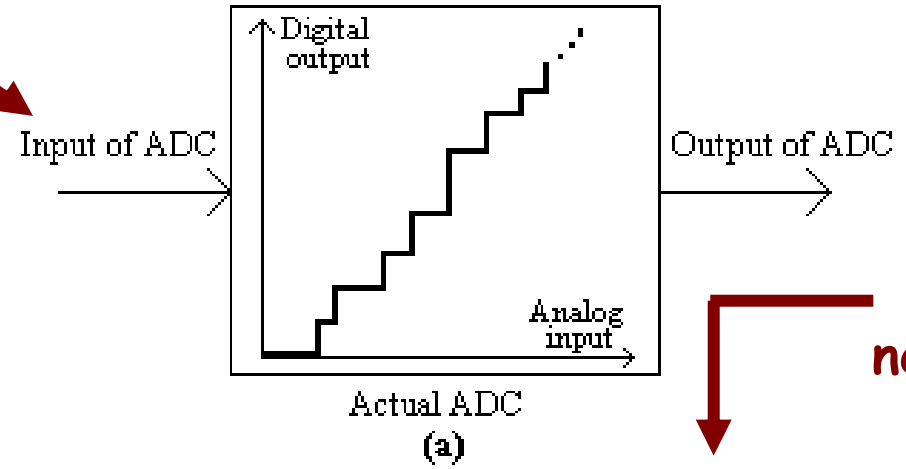
Proposed Technique

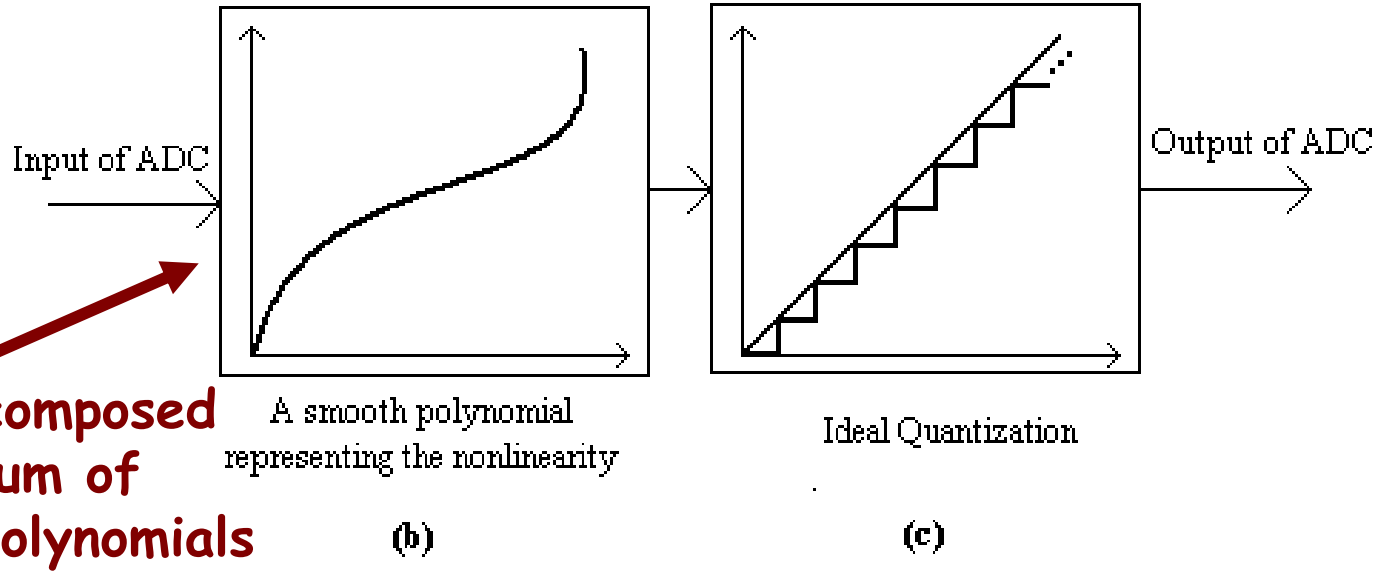
- The proposed technique models the converter as a whole but formulating the INL as a polynomial.
- The technique relies on the theory of the “Chebyshev test” for generating a polynomial describing the average of the non linearity of a given ADC.
- The converter is divided into two blocks:
  - A smooth polynomial representing the converter’s non linearity.
  - An ideal quantizer.



To write the function of this ADC, you need a very large number of terms



The effect of quantization is neglected for high resolution bits



This is decomposed into a sum of Chebyshev polynomials

"Chebyshev Test" Theory

- **Consider the static transfer function:**

$$y = f(x)$$

when stimulated with a sinusoidal signal:

$$x(t) = A\cos(wt) + C$$

will result in a periodic output in the form:

$$y(t) = a_0/2 + \Sigma\, a_n\cos(nwt) + e(t)$$

e(t): this term accounts for all random errors such as noise.

"Chebyshev Test" Theory

- **If the transfer function is a polynomial, then f(x) can be expanded in a sum of Chebyshev polynomials as follows:**

$$f(x)= a_0 / 2 + \sum a_n C_n(\text{'x-}C\text{'} / A)$$

- **From the approximation of dividing the transfer into a polynomial and an ideal quantizer, we can describe the smooth polynomial as:**

$$g(x)= a_0 / 2 + \sum a_n C_n(\text{'x-}C\text{'} / A)$$

where,

$$C_n(\cos\theta)=\cos(n\theta)$$

$C_n()$: Chebyshev polynomial of the first type.

“Chebyshev Test” Theory

- **For the dynamic response:**

$$y(t) = a_0/2 + \Sigma\, a_n \cos(n\omega t) + \Sigma\, b_n \sin(n\omega t) + e(t)$$

- **The converter transfer function will be divided into two functions describing the ADC response to rising and falling values of the sinusoidal:**

$$g_1(x) = g(X) + h(x)$$

$$g_2(x) = g(X) - h(x)$$

where, g(x) is the average characteristics and h(x) is the deviation from the average.

Modeling the INL

- Now we know that g(x) is the polynomial that describes the non linearity of the ADC.
- Coefficients of the equation (a_n) can be evaluated using a FFT test applied to the output of the ADC.
- The FFT test determines the frequency content of a signal.

Modeling the INL

- The FFT output consists of:
  - A noise floor: formed from the quantization noise. This is usually small for high values of resolution bits.
  - Significant harmonics: these are due to the INL and other converter impairments.
- FFT procedure:
  - Apply a sinusoidal to the converter input. This input signal has to span the full scale.
  - Apply an FFT to the stair cased sinusoidal output of the converter.
  - Extract the first few harmonics (magnitude and phase)

Model Implementation

- Using Verilog-AMS.
- Used for bottom-up verification of ADCs.
- Models offset error, gain error, INL.
- Model Parameters:
  - N: Resolution bits
  - Td: Conversion time
  - Reference voltages
  - Offset error
  - Gain error
  - Harmonics (Magnitude and Phase)

```
module adc(in,out,clk)
  parameter integer N=16 from [12:24];
  parameter real refminus=-5;
  parameter real refplus=5;
            …
  parameter h0=90.30886;
  parameter h1=90.309;
            …
initial
begin
  fullscale=refplus-refminus;
  LSB=fullscale/pow(2,N);
  a0=pow(10,(h0/20));
            …
end
always @ (posedge clk)
begin
  inl=…….;
end
endmodule
```

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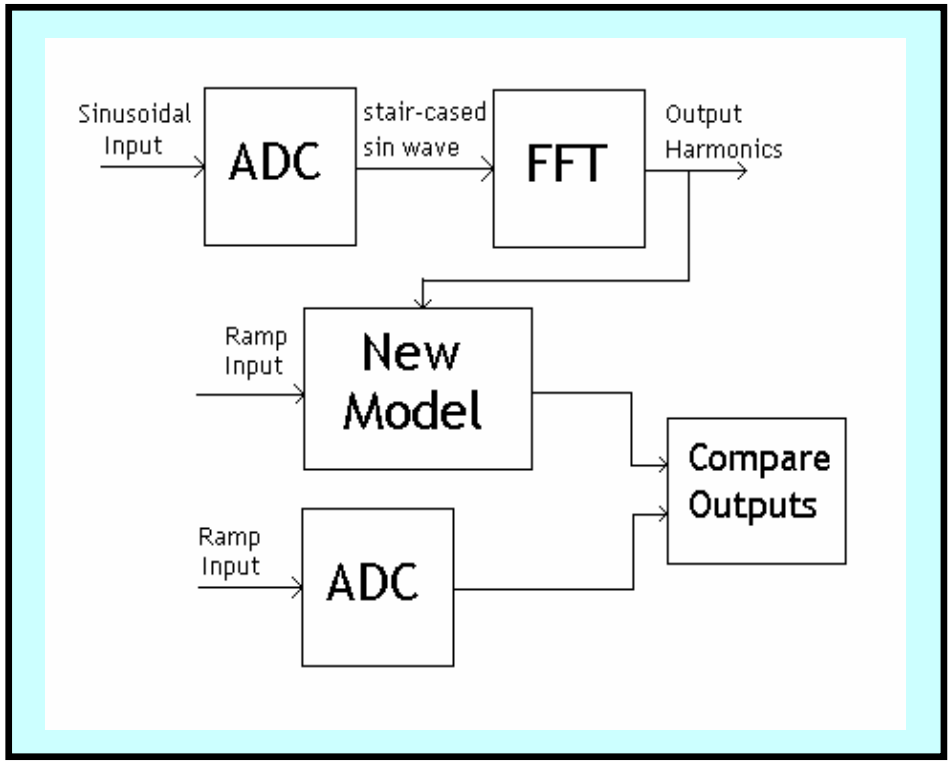
Simulation Results

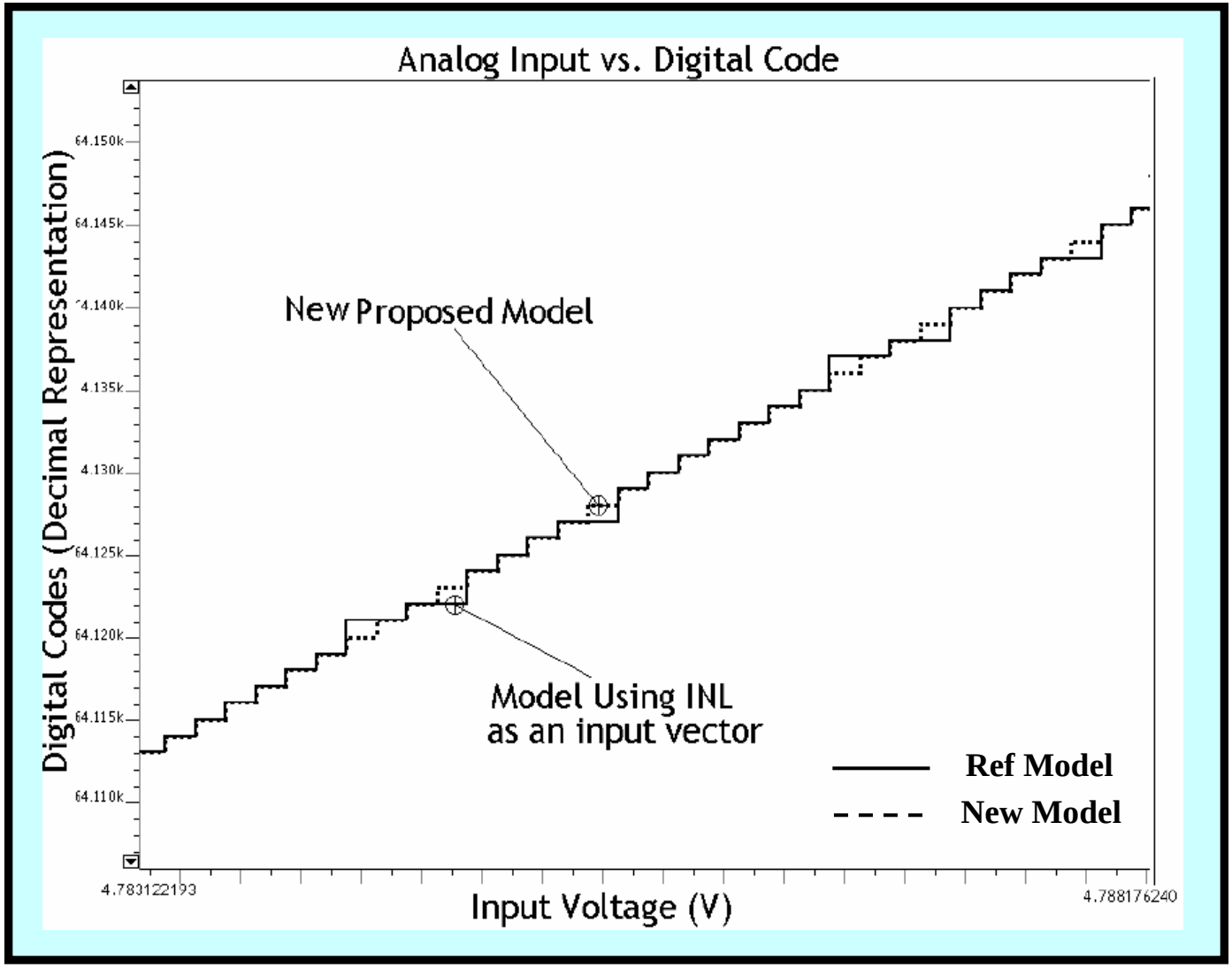
- Simulations performed using Mentor Graphics, mixed-signal simulator, ADVance MS™
- Procedure and Setup:
  - Apply a sin wave to the input of the ADC.
  - Output is passed to an FFT processor.
  - Output harmonics inserted in the model.
  - Slow ramp inputs are applied to the model and the ADC to ensure covering all codes.
  - Transfer functions are compared.



Simulation Results

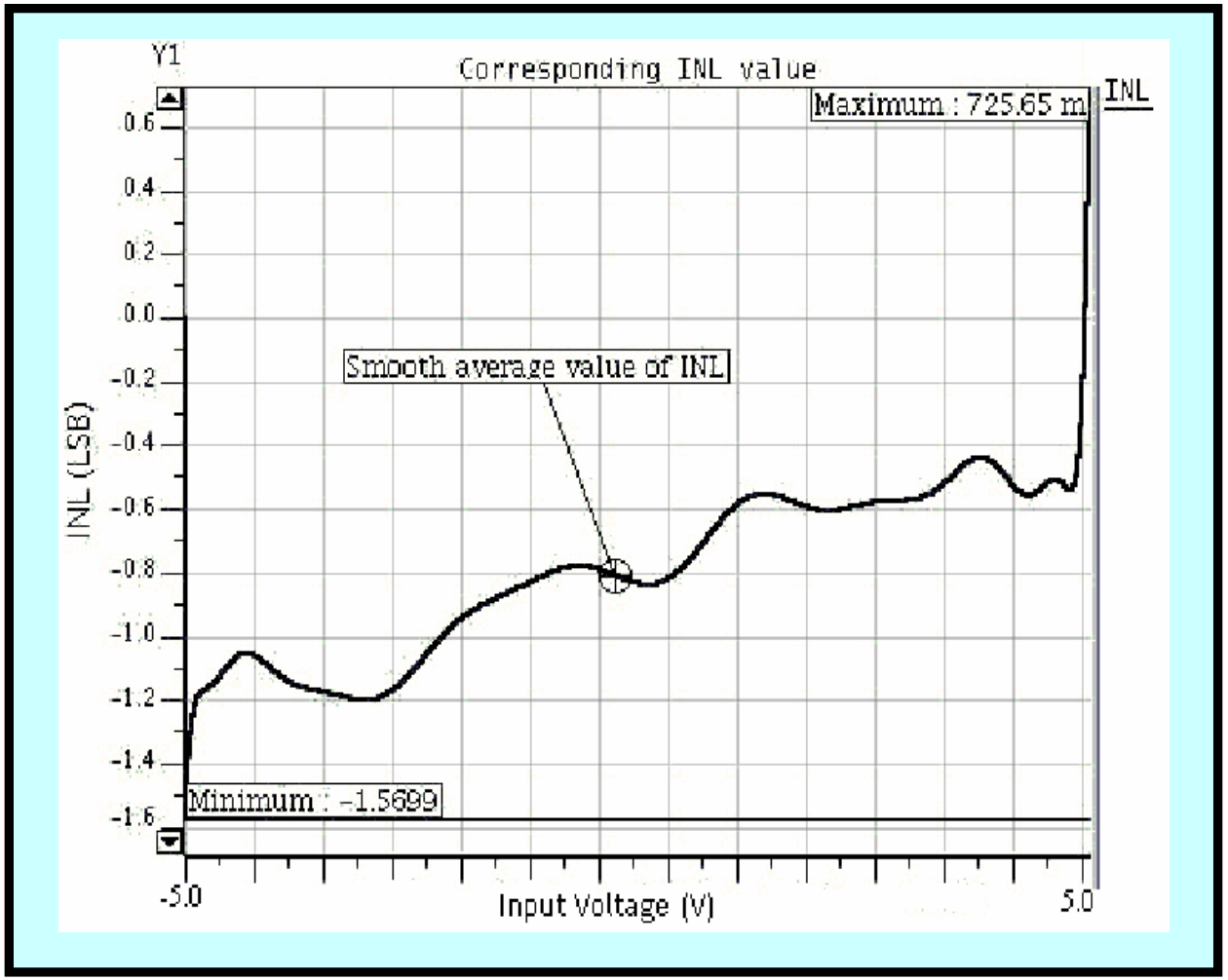
- ADC reference used in the following example is a model for a 16-bit ADC.
- The reference model used 65,535 parameters to describe the INL at every transitional threshold. Reference voltages +5V and –5V and ADC CLK=1Mhz.
- The new model used 8 harmonics and the same reference voltages and clock speed.

Simulation Results



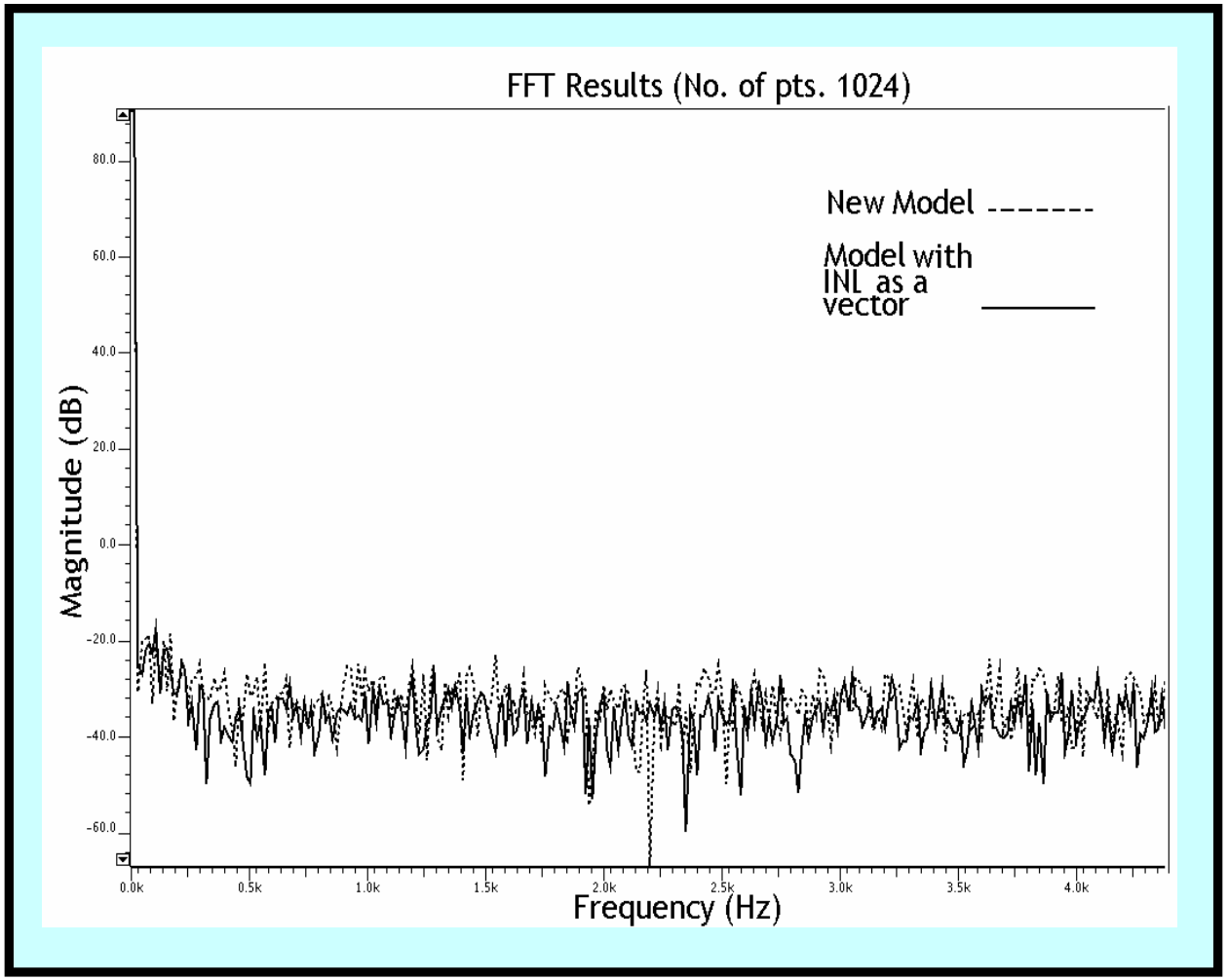
Simulation Results

- INL calculated using the new model.
- The INL is shown for the whole input range.
- The minimum and maximum values are very close to those of the input vector.



Simulation Results

- **Spectral distribution for both models.**



Note: A real 12-bit ADC was simulated and the results were very close.

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Conclusion

- The model appears to be much faster compared to real circuits and other models developed with different techniques without losing much accuracy.
- Showed a noticeable speed gain.
  Varied from 150x to 300x for different tests.
- The proposed model is suitable for all types of ADCs because it is not structural.
- It models the average overall performance of the converter.
- It is used for converters with high resolution bits.

Future Work

- Further experimental tests comparing more real circuits, having different architectures, with the proposed model.
- Validating the model for low resolution ADCs.
- Calculating the exact value of the non linearity rather than the average value. The deviation from the average is a Chebyshev polynomial of the second type. It is expected that this enhancement of the INL value will NOT affect the speed of the model.
- Adding other effects to the model such as supply noise and temperature effects.

Questions?