# Expected Performance Centering for Analog Designs

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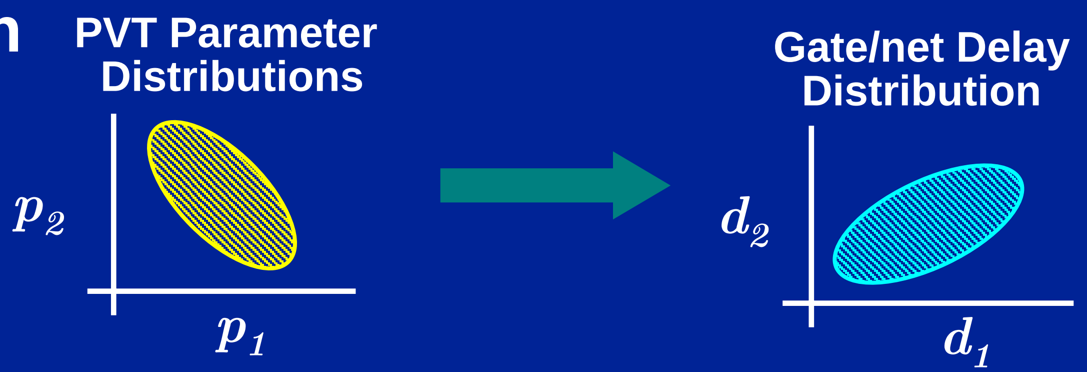
# Outline

- Existing Robust Analog Design Techniques
- Expected Performance Centering
- Statistical Computation Techniques
- Experiments
- Conclusion

# VLSI Variability

- Increased variability in nanometer VLSI designs
  - Process:
    - OPC → Lgate
    - CMP → thickness
    - Doping → Vth
  - Environment:
    - Supply voltage → transistor performance
    - Temperature → carrier mobility μ and Vth
- These (PVT) variations result in circuit performance variation



# Analog Design Parametric Yield Optimization

- Analog design
  - Complex metrics
  - Strong sensitivity to process variations

1. Robust programming
2. Stochastic programming
3. (explicit parametric yield optimization)
4. Design centering
5. Performance centering
6. Taguchi's quality loss function

# Robust Programming

- **Bound design and process parameter variations in polyhedrons or ellipsoids**

$$
\begin{aligned}
&\textit{Maximize} \quad \sup_{x \in u} f_0(x) \\
&\textit{Subject to} \quad \sup_{x \in u} f_i(x) \le 1, \quad i = 1, \dots m \\
&\qquad g_i(x) = 1, \quad i = 1, \dots p \\
&\qquad x_i > 0, \quad i = 1, \dots n
\end{aligned}
$$

- **If the objective and the constraints are all posynomials, this is a geometric programming**

# Stochastic Programming

- Explicit parametric yield maximization

$$\begin{aligned} &\textit{Maximize} \quad Y \\ &\textit{Subject to} \quad Y = \Pr(y < U) = \int_R \Pr(x)dx = \int_{\partial R} D(x)dx \\ &\qquad\qquad\quad \nabla \bullet D(x) = \Pr(x) \end{aligned}$$

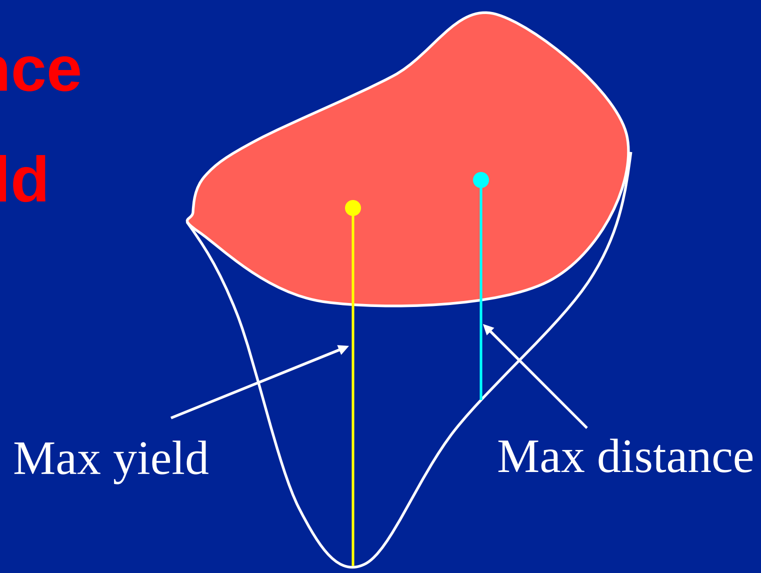
- Y = parametric yield
- y = design metrics
- U = design specifications
- R = acceptability region

# Design Centering

- Explicit parametric yield maximization
  - Yield gradient based greedy optimization
  - Recursive partition of ellipsoids
  - Recursive partition of polytopes
- Maximum parameter distance (to boundaries of an acceptability region in the design parameter space)
- Maximum parameter distance

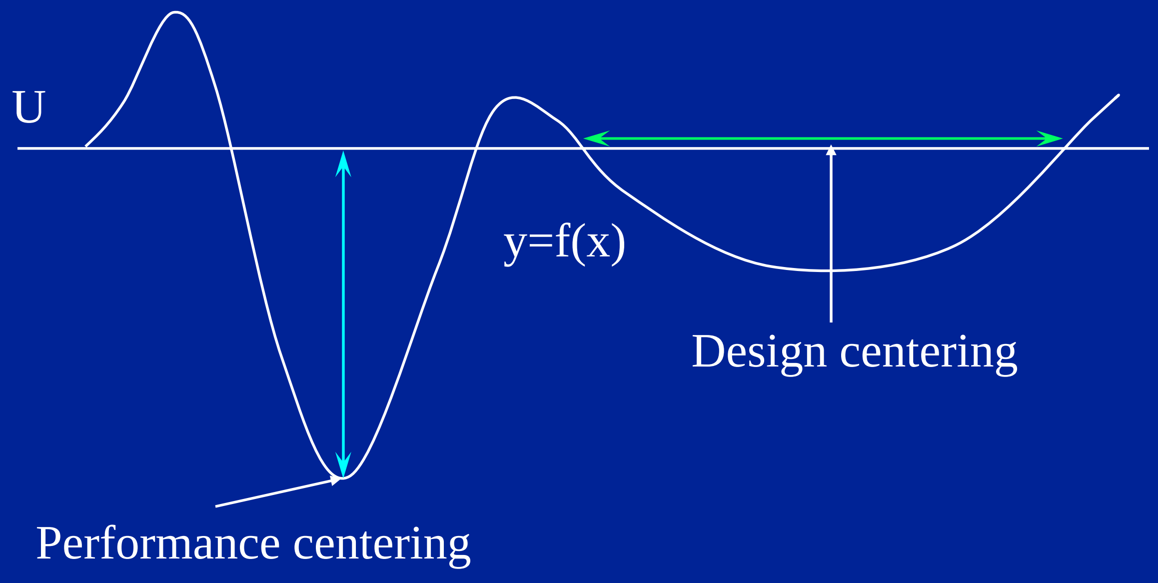
  ≈ maximum parametric yield

  *e.g. 15% Lgate variation*



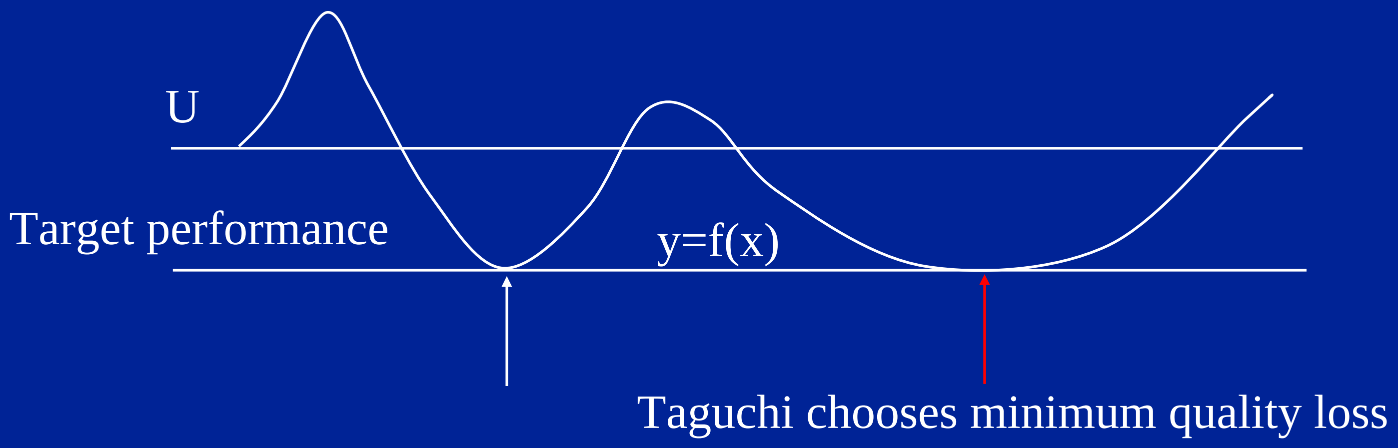
# Performance Centering

- Maximum distance to the boundaries of the performance acceptability region in the performance space
- Performance targeting ≠ yield maximization



# Taguchi's Quality Loss Function

- **Increases as the circuit performance deviates from the target performance**
- **Reducing performance variability as a means for *both* parametric yield maximization and performance targeting**




- ***What is the domain of the quality loss function?***

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# Expected Performance Margin

- **Expected performance margin in the presence of design parameter variation P(x) is given by**

$$\phi(x) = \int_R \rho(x+\varepsilon)\,\Pr(x+\varepsilon)d\varepsilon = \int_R \Pi_i\,(U_i - y_i(x+\varepsilon))\,\Pr(x+\varepsilon)d\varepsilon$$

- **x = design parameters**
- **ε = variations**
- **y = design metrics**
- **U = performance constraints**
- **R = acceptability region**
- **ρ = performance margin**

# Expected Performance Margin

- For extremely small variabilities, e.g., $P(x+\varepsilon)=\delta(\varepsilon)$

$$\phi(x) = \int_R \rho(x+\varepsilon)\delta(\varepsilon)d\varepsilon = \rho(x)$$

→ expected performance margin = performance margin

- For extremely small performance margin $\rho(x) = \alpha$

$$\phi(x) = \int_R \alpha \Pr(x+\varepsilon)d\varepsilon = \alpha Y$$

→ Expected performance margin = parametric yield

- Expected performance margin $\in$ Taguchi's quality loss function

# Expected Performance Centering

- **Given**
  - **Design parameters x**
  - **Design parameter variabilities Pr(x+ε)**
  - **Performance constraints y < U**
- **Find design parameters x* such that the expected performance margin is maximized**

$$\begin{aligned}
&\textit{Maximize} \quad \phi(x) = \int_R \rho(x+\varepsilon)\,\mathrm{Pr}(x+\varepsilon)\,d\varepsilon \\
&\textit{Subject to} \quad \rho(x+\varepsilon) = \Pi_i (U_i - y_i(x+\varepsilon)) \\
&\qquad y_i(x+\varepsilon) \le U_i, \quad \forall x+\varepsilon \in R, \forall i \\
&\qquad x \ge 0
\end{aligned}$$

# Expected Performance Centering

- *Input: x Pr(x+$\varepsilon$), y < U*
- *Output: x* s.t. f(x*) is maximized*

1. *Construct a performance macromodel y = f(x)*
2. *Find acceptability region boundaries y = f(x) = U*
3. *Compute performance margin $\rho$(x)*
4. *Computer expected performance margin $\phi$(x)*
5. *Find maximum expected performance margin $\phi$(x*)*

# Expected Performance Margin Computation

- **Sampling**

$$\phi_{sampling} = \frac{1}{N}\sum_{i=1}^{N}\Pi_i(U_i - y_i(x+\varepsilon = a_i))$$

**posynomial → geometric programming**

- **Gaussian integral**

$$\int_0^z \frac{1}{\sqrt{2\pi\sigma}} e^{-\frac{(\varepsilon-\mu)^2}{2\sigma^2}} d\varepsilon = \frac{1}{2} erf(\frac{z-\mu}{\sqrt{2\sigma}})$$

**if y = f(x) is polynomial, Pr(x) is Gaussian**

- **Surface integral**

$$\phi(x) = \int_R \Pi_i(U_i - y_i(x+\varepsilon))\Pr(x+\varepsilon)d\varepsilon = \int_{\partial R} \Pi_i(U_i - y_i(x+\varepsilon))D(x+\varepsilon)d\varepsilon$$

$$\nabla \bullet D(x) = \Pr(x)$$

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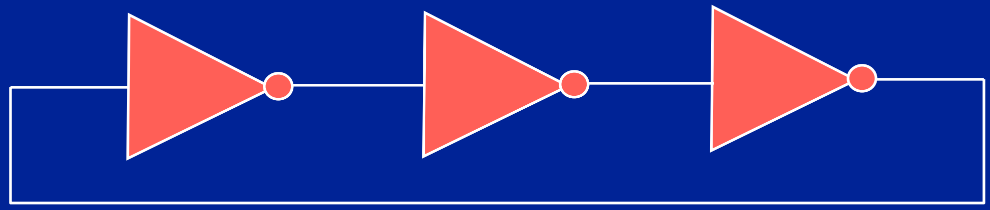
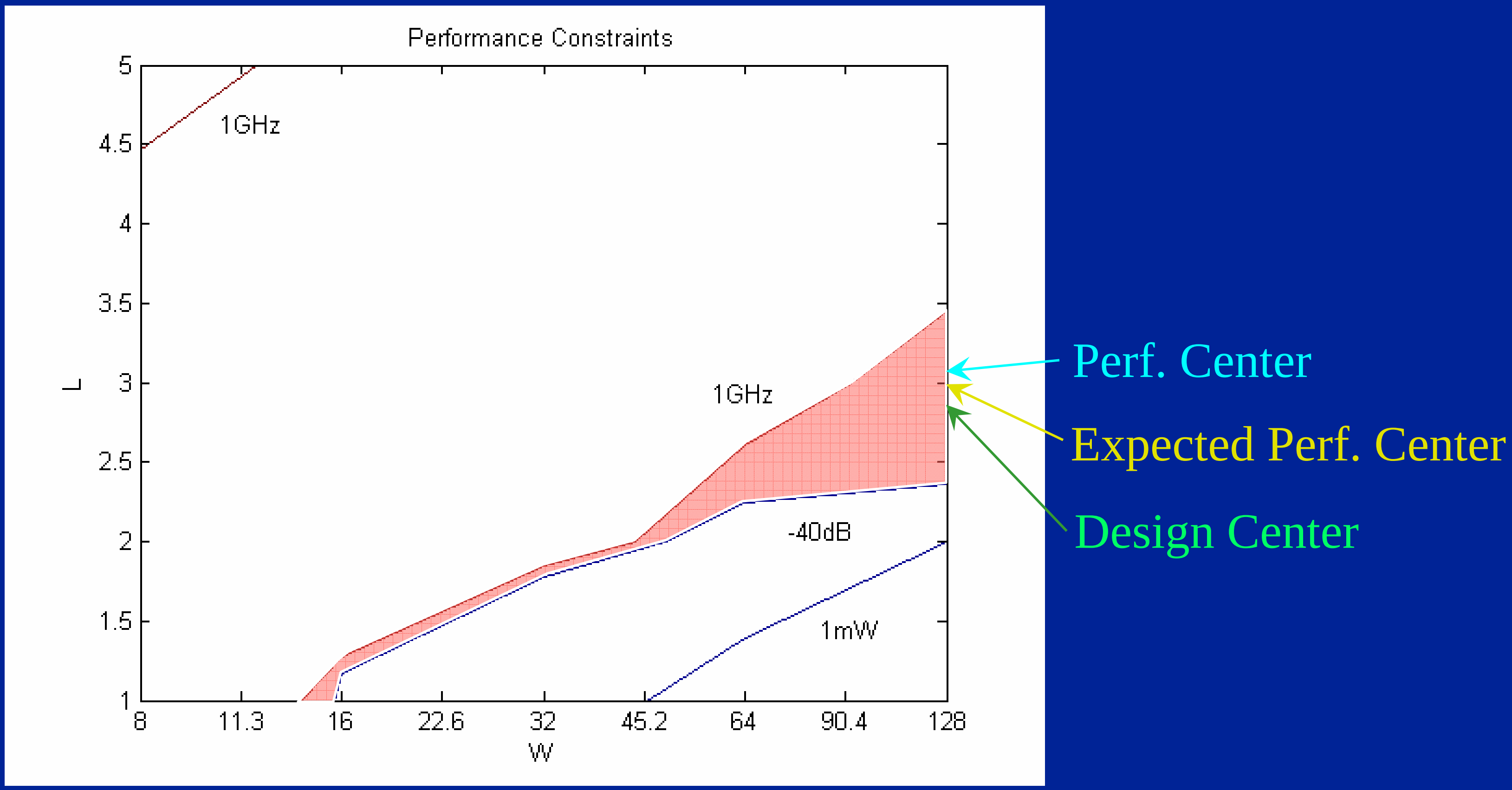
# Experimental Setup

- Three-inverter ring oscillator
- Synopsys HSpiceRF simulator
- 70nm Berkeley Predictive Technology Model
- Performance metrics:
  - Oscillation frequency $f_0$ > 1GHz
  - Phase noise N < –40dB
  - Power consumption P < 1mW
- Delay parameters
  - Transistor channel width and length



# Experimental Results

- **Acceptability region and performance contours**



# Experiments

I. Design centering

II. Performance centering

III. Expected performance centering

- ρ = performance margin
- ϕ = expected performance margin

| | $W$ | $L$ | $\rho$ | $\phi$ |
|---|---|---|---|---|
| *I* | *128.0* | *2.91* | *75.37* | *65.42* |
| *II* | *128.0* | *3.04* | *80.33* | *67.12* |
| *III* | *128.0* | *3.00* | *79.76* | *67.53* |

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# Summary

- We propose maximum expected performance margin as a new analog design objective
- → performance targeting in the presence of small process variations
- → parametric yield maximization (design centering) for small performance margin
- ∈ Taguchi's quality loss function
- Expected performance margin computation and maximization methods

**Thank you !**