Functional Verification of Radio Frequency SoCs using Mixed-Mode and Mixed-Domain Simulations

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ABSTRACT

The main focus of this work is the functional verification of radio frequency (RF) transceivers and RF systems on chip (SoCs). The use of enhanced baseband behavioral description models for an industrial available multiband, low IF GSM receiver is demonstrated. The necessity of functional verification when dealing with complex baseband signals and mixing operations with high/low sideband possibilities is shown. Future demands on language constructs and their implementations into the design flow are presented. Fundamental simulation comparisons for different implementation levels and proposals for new constructs to ensure functionality and connectivity between advanced behavioral description level and transistor schematics are made. This paper concludes with a suggestion for an extension of the Verilog-HDL-family to aid SoC designers in their effort to shorten the time to market and demonstrates the possible benefits of upcoming SystemVerilog constructs.

1. INTRODUCTION

The time consumption of mixed-mode circuit simulations for high frequency transceivers is mostly dependent on the carrier frequency, which determines the maximum time step to be used during the simulation. At carrier frequencies from 850 MHz to 1.9 GHz for GSM systems, the required time for transient simulations on transistorlevel for sophisticated transceiver designs with a high number of active components exhaust the available computation power, even using state of the art computer systems. A transient simulation of a complete transmission burst is therefore impossible for a transistor level view of the final tape out database.

While simulation techniques like harmonic balance or periodic steady state analysis show good performance in strict RF systems, they principally fail in mixed-mode simulations with digital parts as SoC's or single chip transceiver solutions and are therefore of no use for full chip verification.

Rising complexity of upcoming transceiver chips in mobile communications like the E-GOLD Radio from Infineon Technologies or the SiLabs AeroFONE demand for early verification in the design process. A pre-silicon verification of the tape out data base is therefore an important goal to minimize the development costs. Redesigns due to simple but undetected errors could be avoided and the development time decreases in order to achieve a better time to market. An example of one of these critical errors when dealing with complex signaling and low/high sideband mixing operations is shown in section 6.

A top down approach for RF-subsystems in SoC's and their requirements on the EDA-software is proposed and demonstrated for a commercial available multiband GSM transceiver. The benefits and demands for baseband verification and the necessity for new language constructs for present and future behavioral description languages will be shown.

2. TARGET AND PROBLEM DESCRIPTION

One of the desired targets is to achieve a functional verification of the whole chip on the final tape out database, another one to enable accurate long time transient simulations which can be used for system concept engineering. A functional verification is hereby defined as the possibility to verify the complex functionality of the transceiver, such as on/off switching, gain control and calibration loops, ramp ups, power down modes and alike.

This combines the traditional simulations used for system concept engineering and transistor level schematics, which differ a lot. At present, most system designers only think in terms of bit error rates (BER) or even package error rates (PER) which need a huge number of received bits for accurate calculations and are very time consuming for real circuit simulations. The RF designers, creating the schematics and the real silicon focus mainly on aspects like noise figures, gain values and power consumption of their building blocks. This gap is usually imperfectly closed by spreadsheets which contain abstract requirements and additional specifications for each block.

The mentioned (second) long term target of the presented work is to achieve common executable specifications in a matter that can be used by both RF designers and system engineers throughout the whole design process (top down approach). The long-time transient system simulations, re-

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quired to calculate the BER or PER, are typically done on abstract description levels. These are mainly languages and tools like Matlab^{TM} or SPW^{TM}, which don't support a functional check neither on the transitor level schematics nor on the tape out database. The schematic entry and layout is typically done in tools like Cadence DFII^{TM} or Mentor Graphics^{TM}. In contrast to the system level design, the RF designers focus on AC and short time transient simulations like periodic steady state or harmonic balance, which are simulated with tools like SPECTRE^{TM} inside of the design framework. These simulations are typically carried out on special testbenches, seperated from the toplevel layout of the chip.

3. FUNCTIONAL VERIFICATION BASEBAND MODELS FOR TYPICAL RECEIVER STRUCTURES

The RF carrier frequency or multiples of it, which are generated by the on-chip oscillator, enforce short simulation timesteps due to their short time constants. The size of the matrix, which has to be solved for each of these time steps, is approximately proportional to the number of nodes used in the circuit. In analog simulations, each transistor requires at least about ten equations to be evaluated. The count of active transistors in the high frequency signal path is typically quite low, most transistors are used to define operating points, biasing, control logic and current mirrors. In comparison to this, the digital part consists of tens of thousands of transistors which are often synthesized from high level languages like VHDL or Verilog. With mixed signal simulators it is possible to simulate these synthesizable or already synthesized logic together with behavioural and/or transistor models of other blocks.

Complex baseband signals ($I(t)$, $Q(t)$) are typically upconverted in the transmitter to the carrier frequency (ω) with a 90 degree phase shift like shown in equation 1.

$$RF(t) = I(t) \cdot \cos\omega t - Q(t) \cdot \sin\omega t. \quad (1)$$

This can be written as baseband representation with

$$B(t) = I(t) + jQ(t) \quad (2)$$

and the carrier frequency ω as a constant parameter. Another representation for this is the real part of the complex envelope with the modulated carrier

$$RF(t) = \Re\Big\{ B(t) \cdot e^{j\omega t} \Big\}. \quad (3)$$

The theoretical fundamentals are extensively described in [2].

Figure 1 illustrates the verification problem. While a generic single ended LNA has only two pins to connect to the schematic, it is necessary for the baseband simulation to transmit at least I,Q and ω between the blocks. Differential signals are commonly used in RF design, so the workaround in the top right corner has been used for the proposed design keeping ω a constant parameter in the block description. For a complete flow, the connection variant shown in the bottom right corner is necessary, but not available in current implementations of the hardware description languages (HDL). Verilog, as one of the major HDLs does not have

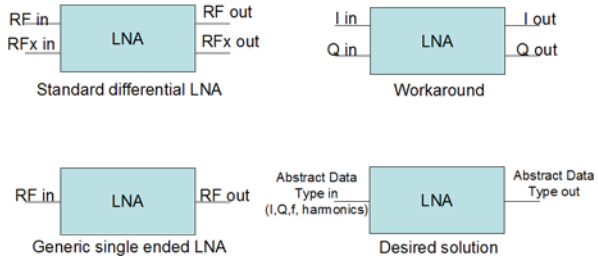

Figure 1. Different connectivity structures

support for complex structures or data types to be passed over single connect wires together with ports in schematics as desired for continous functional verification. The international standards, which are the base for the software implementations of the EDA vendors, still lack sufficient support in terms of new language constructs to ease the connectivity verification. The upcoming SystemVerilog promises good constructs, but misses analog extensions like in Verilog-AMS at the moment. VHDL does support complex dataypes, but these are not sufficiently supported on toplevel by present netlisters and simulators.

For most simulations, one is only interested in the distortion that the baseband information receives during its ride on the carrier, not on harmonic disturbances of the carrier itself. Most distortions and nonlinear effects occur as simple amplitude modulations. Severe problems arise, when harmonics, which can likely be introduced through the mixer and additional large signals present at the input, become critical for the system's perfomance. If these harmonics are introduced in the traditional way as addition to the original signal, the necessary bandwith increases. Hence, the highest simulation frequency for the baseband signal rises again and the performance benefit is lost. The desired solution would connect the blocks with additional harmonic baseband signals, that can be described with their own respective carrier frequency. Each signal is then described as the addition of carrier frequencies and the corresponding baseband informations.

E.g. a simple mixing operation of a sinusoidal carrier with a complex signal

$$RFinput = A(t) \cdot sin(\omega_1 t) + B(t) \cdot cos(\omega_1 t) \quad (4)$$

$$LOsignal_I = L \cdot cos(\omega_2 t) \quad (5)$$

$$I(t) = LOsignal_I \cdot RFinput \quad (6)$$

equals the signal I(t) with two frequency components at the sum and difference of the original frequencies.

$$I(t) = \frac{L \cdot A(t)}{2} \cdot (sin(\omega_1 t - \omega_2 t) + sin(\omega_1 t + \omega_2 t)) \quad (7)$$

$$+\frac{L \cdot B(t)}{2} \cdot (cos(\omega_1 t - \omega_2 t) + cos(\omega_1 t + \omega - 2t)) \quad (8)$$

This can be described as the two baseband representations

$$\overline{I}(t)_{low} = \begin{cases} \frac{L \cdot A(t)}{2} \cdot sin(\omega t) \\ \frac{L \cdot B(t)}{2} \cdot cos(\omega t) \end{cases} \text{ with } \omega = \omega_1 - \omega_2 \quad (9)$$

and

$$\overline{I}(t)_{high} = \begin{cases} \frac{L \cdot A(t)}{2} \cdot sin(\omega t) \\ \frac{L \cdot B(t)}{2} \cdot cos(\omega t) \end{cases} \text{ with } \omega = \omega_1 + \omega_2. \quad (10)$$

For more abstract constructs, this can be extended to the complete range of n harmonics

$$\overline{I}(t) = \overline{A(t)} \cdot sin \begin{pmatrix} n\omega_1 - n\omega_2 & \dots & n\omega_1 & \dots & n\omega_1 + n\omega_2 \\ \dots & \dots & \omega_1 & \dots & \dots \\ -n\omega_2 & -\omega_2 & 0 & \omega_2 & n\omega_2 \\ \dots & \dots & -\omega_1 & \dots & \dots \\ -n\omega_1 - n\omega_2 & \dots & -n\omega_1 & \dots & -n\omega_1 + n\omega_2 \end{pmatrix} \cdot t \tag{11}$$

and

$$\overline{Q}(t) = \overline{B(t)} \cdot cos \begin{pmatrix} n\omega_1 - n\omega_2 & \dots & n\omega_1 & \dots & n\omega_1 + n\omega_2 \\ \dots & \dots & \omega_1 & \dots & \dots \\ -n\omega_2 & -\omega_2 & 0 & \omega_2 & n\omega_2 \\ \dots & \dots & -\omega_1 & \dots & \dots \\ -n\omega_1 - n\omega_2 & \dots & -n\omega_1 & \dots & -n\omega_1 + n\omega_2 \end{pmatrix} \cdot t \tag{12}$$

For most applications the high band of the mixing process is far from any critical performance, the problems which must be thought of occur especially when dealing with large blocking signals or LO feedthrough.

The calculations in the receive blocks grow from simple additions and multiplications to frequency dependent variations of the functions, which can be expressed through simple matrix operations. Since most of the harmonics still remain zero, it is possible to preserve the matrix from growing too big with a generic representation as

$$\overline{I}(t) = \overline{X} \tag{13}$$

$$X = \begin{Bmatrix} A(t) \\ B(t) \\ \omega \end{Bmatrix}. \tag{14}$$

This would require additional computational effort in the models when thinking of e.g. filter algorithms. At present, these simulations can not be realised on toplevel, because the necessary constructs to pass this abstract data types between the blocks are not available.

4. EXAMPLE RECEIVER

4.1 Analog RF components

The demonstration example for this paper is shown in figure 2.

The schematic shows the building blocks of a commercial available GSM sigma delta based multi band receiver, including receive and transmit path as well as oscillator structures, buffers and the digital core in the center.

For the simulation, a GSM signal is generated, transmitted over a fictional AWGN channel and then passed into the receiver. The received signal is amplified and downconverted to the intermediate frequency. After this, the unwanted frequencies are suppressed using a higher order polyphase filter structure. Afterwards a sigma delta based A/D converter is used to convert the analog signal to the digital domain and is passed into the digital baseband.

The behavioural model of the low noise amplifier is a simple differential voltage amplifier with some nonlinearities. To minimize calculations during runtime, the conversion from typical engineering units (3rd order intercept point, noise figure and gain in dB) to the necessary implementation units are done at the initial step of the simulation. The noisefigure is modeled as a white noise voltage source and added to each of the differential inputs. A special treatment of multiple input frequencies as described in section 3 was not necessary due to the wideband characteristics of the LNA.

For baseband simulations, the mixer model can essentially be reduced to it's gain feature, some third order nonlinearities and I/Q mismatch effects.

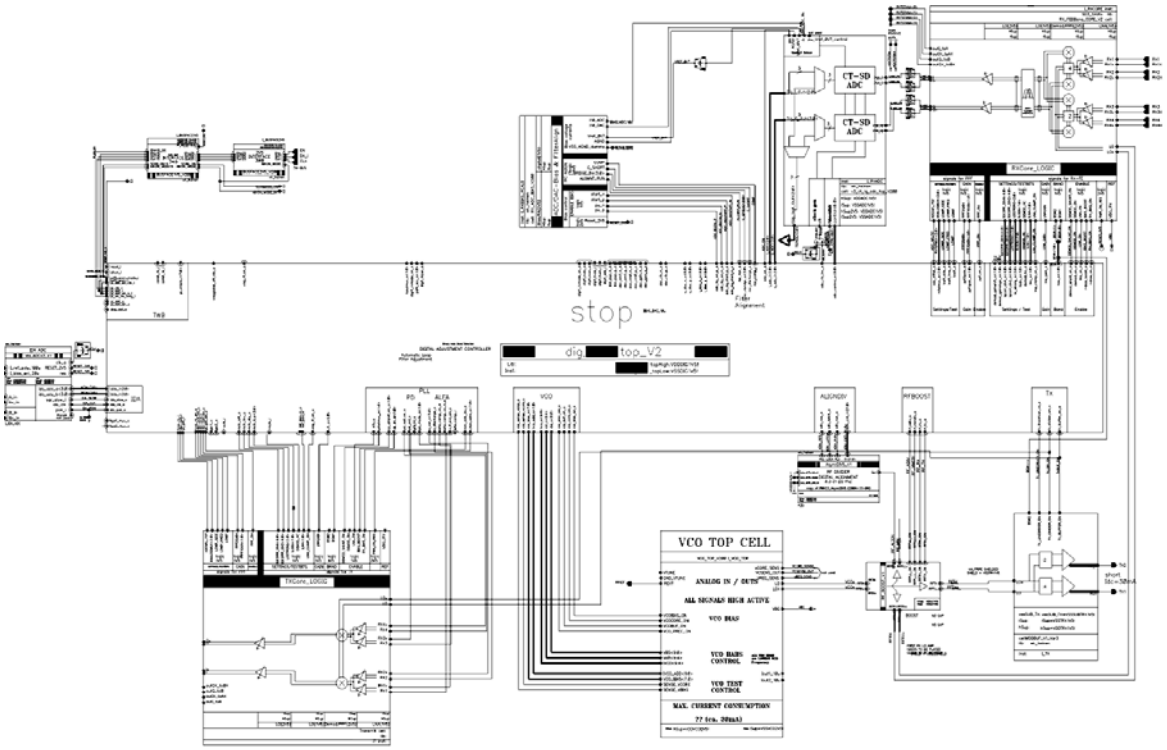

Figure 2. Cadence Schematic View of the Receiver Example

To achieve this, each path is implemented with separate parameters. The gain and limiting effects are then modeled the same way as in a low noise amplifier. The frequency conversion effects have been explained in the previous chapter. For minor variations of the low IF frequency, the mixer can additionally be operated as a complex mixer with

$$I_{out} = I_{in} \cdot cos(\Delta\omega t) + Q_{in} \cdot sin(\Delta\omega t) \quad (15)$$

$$Q_{out} = Q_{in} \cdot cos(\Delta\omega t) - I_{in} \cdot sin(\Delta\omega t). \quad (16)$$

In the available design, several stages interact with each other to set the correct gain values for each block depending on control signals from the digital core. Setting a digital gain value in the VHDL digital baseband core block leads to several adaptions in the biasing as well as forward and backward interaction between the RF blocks. The baseband simulation result for a single gain step of the LNA is shown in figure 3. The biasing blocks were kept on transistor level

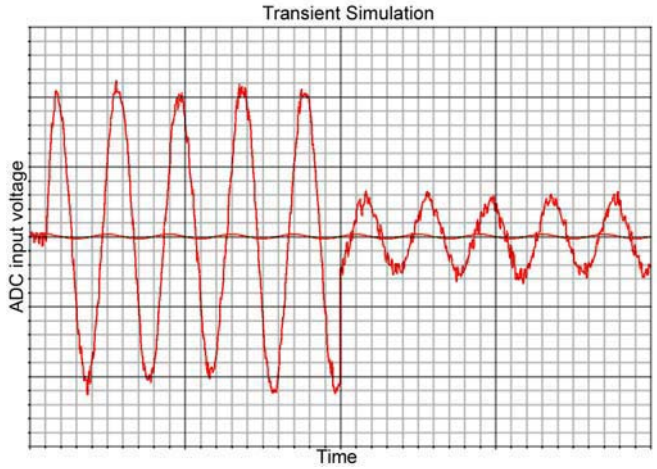

Figure 3. Transient signals

for all simulations, as these are the most critical parts for the functional verification. Nevertheless it would be possible to reduce their complexity by substituting current mirrors and alike through simple switchable dc sources or a behavioural model of the whole block.

The example chip makes extensive use of differential signal wiring. These wires were re-used as shown in figure 1 for passing the seperate I and Q values of the baseband signal between the RF blocks. Typical effects from phase noise, frequency drifts and I/Q imbalances were modeled as static parameters. These could be included as dynamic elements, if abstract datatypes would be passable over single net connections as desired.

4.2 VHDL Core Logic

The digital core logic of the transceiver consists of synthesized VHDL code. For this demonstration, only parts of the whole logic were used to demonstrate the feasibility and performance of the modeling approach. All bias switches, gain settings and power down modes were implemented and programmed to do a full bootup of the receiver chain and to receive a complete GSM burst ($600\mu s$) with different gain steps.

5. CURRENT IMPLEMENTATION AND LIMITS

As stated before, one of the major problems is the functional verification of the final tape out database.

While the baseband models provide enough performance to enable a full burst simulation in an acceptable time frame, one major problem persists. The schematics and connections between baseband models and transistor level schematics must be identical to ensure correct connectivity throughout the design process. But, the number of connections to baseband models and RF models differ in general since the signals are transferred in different variations (see figure 1). While high frequency components just require one input signal (although often differential), even the simplest baseband models require the inphase and quadrature signals as separate components.

Differential circuits are commonly used in RFICs, so it is possible to avoid the use of additional wires by putting the I - signal on the positive net and the Q-signal on the negative net, respectively. Since noisefigures, gain and intercept points are specified for the given carrier frequency, this is at the moment sufficient, but not really the desired solution. Additional harmonics and conversion effects can not be taken care of at the moment.

Additionally, it is necessary to take care of switching the complete chain between the different implementation variants, because I/Q and real differential signals on the wire can't interact with each other. Future system verilog connect modules are giving interesting perspectives here.

The low frequency blocks can more easily be switched between the different implementations, since I and Q signals already exist after the first complex downconversion mixer. Performance benefits can still be obtained, if the IF-frequencies can be obmitted or expressed with abstract signals.

6. SIMULATION AND VERIFICATION PERFORMANCE

Figure 4 shows the analog frontend receive chain of the transceiver. It mainly consists of two dual band LNAs and two mixers for the 850/900 Mhz and the 1800/1900 MHz range. Additionally common mode supression and the polyphase filter is implemented, as well as a biasing block and the I/Q generation.

The receiver was simulated using a state of the art multi processor computer system and Cadence^{TM} IC 5.10.41 USR 3 with SPECTRE 6.0 and Incisive Unified Simulator 5.6. The simulated GSM system time was slightly more than a complete burst for the baseband structures and far less for the transistor level schematics, because the simulation on transistorlevel would have taken 25 days real time for a complete GSM burst compared to only 37 seconds for the best baseband implemenation.

In Figure 5 the simulation performances is compared for different implementation levels of the polyphase filter in the complete receive chain. For the far left simulation a complete baseband modelling of the transceiver was used.

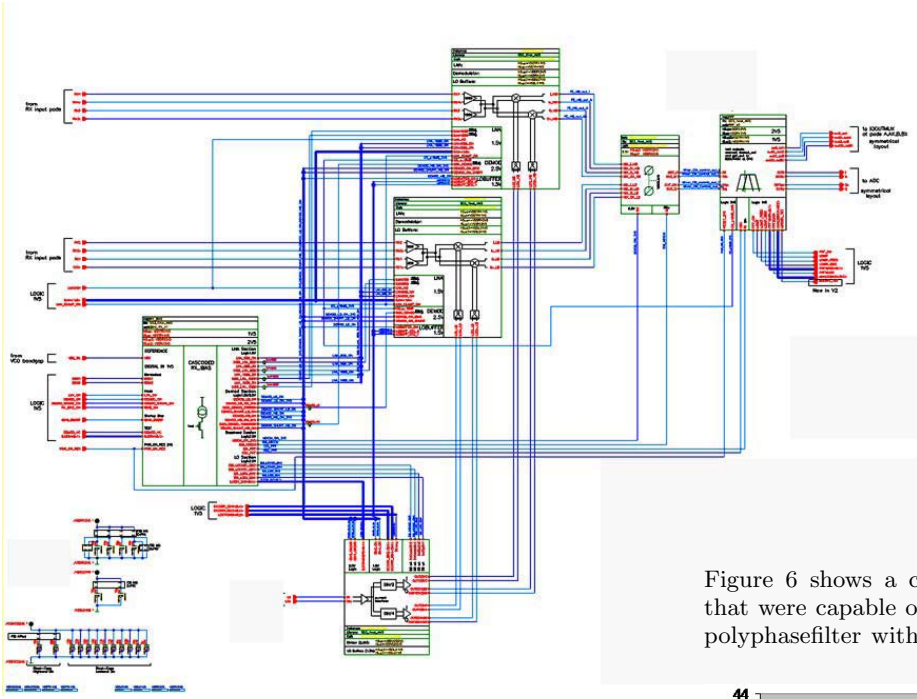

Figure 4. Receive Chain of the Transceiver

Demonstrating the top-down approach, a simple schematic of a Tow-Thomas biquad using voltage controlled voltage sources as operational amplifiers uses only slightly more computation time (42.35 s). Using this schematic with real models for the operational amplifiers required 287.36 seconds (5 minutes). This is still far less than the original polyphase filter which took 7243.66 seconds (2 hours) to simulate. Omitting the baseband modelling approach for the RF frontend, using the RF frequency verilog models for LNA and mixer, the simulation time raised to 697431.89 seconds (8 days). Simulating the complete receive chain on schematic level including the LNA, mixer, filter and biasing would have taken 25 days to complete.

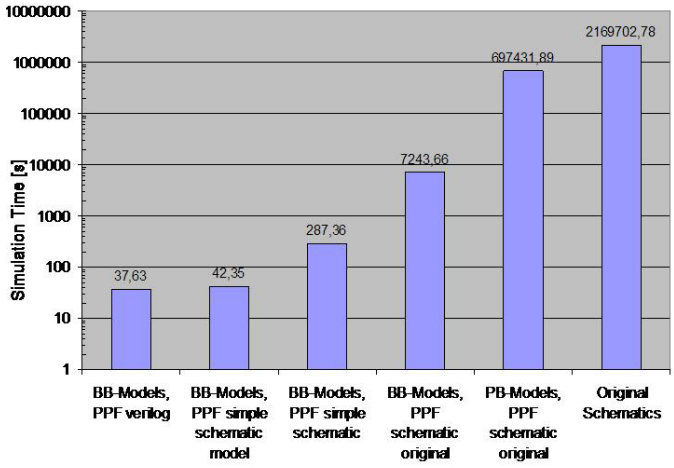

Figure 5. Simulation comparison for different configurations

Figure 6 shows a comparison for the different simulators that were capable of simulating the testbench of the single polyphasefilter without digital control features. The AMS

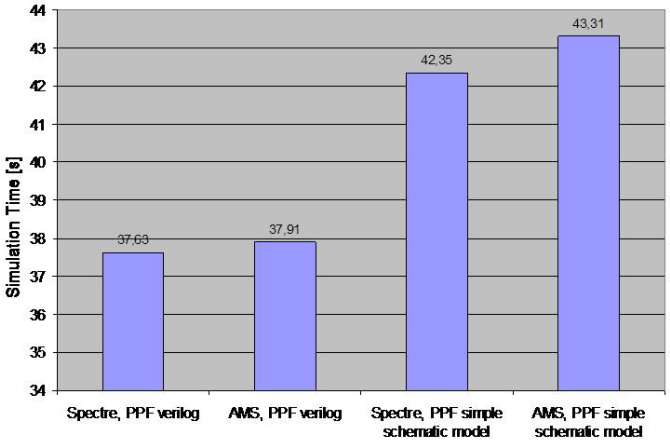

Figure 6. Simulation comparison between mixed signal simulator and SPECTRE

simulator from Cadence required only slightly more time simulating the baseband models than the pure SPECTRE simulator, although it is far more complicated (see [1]). On the left hand the complete baseband modelling approach is shown, compared to the Tow-Thomas structure of the polyphase filter on the right hand side. It is therefore obvious, that the mixed signal simulation, although more complicated than an analog only approach is not critical for the simulation duration.

In figure 3 the simulated output signals with high and low gain settings of the LNA prior to the polyphasefilter have already been shown. Clearly visible is the noise influence of the receiver blocks, which was significantly increased for the simulation compared to the original values and noisefigures. For this simulation it was necessary to exchange the VHDL logic block with SPECTRE compatible sources, since the transient noise option is not yet available in the AMS

simulator.

Today's GSM systems use a GMSK modulation for the signal. To verify the complete connectivity of the transceiver, a theoretical QPSK signal, fitting into the frequency range and limits of the receive path, was attached to the input. In state-of-the-art receivers, the in-phase and quadrature phase path can be switched digitally for reasons that are not in the focus of this paper. Figure 7 shows an incorrect constellation plot due to phase errors when these signals are accidentally twisted in the RF frontend. Figure 8 shows the

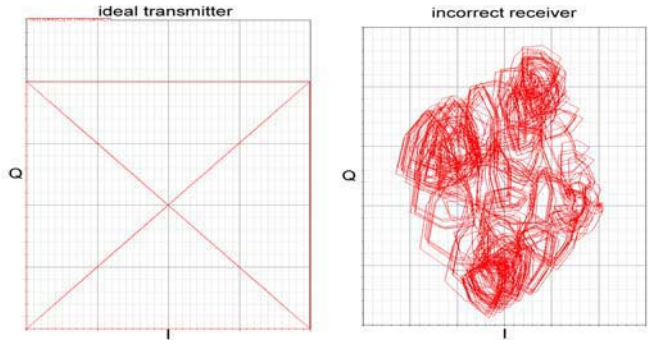

Figure 7. Incorrect constellation plot due to IQ twist

expected correct result. The rotation in the plot occurs due to a non-ideal coherent demodulation. With this simulation it is possible to evaluate and verify complex algorithms and adjustments to provide a correct digital baseband signal.

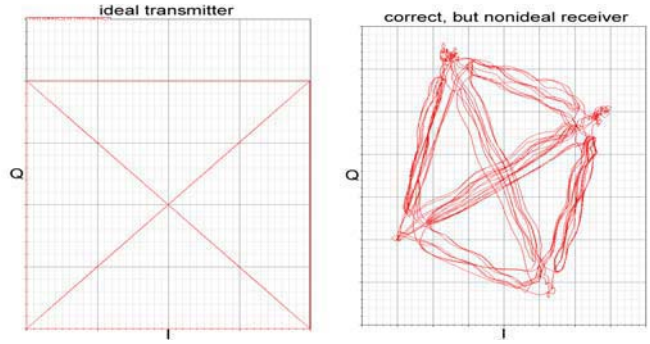

Figure 8. Correct constellation plot

7. RECOMMENDATIONS FOR HDL IMPROVEMENT

On the one hand, baseband modeling promises efficient ways of simulation speedups, but on the other hand, every simulation simplification leads to some information loss. Conversion effects from different harmonics, which occur through nonlinearities and mixer effects, are not taken care of anymore when using the simple approach. To ease the implementation of such additional information, which are to be transferred between the different simulation blocks of a transceiver, it would be desirable to have abstract data structures passed over single connections. This would enhance the simulation quality and would enable executable specifications as a long term target.

SystemVerilog as an upcoming new language promises a good and effective way of modeling these structures, but misses analog extensions like in Verilog-AMS at the time being. The implementation of packed and unpacked datatypes into combined structures is not yet possible. A comprehensive SoC-verification will require both, a SystemVerilog as well as a Verilog-AMS support for the RF components using abstract data types in their interfaces. The first of these might be used in a pure digital simulation environment, to verify the RF together with a large digital part, verifying the whole SoC. The second approach will be necessary for mixed-mode simulations in order to design the transistor level of the baseband analog or mixed-signal part.

Listing 1 shows the intended abstract structure for a single frequency wave. It includes the time varying I and Q components, the carrier frequency as a (typical) constant and additionally the phase information of the carrier frequency. With these informations, every single frequency conversion effect can be modeled for simple signals.

Listing 1. Typedefinition complex wave

```
typedef struct {
        real I,Q;
        real frequency;
        real phase;
        } complex_wave_t
```

Arrays of these complex waves as shown in section 3 can be used to add multiple harmonics, interferers or alike to the simulation. Combining different frequencies, signals and noise sources would lead to not only a time beneficial simulation, but also to more accurate and acceptable simulation results.

8. CONCLUSIONS

The feasibility and the performance benefits for using baseband behavioral models for the functional verification on the final tape out database has been demonstrated. At present, the main target of a functional verification on the final tape out database is achieved. Nevertheless, it is desirable to enhance the simulation quality to enable executable specs as long term target. The main problems which arise from the current HDL implementations are shown. A recommendation for HDL improvement was given in the last chapter. Using this strategy, a complete top down approach is possible. A comparison with more detailed simulations (e.g. on transistorlevel) is due to the immense time requirements not feasible. To our regrets, hardware measuremens were not available, but simulation accuracy is not the main focus of this paper. For future highly integrated RF transceivers, the benefits of early functional verification, using baseband behavioral models and the proposed structures for the connectivity checks, would be enormous. In addition to this, the common executable specifications for system engineers and schematic/silicon designers are getting closer due to the dramatic performance improvement and this would be a great achievement in overall chip design, opening doors for new concepts and approaches.

9. REFERENCES

[1] Cadence. Documentation for ius 5.6.

[2] J. E. Chen. *Modeling RF Systems.*