Functional Verification of Radio Frequency SoCs using Mixed-Mode and Mixed-Domain Simulations

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Outline

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Motivation

Modern transceiver systems feature:

- analog frontend
- digital enhancements
- digital calibration
- digital control loops
- digital predistortion
- digital interfaces
- digital programming

Several 100k gates are supporting and controlling the analog RF functions. RF verification consumes lots of manpower & money.
Motivation

• **Tape – Out produces immense costs**
  – First time right
  – Mask set - about a million $ for nano meter technologies
  – Wafer processing (time delay !)

• **Mistakes in complex systems are likely !**
  – Feedback between digital baseband logic and analog circuits (e.g. AGC, switchable filters, power up modes, PLL locking).

• **RF simulation speed is the bottleneck**
Targets

• **Short Term : Functional Verification of Tape Out DB**
  – Verify a complete transmission burst for different modes
    • Necessity to define a simulation strategy that covers all possibilities
  – Pin accurate compatible for all implementation levels!
  – Common database for verification and tape out
  – Just in time – always.

• **Long Term : Executable Specification**
  – Close the gap between
    • RF Engineer (Noisefigure, Gain, …)
    • System Engineer (BER, PER, …)
Verification Problem for Complex SoC

- **Simulation speed aspects**
  - A complete transmission burst including power up and bias settling is necessary (long transient).
  - Typical schematic of demonstration example (GSM Transceiver) on tape out database would take ~ 10 months to complete.
  - Traditional VerilogA model takes several days to complete
  - It is necessary to include the digital control logic and biasing structures.
  - Analog stepsize is inversely proportional to the highest frequency

- **Connectivity and functionality**
  - „Simply“ has to be ensured – more difficult than one may think…
Can We Speedup the Simulation?

- Distortions, noise and signal combinations are the verification target.
  - Distortions of the RF-carrier itself don't have any information.
  - Only the distortions of the carried payload are relevant.

=> Baseband modeling omits the carrier frequency.
Baseband-Modeling

- RF Signal from a complex upconversion:

\[ RF(t) = I(t) \cos(2\pi f_0 t) - Q(t) \sin(2\pi f_0 t) \]

- Equivalent, but complex baseband signal at the carrier frequency \( \omega_c \)

\[ B(t) = I(t) + jQ(t) \]

- Can be extended to frequency harmonics of the signal without increasing the bandwidth of each part through Fourier’s Theorem. Rises number of nodes in signal path, but keeps low frequencies.

- Main difference to standard behavioral modeling approach:

**Abstract and complex signals demand for other models and for different connectivity structures between the blocks.**

There’s still nothing like a „struct“ or „record“ on analog toplevel to pass multiple data over single connect wire.
Baseband-Modeling

Connectivity problem for verification purposes

„Single Ended Schematic“ with real valued signals

Equivalent baseband signal needs (at least) two connections (I,Q,f,harmonics,digital trigger,…)

=> New connectivity structures on simulation level are necessary!

Workaround at present:
RF blocks typically have differential wires that can be used
Demonstration Example

Commercial quad-band GSM transceiver
(Toplevel reduced for better display)
RX - RF Frontend

Analog Receive Chain

BIAS / CTRL

BB verilog models

Transistor Level

I/Q Generation

ADC

Digital Verilog AMS

ADC BIAS

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BMAS 2006
Polyphasefilter Implementation

Different implementation variants are possible (instantaneously switchable)

- a „near silicon“ schematic implementation with ideal or non-ideal opamps, that tries to match the real implementation as close as possible

- an approximation with a „standard“ polyphase structure which just implements near correct corner frequencies and gain

- an approximation as a true verilog modelling with parameters from the system designers

⇒ They differ more in simulation speed than in accuracy aspects arising from the number of equations to be solved.
Polyphasefilter Implementation (simple Schem)
Polyphasefilter Implementation (VerilogA)

module PPF_V2(...);

[...]

analog begin

[...]
\ A lot more stuff like VDD/VSS range checking, limitations, biasing, etc.pp.

[...]

I_{sum} = V(I_{in}) - V(I_{out}) - \frac{wM}{w_0} V(Q_{out});
Q_{sum} = V(Q_{in}) - V(Q_{out}) - \frac{wm}{w_0} V(I_{out});
V(I_{out}) = \text{laplace}_nd(I_{sum}, \{1\}, \{0, 1/w_0\});
V(Q_{out}) = \text{laplace}_nd(Q_{sum}, \{1\}, \{0, 1/w_0\});

end;

endmodule;
AC Simulation Times for PPF

- **Original Schematic**
  - 2297 nodes
  - 2348 equations
  - 459 s

- **Simplified Schematic** (no control/adjustment)
  - 36 nodes
  - 43 equations
  - 8.28 s

- **Verilog Modelling**
  - 28 nodes
  - 53 equations
  - 5.5 s

**Performance Gain**  x 80
First Testbench description

- GFSK (or QPSK) signal source @ 850, 900, 1800 or 1900 MHz
- low noise amplifiers
- mixers capable of mixing higher or lower sideband
- higher order polyphase filter
- Biasing structures
- **No ADC**

- ~ 13,000 Nodes
- ~ 16,000 Equations
- ~ 5,000 Transistors
- ~ 10,000 Caps
- ~ 10,000 Resistors
Implementation

• The RF-RX-part was implemented as pure VerilogA
  (although partly in VerilogAMS-Syntax)
• No clock necessary
• Pure analog signals and slow varying digital control logic
• RF frequency ommitted through use of baseband models
• Simulation is therefore only in the analog domain, not event triggered

-> possible to simulate with pure spectre
Simulation Results RF-RX
(no ADC, no digital part)

Performance Gain  x 50000
Extending with digital logic and ADC
Complete RX System

- ~ 30,000 Nodes
- ~ 35,000 Equations
- ~ 23,000 Transistors
- ~ 21,000 Caps
- ~ 17,000 Resistors
- Digital part as VHDL-model with >10,000 parallel processes
Signal Flow and Possibilities

Possibilities:

- **Source**: IQ Baseband (GFSK/QPSK)
- **LNA**: schematic, IQ Baseband, RF Passband
- **Mixer**: schematic, IQ Baseband, RF Passband
- **PPF**: schematic, simplified schematic, verilogA
- **RX/SD Bias**: schematic, verilogA
- **Digital Logic**: VHDL, verilogAMS
- **Clock**: analog, verilogAMS
Simulation Results Complete RX

Performance Gain  x 25000 (2.000.000 with simple ADC)
Simulation Profiles

<table>
<thead>
<tr>
<th>BB Modeling</th>
<th>digital</th>
<th>analog</th>
<th>Cost function digital</th>
<th>Cost function analog</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistorlevel - Bias</td>
<td>0.1%</td>
<td>99.9%</td>
<td>Connectmodules (7 %) VHDL core (6 %)</td>
<td>QPSK filter (2*0.6 %)</td>
</tr>
<tr>
<td>BB Modeling VerilogAMS - Bias</td>
<td>1.9 %</td>
<td>98.1 %</td>
<td>VHDL core(20%),</td>
<td>QPSK filter (2*1.8 %)</td>
</tr>
<tr>
<td>BB Modeling Verilog Bias Incl. ADC</td>
<td>3 %</td>
<td>97 %</td>
<td>VHDL core(6%), ADC (5%)</td>
<td>ADC (300%)</td>
</tr>
</tbody>
</table>

RF Simulation speed still is the bottleneck, but at least the verification is possible!
Simulation possibilities

Fast and effective I/Q verification

Accidentally twisted IQ path
Limitations of actual implementation

- Only simple real values are passable between the modeling blocks
- Abstract datatypes for connectivity approved simulation on toplevel are required to enable
  - Easy to go baseband modeling
  - LO influence on mixer (I, Q, f, PN, harmonics)
  - Harmonics for mixing and conversion effects
- Example and demands are already at EDA R&D
- System Verilog promises interesting variants
  - Access by name / access by task would enable mixed BB/PB simulations without taking care of switching the full chain.
  - SystemVerilog AMS would really be great …
Conclusion

• A GSM RX path has been modeled using baseband behavioral description approaches.
  – Functional verification prior to Tape Out was completed in ~ 16 min, including clocked SD-ADC
  – Included in this verification
    • Signal flow (Constellation plot with QPSK signal)
    • PU/PD modes
    • Frequency select
    • Sideband select
    • Gain settings
    • Biasing on transistor level
    • Digital Core