Design in the nano era: a statistical challenge!

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Small dimensions on large wafers

Wafer Size History

200mm/1990  300mm/2001  450mm/2012  675mm/2021?
IC industry: Quo vadis?
Moore’s law: Cost per IC function

Reference point: 30 mm² in CMOS12,

Dataquest: monitor of wafer price per unit area 1998-2005
Dataquest mask cost: 1998-2010
More on a chip: the power crisis

Year of production (ITRS)

Power = activity x frequency x capacitance x \( \text{voltage}^2 \)
Power crisis:

Need to reduce power supply voltage limited by:
- sub-threshold leakage
  (can be avoided by switching functional blocks)
- variability
Outline

• Variability: deterministic effects
• Variability: statistics
• The analog approach
• The digital approach
• Signal Integrity
• Outlook
Variability: what is it?

Uncontrolled parameter variation between individual transistors or components in one circuit:

intra-die instead of inter-die variations.

“Uncontrolled”=

- Technologist: something new on the IEDM
- Designer: something not included in the CAD tools
Deterministic effects, but difficult to predict and control:
- Lithographical deviations
- Negative Bias Temperature Instability
- Well Proximity Effect
- Signal integrity
- Stress by wiring or Shallow Trench Isolation
- Temperature gradient
- Substrate noise

Stochastic (random) processes:
- Component mismatch
- Jitter
- ........................and many more effects
Lithography

Variability:
90 nm CMOS
Frequency distribution of free-running oscillators
16x7 per reticule

Center Donut (RTA)

boundary

Random deviations

Courtesy: Boris Ljevar (Philips)
Stress is used to improve mobility

Layer applied to create stress

Tensile stress increases electron mobility (30-50%)

Compressive stress increases hole mobility (50-70%)
Shallow trench isolation (STI):

- STI field isolation creates compressive stress
- Increases hole $\mu$, reduces electron $\mu$
- Up to 10% $\Delta I_{D_{sat}}$ at close range
- Links lay-out environment to current drive

Source: “Observation after SACOX, C065 STI Trench morphology » Crolles 2 alliance Celine Detchevery
Stress caused by tiling!

Mismatch differences caused by mechanical strain differences due to asymmetrical placement of Metal-2 CMP dummies! Current loss of 1-5 %

2/1 μm trans.
Substrate Noise:

A designers view
The problem:

Interference generator:
- every node of the circuit is contributing, depending on frequency components, capacitor, undershoot

Interference channel:
- mostly through substrate, but may take short-cuts!

Interference receiver:
- every node picks up interference, many (canceling) paths
A simple experiment

0.18 um CMOS
High-ohmic substrate
Substrate model extracted by commercial tool:
5487R’s and 6765 C’s

 Courtesy: AMoS/G.Vogels
A simple experiment

8 variants in x, y, guard ring
silicon compared to simulation

70 dB between different layout implementations!
(interferer: 1 MHz sine wave at 100 mV amplitude)

Courtesy: AMoS/G.Vogels
Some observations:

• Substrate modeling works for simple circuits however also a very accurate description of the power grid is needed!

• Simple circuits result in a complex substrate description, interpretation is difficult

• No practical solution to simulation with substrate noise

• No clue towards interference reduction
Variability: Deterministic effects

• Many flavors of effects as processes shrink

• Most effects can be kept in check via design rules

• The penalty is in additional area, labor and power.

• Transfer of designs becomes more difficult: “annotated designs”

• Simulation approach is unclear.
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Limits to accuracy

Basic limit to accuracy is the ability to reproduce exact copies,

What are the basic reasons?
Granularity on molecular level is reached:
0.25/0.25 transistor = 1200 doping atoms
0.1/0.065 transistor = 60-80 atoms

Stochastic variations in number of atoms dominate the component behavior
CMOS matching

\[ \Delta V_T = V_{T1} - V_{T2} \text{ in mV} \]

\[ \sigma_{\Delta V_T} = \frac{A_{VT}}{\sqrt{WL}} \text{ in mV} \]

The mean variation can be reduced to zero, The s. d. is prop to the square root of charges
CMOS matching

\[ \sigma_{\Delta VT} (\text{mV}) \]

0.5 \( \mu \text{m} \) NMOS
0.18 \( \mu \text{m} \) NMOS
90 nm NMOS
65 nm NMOS

\[ \sigma_{VT} = \frac{A_{VT}}{\sqrt{WL}} \text{ in mV} \]

Ref: M. Pelgrom IEEE JSSC 1989 p. 1433
Matching: CMOS 90nm, W/L=10/5

V_p

V_n

V_n

V_p

1.5 volt

10 μA

(typ, snsp, snfp, fnsp, fnfp)
Matching: CMOS 90nm, W/L=1/0.5
Matching: CMOS 90nm, W/L=0.2/0.1
Global and local variation:

Differential design:

\[ \Delta V_{out} = 0 \]

\[ \Delta V_{T1} = 100 \text{ mV} \]
\[ \Delta V_{T2} = 100 \text{ mV} \]

\[ \Delta V_{out} > 0 \]

\[ \Delta V_{T1} = +1 \text{ mV} \]
\[ \Delta V_{T2} = -1 \text{ mV} \]

Just increasing the parameter window is no option!
Present approach to statistical sim:

Global variations:
- worst-best case, or
- use random point in parameter space

Local variations:
- \( \sigma_{VT} = \frac{A_{VT}}{\sqrt{WL}} \) relates process and size to distribution
- determine per component a unique set of parameters
- run in Monte Carlo mode.

Global and local variations can be used independently
Example:

Differential design:

- y1-axis -

DB($V_{\text{common}}$) -10.0

DB($V_{\text{diff}}$) -20.0

VDD

Analysis: ACSTAT

Substrate noise

Date: Sept 14, 2006 Behavioral Modeling And Simulation Conference 2006
Prediction of bandgap:

Prediction of matching in CMOS is good (s.d. within 5-10%)
Yield vs. comparator mismatch

Probability that all $2^{N-1}$ transitions are monotonic

Yield

0% 20% 40% 60% 80% 100%

Standard deviation of comparator s.d. voltage

0 mV 1 mV 2 mV 4 mV 6 mV

Ref: M. Pelgrom, IEEE J SSC 1994, p. 879
Improving performance

Differential linearity errors in 10-bit CMOS ADC, before and after fine tuning (measured).
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Statistical analog design

1985 design:
- Auto-zero techniques
- Dynamic element matching

1985 simulation:
Simulate with offset sources on transistor level
Statistical analog design

Auto-zeroing comparator

Removes offset at the input, loses time
Averaging out current sources mismatch. THD < -95dB possible
Output currents have to be filtered by RC.
Statistical analog design

1985:
- Auto-zero techniques
- Dynamic element matching

1985:
- Simulate with offset sources on transistor level

1995:
- Sub-block techniques
- Data-weighted averaging
- Averaging inputs

1995:
- Statistical models and Monte-Carlo, digital control treated as analog circuit
Resistors add the input signal linearly, while the comparator mismatch adds with sqrt.

Ref: Kattmann, K. and Barrow,
Statistical analog design

Data weighted averaging

Digital to analog conversion:
Statistical analog design

1985:
- Auto-zero techniques
- Dynamic element matching

1985:
Simulate with offset sources on transistor level

1995:
- Sub-block techniques
- Data-weighted averaging
- Averaging inputs

1995:
Statistical models and Monte-Carlo, digital control treated as analog circuit

2005:
- (Sub)-system cancellation
- Error calibration

2005:
Need for advanced mixed-level and mixed mode
Statistical analog design

Coarse ADC
n bits

DAC

Σ

Fine ADC
N-n bits

DECODER

Correction

Digital analysis

Input

N bits

Digital analysis

\(\Sigma\)

Digital analysis

out

in
Present status in analog:

• Analog designers tackle statistical problems on a sub-system level for optimum performance

• These methods involve signal processing of increasing (digital) complexity.

• Co-Simulation in various domains (digital, “MatLab”, extracted lay-out and transistor level) is needed.

• Statistical simulation with Monte-Carlo is no longer acceptable: too time consuming and does not trace the real corner cases.
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Transistor mismatch dominates thermal noise:
- Major issue in many analog components
- Starts bothering digital designers

\[
\sigma_{\Delta V\text{T}} = \frac{A_{V\text{T}}}{\sqrt{W \times L}}, \quad C_{\text{gate}} = WLC_{\text{ox}}
\]

\[
E_{\text{gate}} = C_{\text{gate}} \times \sigma_{\Delta V\text{T}}^2 = C_{\text{ox}} A_{V\text{T}}^2 \approx 100 \text{ kT}
\]
SRAM 6T cell

Current drive must be sufficient to retain data during read and avoid flipping due to BL pre-charge level.

Cell must allow a write operation by a low bit line
SRAM has mismatch problems

In SRAM 6T cells Static Noise Margin: size of “eye” defines robustness

Date: Sept 14, 2006
Behavioral Modeling And Simulation Conference 2006
SRAM static noise margin “32nm”

1000 trials, nominal conditions, predicted $A_{VT}$
SRAM moving to 7, 8, 10 transistor cell

Ref: B. Calhoun, MIT, ISSCC2006
Timing getting worse for new generations.

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<th>0.25 μm</th>
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<th>0.13 μm</th>
<th>90 nm</th>
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<td>16 ps</td>
<td>21 ps</td>
<td>38 ps</td>
<td>68 ps</td>
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Statistics in digital design

• The first digital paradigms (6T cell) are under discussion due to the statistical challenge.

• More trouble to follow (statistical timing).

• In contrast to analog there is little room to escape in digital.

• How to maintain the digital abstraction without sacrificing too much area/power/performance?

• Digital circuits go analog! Will digital simulation also go analog?
Variability: What to do?

Actual values from stochastic distributions cannot be predicted.

Circumstances (temp, voltage, process corner) can be measured

More optimum setting can then be achieved

Measuring of analog parameters in VLSI ICs
Signal Integrity Architecture

Petrescu, Pelgrom, Veendrick et al, ISSCC 2006
Silicon

Four identical functional cores
  A: No decap
  B: Half decap
  C: Nominal decap 500pF
  D: Double decap

In 90nm CMOS process
Measurements Results

![Graph showing min Vdd (V) vs. Activity for different DECAP configurations (no, half, nominal, double).]
65 nm test chip

[Image of a 65 nm test chip with labeled components: interface, Processor, Mem, and sist.]
Measurement Results
65 nm

Petrescu, Pelgrom et al.
ESSCIRC 2006

Date: Sept 14, 2006
Outlook

Variability is one of the main design-technological problems in deep sub micron technology.

• Most effects are understood and can be addressed either by design rule or by statistical analysis.

• Statistical design will become dominant over best-worst case practices.

• Digital and analog design come together on circuit but also on block level.

• Still a lot of challenge ahead!
Conclusion

• In the nanometer era the atomic scale is reached: this inevitably leads to statistics dominating the behaviour of components.

• In analog design statistics are part of the design process.

• The CAD tools to support the analog circuit solutions are unavailable or immature.

• Digital designers rapidly find themselves in trouble facing the same issues.

• Solutions on circuit and CAD level will borrow from analog methodologies.