System Design Oriented RF Block Modeling : When Top-Down Reaches Bottom-Up

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ABSTRACT

This paper deals with a new RF block model implementation dedicated to the design of complex Systems on Chip. The hierarchical library have been developed with simulators that can be used in a single design platform, which ensure a unique simulation environment and a full interoperability between the models. This is the first step in the development of a complete hierarchical models solution that can be compared to the SPICE MOS models ranging from level1 to BSIM.

Keywords

RF system design, hierarchical modeling

1. INTRODUCTION

Actual RF system design method is composed of a combination of top-down and bottom-up design considerations. Each design team follows its own methodology, depending on the RF system which has to be designed and also on existing design (reuse). At this time, it is still not clear whether a design method is chosen because of its efficiency or because reuse can be done easily. To further understand this problem, let us consider separately top-down and bottom-up approaches.

The standard bottom-up design starts from the technology choice, and goes up to the block design such as low noise amplifier (LNA), voltage controlled oscillator (VCO), power amplifier (PA) or mixer. Another part of bottom-up approach is the IP reuse ; from known block architecture, it is possible to choose an optimal topology with minimal changes from existing designs, which lowers development time. Finally, system designers use high level and/or hierarchical modeling to check the system specifications. On the other hand, top down approach starts from system level specifications, such as BER or power consumption and block specifications (gain, third order intercept point, compression point at 1 dB, noise figure, ...), are defined to meet system level requirements. Then, the RF blocks are designed in order to respect their specifications. A classical method is presented in figure 1.

From this short overview, it becomes clear that there is no universal solution for moving easily from block level design to system level design. In other words, we reach the limit of the classical hierarchical modeling. Indeed, at this moment it is possible to have IP hierarchical library, however it takes quite some time in order or replace a block model with another one : checking compatibility (the electrical input and output ports must remain the same at each level), or evaluating block specifications for the design architecture and the corresponding physical parameters (component sizes).

It is also very important to keep as much as possible the same design environment for bottom-up design, as this can save development time. For the same reason, co-simulation, which could be very helpful for the first design steps, should be avoided. Some solutions already exist to ensure a single design environment. For example, Matlab and Simulink, used for high level modeling, are compatible with Mentor Graphics' design flow. This requires that the high level are compiled into VHDL code (with C code as architecture) and are used as black box in ADVance MS [1].

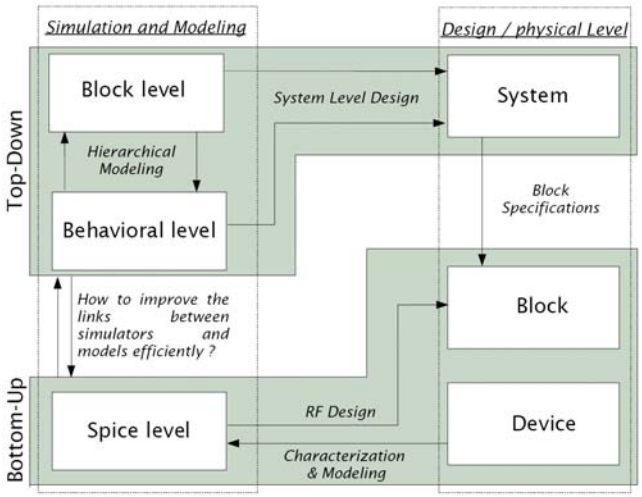

Figure 1 : Design method overview

What we propose in this paper is to develop a simulation interface linking bottom-up and top-down designs based on design and modeling considerations. This aims at improving the system design method efficiency. To do so, we consider a 2.4GHz transmitter [2] and a 2.4 GHz LNA as system and block design basis. In the second part, we give an overview of design needs and modeling capabilities. In the third part, we propose a solution for unifying models and design methods for RF system design. Finally, the last part shows the corresponding results.

2.DESIGN AND MODELING CONSIDERATIONS

This section gives a short state of the art about system design needs and hierarchical modeling capabilities. This will serve as a basis for the method proposed in section 3.

2.1 Modeling capabilities

IP hierarchical RF models already exist and have been developed using behavioral, block level and SPICE description or a mix of the above. However, the main issue is that the input parameters are different for each description level. For example, SPICE uses technology parameters such as transistors width and length and inductors width, spacing, diameter and number of turns, while behavioral and block-level models are based on electrical parameters : voltage or power gain, third order intercept point, noise figure, input and output matching. On top of that, most of the RF blocks are modeled as two-port devices while SPICE level circuits are four-ports devices if we consider the V_{DD} and V_{SS} power supplies ports. For theses reasons, it makes it hard to develop efficient models for such parameters as power consumption. Indeed, for this latter, it is clear that high level modeling requires a lower level analysis.

The natural question that arises is then : "How to link the hierarchical models efficiently ?". To answer this, one should carefully consider the following design considerations.

2.2 Design requirements

To reduce simulation time and thus to quickly get efficient results for feasibility study, system design requires high level block modeling. The input parameters for these blocks are the electrical specifications such as gain or IP3. High level or block-level modeling will then be used.

Based on these simulations, system designers will provide the block specifications to RF designers. Then starts the bottom-up procedure when one has to find the ad hoc IP that will be reused. Actually, some parameters of interests, such as power consumption are available only after SPICE simulations, which is quite inconvenient. This method, sometimes referred to as "V method" [3] is the one which is the most usual for the design flow. The main issue with this methodology is that it often takes quite some time to get block-design feedback once the system design is done.

A solution to mix bottom-up and top-down methodologies has been proposed in [4], where the bottom-up verification is ensured *de facto* thanks to the design optimization. The modeling and simulation methodology we propose uses the link between Simulink and ADVance MS to have access to low level parameters with high level simulations in order to reuse existing RF blocks models and improve the optimization phase.

3.SIMULATION AND MODELING UNIFICATION FOR RF BLOCKS

The method we propose is based on hierarchical plug-and-play models. As a consequence, lower level sub-systems models can be called at system level simulation without any change in the testbench and other simulation files. To do so the first requirement is the interoperability of the hierarchical description levels into a unique simulation platform. For this purpose, block-level models can be compiled into C code, implemented into VHDL blocks, and that can be used as a black box with behavioral description language. Then, it is important to allow system level designers to have access to technology and electrical parameters.

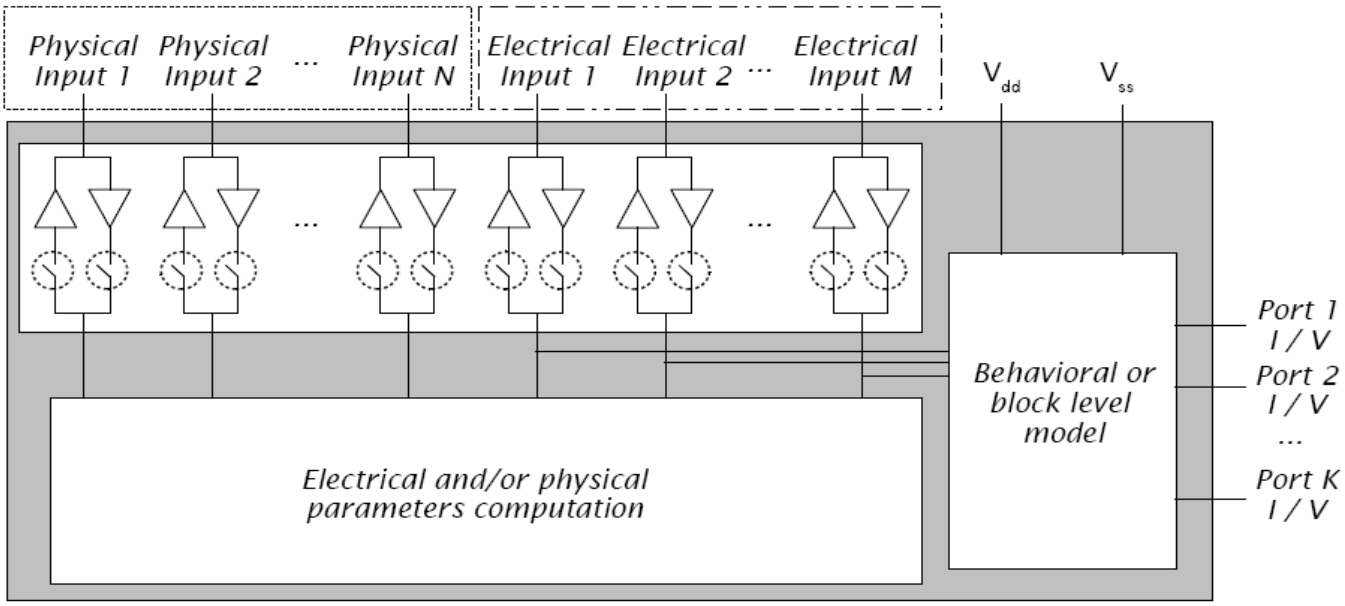

Figure 2 : Model architecture

The solution we propose is to start from an exhaustive study of existing RF blocks. The model architecture is proposed in figure 2.

The electrical parameters used for high level modeling are extracted with SPICE parametric simulations for some variations on the corresponding physical parameters. Then, the results can be either stored in a lookup table/equations or some trends can be extracted for characteristic parameters, such as gain versus inductances and transistor sizes. In case a trend line based model is developed, additional functionalities such as call back can be added.

In these conditions, it is possible to develop some links between SPICE results and block and/or behavioral models without developing new model architecture. This is shown in figure 3.

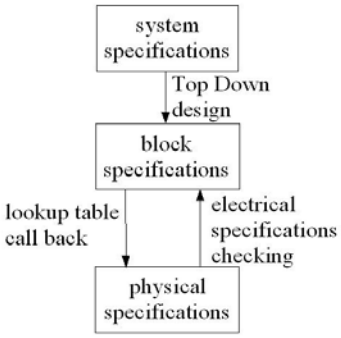

Figure 3 : Interactions between block and physical specifications

We start from an existing behavioral model which has the same electrical inputs and outputs as SPICE circuit. Most particularly, the power supplies must be taken into account. This model already has electrical parameters in input, and adding extra physical parameters can be of interest. Then each electrical or physical parameter can be considered as an input or an output depending on user-define priorities. The point is that whatever the status of these parameters in the new description, the electrical parameters must remain the behavioral or block-level model inputs. This creates a link between SPICE simulations and higher level modeling.

The way we propose to link the parameters is easy to implement and proves the method application. It can be implemented either at block or at behavioral description level. The first step is to define specifications with a corresponding priority. The specifications can be either on electrical or physical parameter. Then a program sparse the lookup table or any corresponding data file to restrict the other parameters values. After some few iterations, all the parameters values are determined. Moreover, in case simple equations can be extracted between physical and electrical parameters, it is possible to include these equations inside the model. This can easily be handled by inserting goal and optimization functions. The corresponding algorithm is described in figure 4.

The complete interaction is ensured by performing a call back on all the electrical parameters based on the physical ones, then the user can check if the performances obtained on low priority parameters are acceptable or not. If the result is not satisfactory, the user can change the specifications before running the simulation.

To make this more user-friendly, it is also possible to develop a graphical interface to show which parameters can still be varied [5]. One can compare this to a layout graphical interface, where the user can choose, to define a resistor in classical CAD environments, two parameters out of the width, number of squares and the resistance value,

Another problem that arises is to account for input and output impedance matching in “real-time”. Indeed, a need to change an electrical parameter results in a physical parameter variation which will in turn more or less mismatch the input and output impedances. In these conditions, other parameters have to be adjusted to keep the circuit matched. To account for this, input and output impedances are de facto set to higher priorities. Another solution is to remove all the parameters set which do not correspond to a given impedance matching (e. g. S_{11} < -20dB) from the look-up table.

It is important to note that this design step (specification definition) does not increase much the simulation time, since the parameter computation is done only once before the first simulation.

As a result, we get SPICE simulation accuracy in terms of electrical parameters as a function of physical parameters, and behavioral model performances for simulation time. In this way, pure co-simulation, which is usually very time consuming can be avoided.

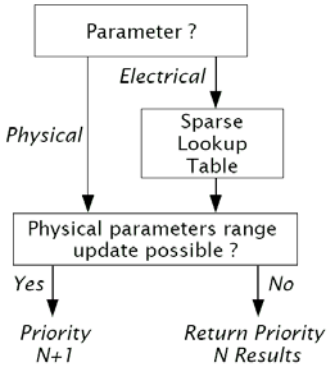

Figure 4 : parameters computation algorithm

Then should be raised the question of the development time. For one RF block, starting from SPICE simulation, the model development time is about one week. As counterpart, the exhaustive analysis has to be performed only once for a given architecture in a given technology and it therefore saves time for IP reuse study.

4.Results

We have applied this method to an LNA modeling for use in a transceiver system simulation. The LNA architecture of interest in presented in figure 5. The design platform we used is the ADVance MS environment, where the VHDL-AMS behavioral models are developed with ADMS, block-level models with Matlab and Simuling and SPICE description with Eldo. The link between Matlab, Simulink and ADVance MS is ensured by ADVance SME.

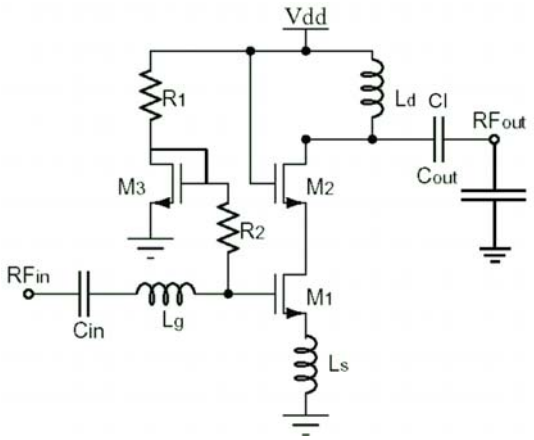

Figure 5 : LNA Architecture

The behavioral model [6] takes into account the power gain, IP3, CP, NF, input and output matching and power consumption (electrical parameters). Theses parameters are stored into a lookup table as a function of physical parameters : width over length ratio of each transistor and the inductances diameter (resulting in a an inductance change).

The comparison between SPICE simulations and behavioral models is given on figure 6 and the corresponding graphical user interface in figure 7. In our example, gain and IP3 are set to high priority, then transistor sizes are medium priority. After three iteration corresponding to the gain transistor 1 size and intercept point of the third order, all the electrical parameters are defined, and the corresponding NF and power consumption are computed from those specifications.

We can see that for the high priority parameters, SPICE and high level simulation results are very close to each other, which means that each model can be used without significant change for system-level simulations. In practice, high level model will be used during design exploration phase and SPICE simulation during for verification.

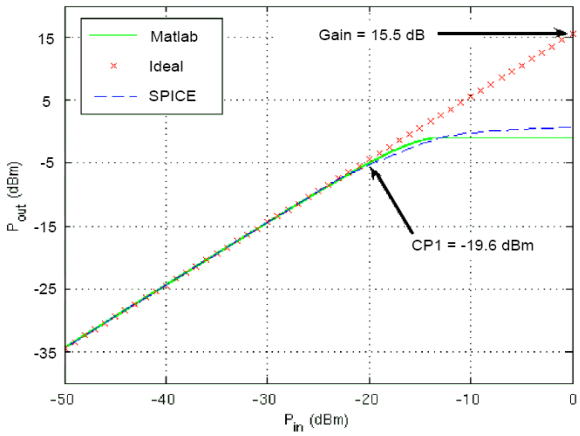

Figure 6 : gain and 1dB compression point

Finally, we include the LNA model in a complete 2.4 GHz transceiver described in figure 8. the system level simulation is first done using block-level models, but it is possible to replace each block by its corresponding lower-level description.

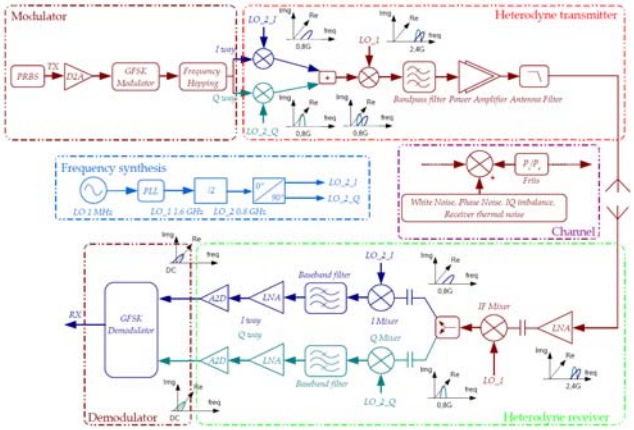

Figure 8 : Transceiver architecture

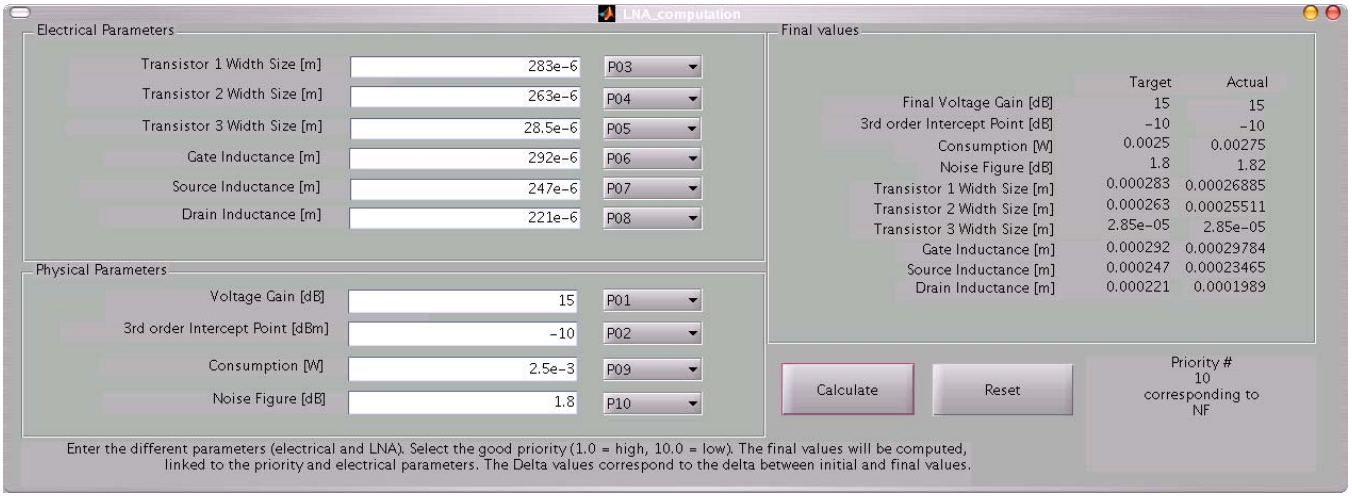

Figure 7 : Graphical User Interface

5. Conclusion

This study has shown a new system-level-oriented model architecture in order to develop the interoperability between the different hierarchical levels of RF blocks. The proposed method can be further investigated in order to develop an analytical optimization solution. The point would be to define equations for each block topology and propose a call back method for call-back (electrical to physical parameters computation), when one could make the comparison with BSIM-like models, where the transistors are modeled with physic-based equations in addition with some fitting factors and where RF blocks hierarchical models could be compared to the different SPICE levels for transistors.

6. ACKNOWLEDGMENTS

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