An Efficient Bottom-Up Extraction Approach to Build the Behavioral Model of Switched-Capacitor ΔΣ Modulator

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Abstract

In this paper, an efficient bottom-up extraction approach is proposed to build accurate behavioral model for the switched-capacitor (SC) delta-sigma (ΔΣ) modulator. In the special extraction mode, we can use several specific patterns to obtain the key circuit parameters of the design in a short time without separating it into several sub-blocks. Actual loading effects and parasites can be considered automatically, which makes our modeling approach become more suitable for existed IPs and flattened post-layout designs. In the experiments, the comparison results between our behavioral model and HSPICE simulation have demonstrated the accuracy and efficiency of the proposed modeling strategy.

1. Introduction

Analog mixed-signal (AMS) design is more and more popular in current System-on-Chip (SOC) era. Traditional mixed-signal design procedure is to divide a system into digital and analog parts. These two parts are often designed in isolation due to different design approaches. Finally, the two parts are integrated at layout level and analyzed by transistor-level simulations to check the entire system performance. If the analysis results violate initial specifications, designers have to adjust the circuits and repeat the entire design procedure. Such kind of bug-fixing iterations are very time-consuming, especially for large systems. In order to reduce the iteration time, design reuse and IP-based design methodology are very popular methods. However, transistor-level simulations may still be required in system integration because the protected IPs often appear as layout forms, especially those analog IPs.

One of the popular ways to solve these integration issues is building the behavioral models for both digital and analog circuits and performing system simulation at behavioral level. In general, behavioral models describe the circuit functions using hardware description language (HDL), such as Verilog, VHDL (for digital circuits), Verilog-A [1-3] (for analog circuits), MATLAB SIMULINK, etc. Using those behavioral models, whole chip simulation can be finished in a short time, which enables complete checks on the system functionality after integration. They also enable the designers to verify the integrated system at higher levels instead of layout level such that the design iterations can be reduced.

In the literature, there are a lot of researches on building behavioral models for switched-capacitor (SC) delta-sigma (ΔΣ) modulator [4-9]. According to the specifications, designers can use Simulink/Matlab or analog HDL to describe the mathematic formulas of analog circuits and simulate the possible results. In other words, using this kind of behavior models helps designers estimate the final results much faster before implementation. Therefore, such kind of top-down modeling approach is helpful for circuit designers when they are building their new designs.

However, without the help from original designers, it is hard to understand the flattened designs and protected IPs. Some subtle properties, such as timing information and parasitic effects, are hard to be modeled in the top-down approach due to the lack of layout information. Therefore, for IP-based designs, bottom-up extraction approach that builds the models from low-level simulation results may be a better way to obtain accurate behavioral models for existing designs. Figure 1 illustrates the typical bottom-up behavioral modeling flow for existing designs.

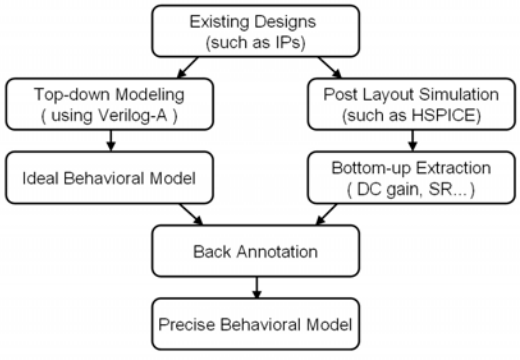

Figure 1. Bottom-Up Modeling Flow for Existing Designs

In this paper, we focus on building accurate behavioral models for existing second-order SC ΔΣ modulator. Firstly, we use Verilog-A to describe the function of each sub-block in the modulator and build an ideal behavioral model. Secondly, we will use several specific patterns to obtain the non-ideal effects of the design from transistor-level simulations. During the extraction procedure, we switch the ΔΣ modulator to a

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special extraction mode instead of separating it to several sub-circuits. It can help us to avoid tracing a flattened netlist with numerous parasitic capacitors. The parasites and actual loading effects can also be included automatically using this approach. Finally, these non-ideal parameters are annotated into the ideal behavioral model to generate a precise behavioral model with non-ideal effects.

The rest of this paper is organized as follows. In Section 2, we will briefly introduce typical second-order SC ΔΣ modulators and the ideal behavioral model of each block in the modulators. The bottom-up extraction approach for the non-ideal effects is presented in Section 3. In Section 4, we will compare our behavioral model with HSPICE to demonstrate the accuracy and efficiency of our approach. Finally, some conclusions are made in Section 5.

2. Second-Order SC ΔΣ Modulator

SC ΔΣ modulators are applied widely in mixed-signal integrated circuits due to several advantages, such as achieving high performance with low sensitivity to analog component imperfections, inherent linearity, robust analog implementation, noise shaping nature and so on [4-11]. In this paper, we focus on the second-order SC ΔΣ modulators, which its block diagram is illustrated in Figure 2. In the following subsections, we will briefly introduce the each sub-block of the modulator and its ideal behavioral model.

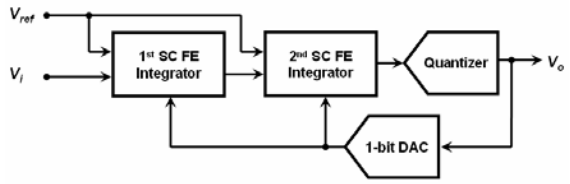

Figure 2. Second-Order SC ΔΣ Modulator

2.1 SC FE Integrator

The operation principle of SC Forward-Euler (FE) integrator can be generally classified the sampling and integration mode. In real circuit, the input and output of the integrator is full differential. However, for simplicity explanation, we adopt the single-ended configuration, as shown in Figure 3, where V_{ref} and V_i are the reference and input voltages, C_1 and C_2 are the sampling and integration capacitors, A_o is the finite OP gain, Φ_1 ,Φ_2 and Φ_{ref} stand for clock control signal. Generally, the signal phase of Φ_1 and Φ_2 is non-overlapped and complementary. The phase of Φ_{ref} is the same as Φ_2, which is generated by 1-bit DAC. We assume that A_o is infinite for the ideal behavioral model of SC FE integrator.

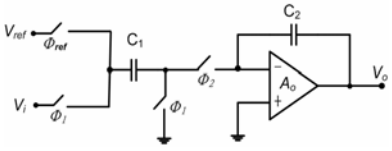

Figure 3. Single-ended Configuration of SC FE Integrator

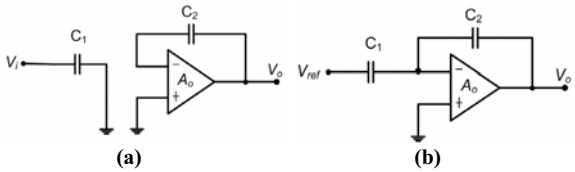

Figure 4. Operation Mode (a) Sampling (b) Integration

When Φ_1 is on and Φ_2 is off, the integrator operates in sampling mode as shown in Figure 5(a). During sampling mode, the voltage V_i is sampled to C_1 which stores the charge $Q_1=C_1V_i$. Then, when Φ_1 is off and Φ_2 is on, the integrator is controlled in integration mode, as shown in Figure 4(b). At this moment, the voltage V_{ref} will be injected into C_1 and adjusts Q_1. Simultaneously, the adjusted charge $Q_1'=C_1(V_i-V_{ref})$ will be translated to C_2. According to above the process of charge translation, we use equation 1 to describe the behavior of integrator in time domain. In order to reduce the complexity of building behavior model, we transfer time-domain to z-domain, as shown in equation 2. Finally, we represent equation 2 by Verilog-A language to model the SC FE integrator.

$$C_1 \cdot [V_i(t_n + \frac{T_s}{2}) - V_{ref}(t_n + \frac{T_s}{2})] = C_2 \cdot [V_o(t_n + \frac{T_s}{2}) - V_o(t_n - \frac{T_s}{2})] \quad (1)$$

$$V_o(z) = \frac{C_1}{C_2} \frac{1}{1 - z^{-1}} [V_i(z) - V_{ref}(z)] \quad (2)$$

2.2 Quantizer and 1-bit DAC

The structure of quantizer and 1-bit DAC is shown in Figure 5(a) and Figure 5(b) respectively. Basically, the quantizer is used to transform analog signal to digital signal. Firstly, the differential-pair output signal of 2nd SC FE integrator is sent to the input of comparator. If $V_+ > V_-$, the output of comparator is set to 1; otherwise, it is set 0. Secondly, D-latch transfers the output of comparator to the output of quantizer. Finally, the output of quantizer decides that Φ_2 be sent to Φ_{ref+} or Φ_{ref-}. If V_o is 1, then $\Phi_2 = \Phi_{ref+}$; otherwise, $\Phi_2 = \Phi_{ref+}$.

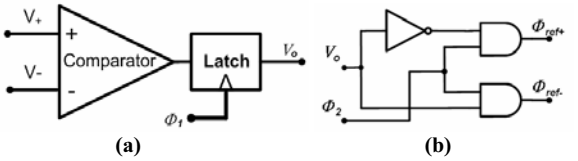

Figure 5. Schematic Circuit (a) Quantizer (b) 1-bit DAC

3. The Bottom-up Extraction Flow

In [4-11], several non-ideal effects of second-order SC ΔΣ modulator are discussed, such as the finite DC gain, DC-level offset, slew rate (SR), finite bandwidth, switch thermal noise. Many researchers aim at these non-ideal effects to propose their modeling approaches for the behavioral model of ΔΣ modulator [4-9]. However, these approaches can not be suited for existing IP designs due to more complex non-ideal properties, such as parasites and

actual loading effects. These effects are hard to be modeled in top-down approach. Hence, we propose the bottom-up extraction flow to overcome them, as shown in Figure 6. In the following subsection, we will introduce the overall extraction flow in detail.

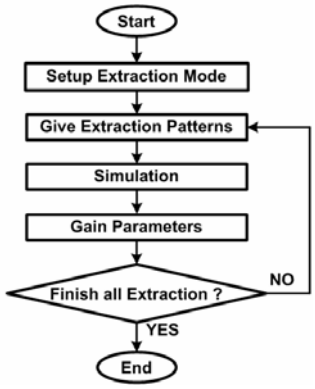

Figure 6. Our Bottom-Up Extraction Flow

3.1 Extraction Mode

In our bottom-up extraction flow, we firstly switch the modulator to extraction mode instead of separating it into several sub-circuits. It can help us to conveniently give the specific patterns for extracting some key parameters of non-ideal effects. Moreover, the parameters automatically include some complex non-ideal effects between each sub-block, such as parasites and loading effects. Figure 7 illustrates our extraction mode. The feedback loop between SC FE integrator and 1-bit DAC is broke. Finally, we control Φ_1, Φ_2 and Φ_{ref} signal to operate the integrator in integration mode.

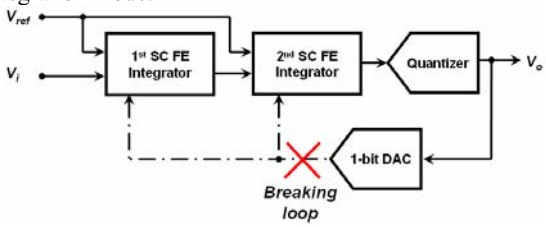

Figure 7. Extraction Mode of Second-Order SC ΔΣ modulator

3.2 Extraction Pattern

We give some specific patterns to extract our required parameters. Our specific patterns are shown in Figure 8, where V_{ref_+} and V_{ref_-} are the differential input of integrator, V_{comm} stands for the common voltage, ΔV stands for the arbitrary voltage, V_{o_+} and V_{o_-} are the output of integrator. We will give three groups of extraction pattern to gain our all required parameters, such as V_1 for finite DC gain, DC-level offset and SR_1, V_2 for SR_2, V_3 for the maximum value of SR, finite bandwidth and switch delay. These parameters can be easily measured from the timing output response of SC integrator. In this paper, we will only focus on the non-ideal effects of SC integrator for our developed behavioral model because it seriously affects the performance of ΔΣ modulator [4-11].

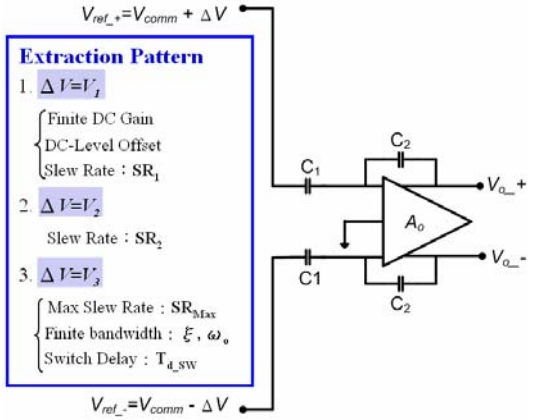

Figure 8. Extraction Pattern

3.3 Key Parameters of Non-ideal Effect

In this subsection, we will discuss the non-ideal effects of SC integrator and explain how to extract all key parameters. Please notice that our behavioral model is not required the information of device parameters.

3.3.1 Finite DC Gain

DC gain of an ideal integrator is equivalent to the ratio capacitor, $k=C_1/C_2$. Actually, due to the parasites and the mismatch of process manufacture, it still includes other parameters, such as the open-loop gain of operational amplifier, mismatch error of capacitor and so on. In [4-9], many complicated transfer functions of SC integrator with the finite DC gain effect are proposed. However, these complex parameters are not required extracting for our behavioral model with finite DC gain. We only give the extraction pattern V_1 to measure the actual ratio of output to input of existing SC integrator, k'. The ratio value represents actual DC gain. Hence, we still use equation 2 with k' instead of k to model SC integrator.

3.3.2 Settling Response

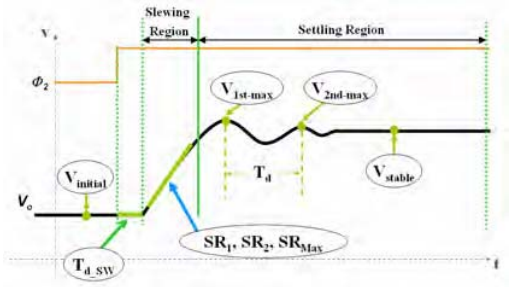

Figure 9. The Required Parameters of Settling Response

Settling response is consists of SR, finite bandwidth and switch delay. SR represents the variation slop of transient and the finite bandwidth causes the oscillated condition of initial stability voltage. They result in the non-

ideal transient response in each clock cycle. Switch delay stands for the delay time of transient behavior. In order to simplify explanation, we divide the settling response into two parts, slewing region and settling region, as shown in Figure 9. Next, we will explain our required parameters respectively, such as SR_1, SR_2 and SR_{Max} for SR, $V_{initial}$, $V_{1st\text{-}max}$, $V_{2nd\text{-}max}$, V_{stable} and T_d for finite bandwidth, T_{d_SW} for switch delay.

Slewing region is mainly represented by SR. Hence, we can only extract actual SR to model it. SR is caused by an operational amplifier. The various input voltage causes the various external branch current of operational amplifier. Moreover, SR can be represented by these branch current, as shown in equation 3. In order to dynamically exhibit the various SR, we use equation 4 to immediately calculate SR according to the sensitivity between the input voltages and SR. We use two groups of extraction pattern V_1, V_2 to gain SR_1 and SR_2. Finally, we will and limit SR to maximum value SR_{Max}, which be gained by the extraction pattern V_3.

$$SR = \frac{I_{out}}{C_L} = \frac{I - I_1}{C_L} = \frac{I - \frac{1}{2}\beta(V_{in} - V_{tp} - V_{tn})^2}{C_L} \tag{3}$$

$$\frac{SR_1 - SR_2}{SR_2 - SR_{in}} \approx \frac{V_1 - V_2}{V_2 - V_{in}} \Rightarrow SR_{in} \approx SR_2 - \frac{V_2 - V_{in}}{V_1 - V_2} \times (SR_1 - SR_2) \tag{4}$$

where I stands for a fixed current, β is manufacture parameter, V_{tp} and V_{tn} are threshold voltage, C_L is the output load capacitor, V_1 and V_2 are extraction patterns, SR_1 and SR_2 are two various SR.

In settling region, the finite bandwidth results in the oscillated waveform. As shown in equation 5, we use a standard second-order transfer function to describe this behavior. ξ and ω_0 are our required parameters and can be gained by equation 6 and equation 7 [12]. Similarly, we use the extraction pattern V_3 to gain the required timing information, such as $V_{initial}$, $V_{1st\text{-}max}$, $V_{2nd\text{-}max}$, V_{stable} and T_d. The timing information can be efficiently measured in underdamping case. However, when overdamping case occurs, the voltage $V_{2nd\text{-}max}$ is very approximate to V_{stable}. In this condition, we regard the difference in timing between $V_{1st\text{-}max}$ and V_{stable} as T_d for ω_0 and set ξ=1.

$$\frac{V_o(s)}{V_{in}(s)} = \frac{(C_1 / C_2) \cdot \omega_0^2}{s^2 + 2\xi\omega_0 s + \omega_0^2} \tag{5}$$

$$\xi = \frac{1}{2 \cdot \sqrt{\frac{\left(-\pi / \ln(OS\%)\right)^2 + 1}{4}}}, OS\% = \left(\frac{V_{max} - V_{stable}}{V_{stable} - V_{initial}}\right) \tag{6}$$

$$\omega_0 = \frac{2\pi}{T_d\sqrt{1-\xi^2}} \tag{7}$$

where ω_0 and ξ stand for pole frequency and damping ratio respectively, $OS\%$ is the overshoot percent, Q is the pole quality factor and $V_{max} = V_{1st\text{-}max} - V_{initial}$.

Switch delay is generated by switch circuit and can be represented by T_{d_SW}. Therefore, we use the extraction pattern V_3 to extract the difference in timing between the initial transient of Φ_2 and V_o. Finally, we combine the three type models to represent the complete behavior of settling response.

3.3.3 DC-Level Offset

DC-level offset is generated by the imperfection of operational amplifier and represents the difference in reference voltage between the ideal and actual. Generally, the reference voltage is equivalent to Vdd/2, where Vdd stands for the difference in supply voltage between positive and negative. Therefore, we will measure the actual center voltage of the differential output of SC integrator by the extraction pattern V_1. Finally, we add this offset voltage to the output of our model.

3.3.4 Switch Thermal Noise

Switch thermal noise is mainly caused by the random fluctuation of carries due to thermal energy of the switch circuit. In [4-11], it has been discussed in detail. We use the popular Gaussian random variation to model this effect. Equation 8 shows the total thermal noise power [5]. Finally, the noise signal will be add to the input of our model.

$$e_T^2 = \int_0^\infty \frac{4kTR_{on}}{1 + (2\pi 2\pi_{on} C_1)^2} df = \frac{kT}{C_1} \tag{8}$$

where k stands for Boltzmann's constant, T stands for the absolute temperature, and $4kTR_{on}$ is the noise PSD associated with the switch on-resistance.

4. Experimental Results

In this section, we use a second-order SC $\Delta\Sigma$ modulator to demonstrate the accuracy and efficiency of the proposed behavioral modeling approach. This modulator has been implemented in TSMC 0.25μm TT_3V CMOS process. Oversampling ratio (OSR), sampling frequency, and signal frequency are 303, 12.5 MHz and 20.6 KHz respectively. The behavioral model is described by Verilog-A language and the simulation environment is Cadence's Virtuoso (Analog Artist). The "wavescan" tool is used to show the timing waveform, calculate the Signal-to-Noise Ratio (SNR), and show the frequency-domain response after Fast Fourier Transform (FFT). While calculating the SNR, signal range is set from 19.073 KHz to 21.362 KHz. Noise range is set from 1.5259 KHz to 40.054 KHz, and the number of sampling point is 32768.

Referring to the previous researches [4-11], the non-ideal properties of SC integrator dominate the performance of $\Delta\Sigma$ modulator. Therefore, the accuracy of the integrator model is critical to the overall accuracy. Figure 10 shows the partial enlarged view of 1st integrator output waveform. The upper curve is obtained from the ideal behavioral model without slope and settling response. Using the extracted non-ideal parameters, the timing waveform generated by the behavioral model can become very similar

to the HSPICE results, as shown in the lower curve of Figure 10. The simulation time of such an accurate behavioral model is only 1490.97 seconds, while HSPICE simulation requires 123252 seconds.

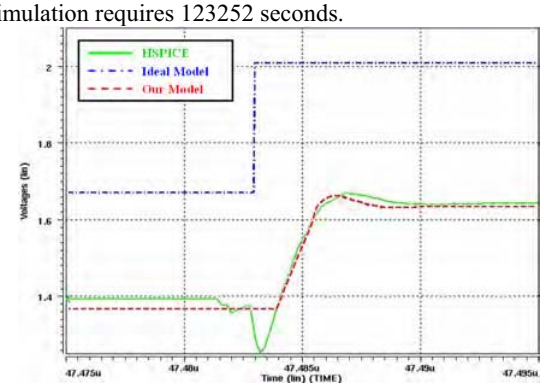

Figure 10. Output Timing Waveform of 1st Integrator

Next, we compare the frequency-domain response of our behavioral model and HSPICE simulation. The FFT results of the two waveforms are shown in Figure 11, which also show that our behavioral model can provide similar results as in HSPICE simulation using much less simulation time. The SNR of the waveform obtained from our behavioral model is 86.31 dB, while the SNR measured in HSPICE simulation is 85.62 dB. The two waveforms have only 0.69 dB difference in SNR values.

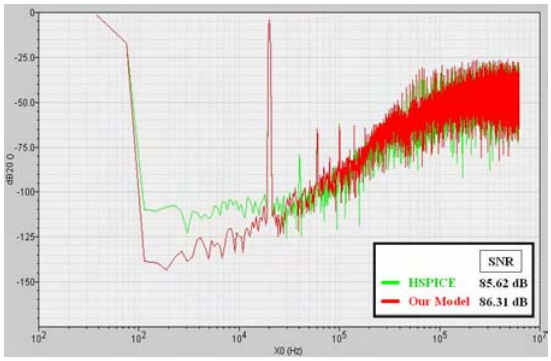

Figure 11. Frequency Domain (Our Model VS HSPICE)

5. Conclusions

An efficient bottom-up extraction approach to build accurate behavioral models for existing SC ΔΣ modulators is presented in this paper. In the special extraction mode, the non-ideal properties existed in real circuit can be easily measured by using several specific patterns. Since we do not separate the design into several sub-blocks, actual loading effects and parasites can be considered automatically without tedious layout tracing, which makes our modeling approach become more suitable for existed IPs and flattened post-layout designs. As shown in the experimental results, our behavioral model does provide similar results as in the HSPICE simulation, no matter in time domain or frequency domain. We believe that those results have demonstrated that our method is really an accurate and efficient modeling approach for existing designs.

6. References

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