An Efficient Bottom-Up Extraction Approach to Build the Behavioral Model of Switched-Capacitor ΔΣ Modulator

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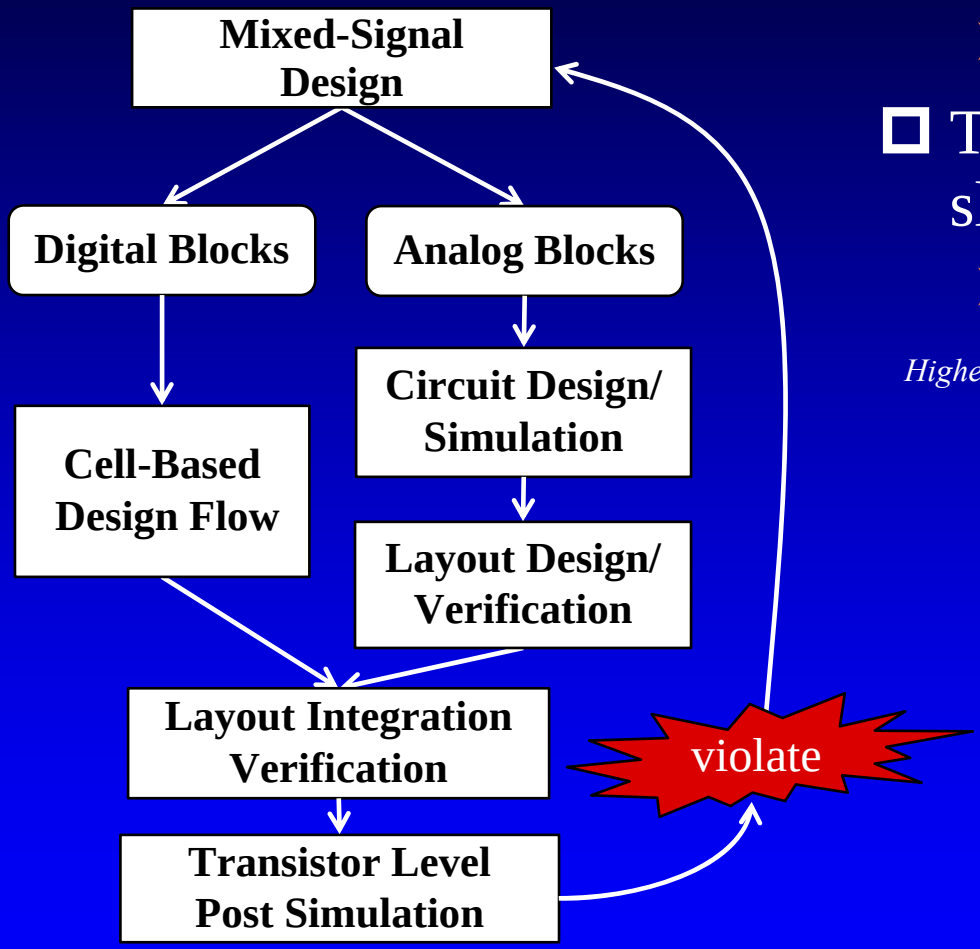
Outline

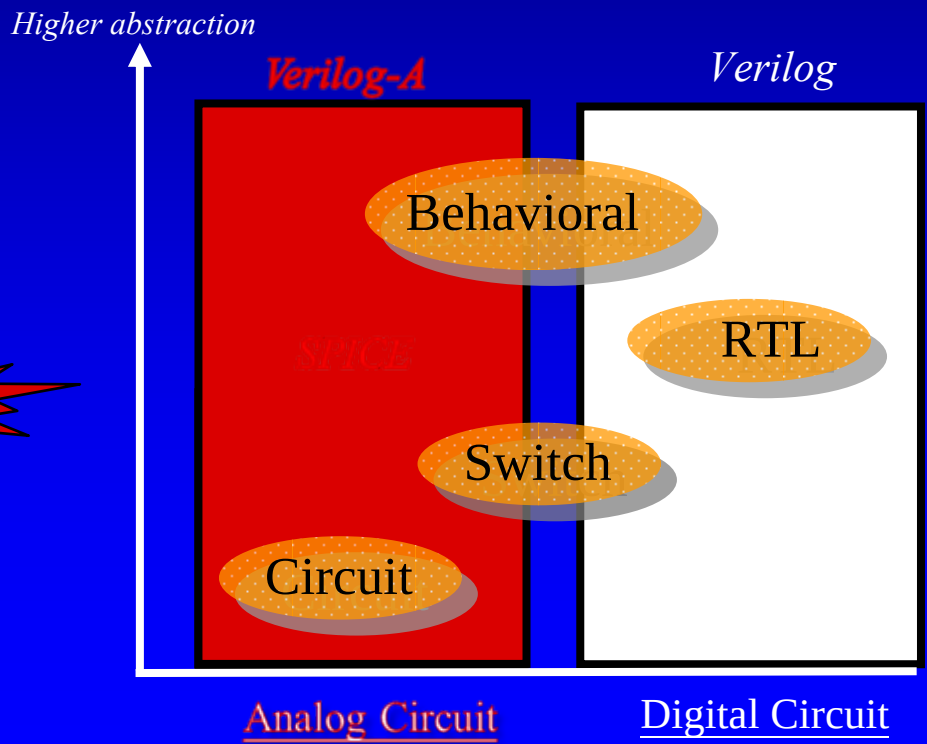
- Introduction
- Second-Order Delta-Sigma (ΔΣ) Modulator
- Our Bottom-Up Extraction Flow for Non-Ideal Effects
- Experimental Results
- Conclusions

Introduction



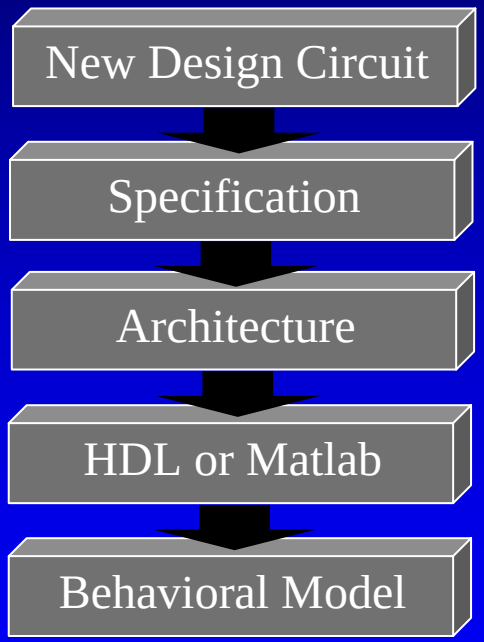
Conventional MS Design Flow

- Reduce iteration times
  - Reuse design and IP-Based design
- Transistor-level simulation is too slow
  - Behavior-level simulation

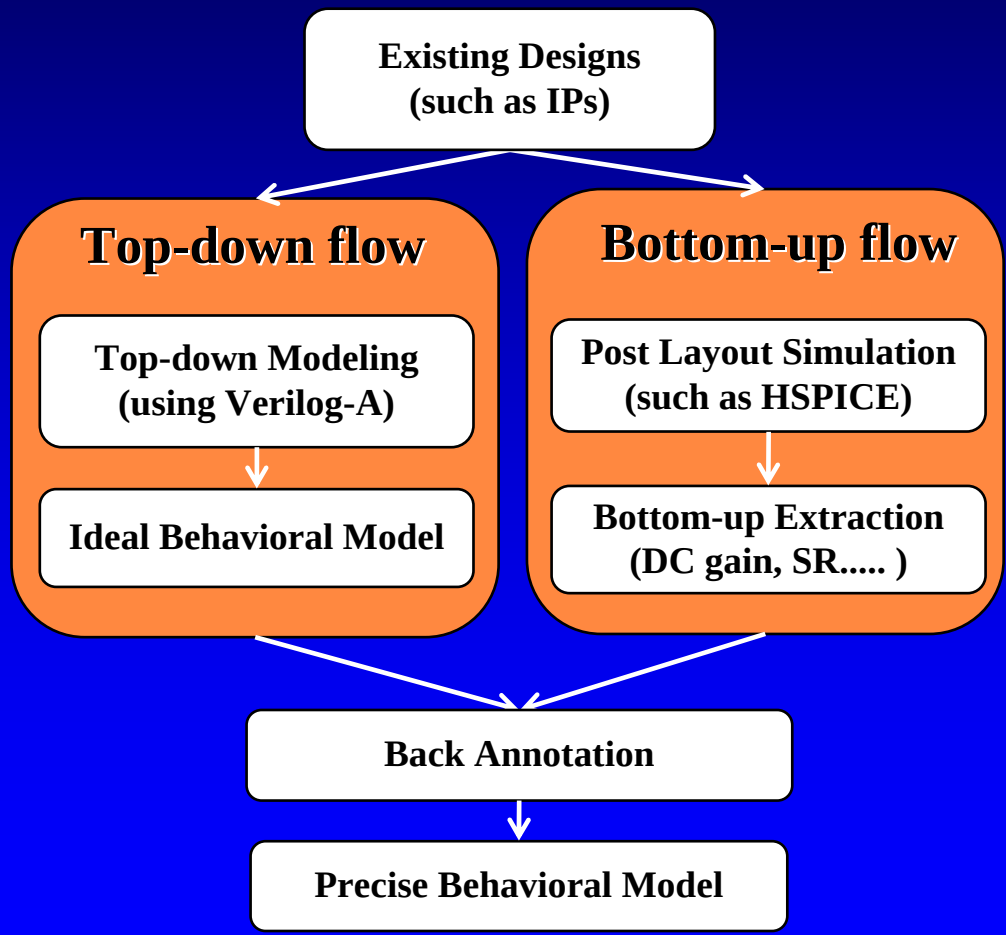


Our Bottom-Up Modeling Flow

- Top-Down Behavior Modeling
  - Not Suitable for IP designs



- Our Modeling flow
  - Suitable for IP designs

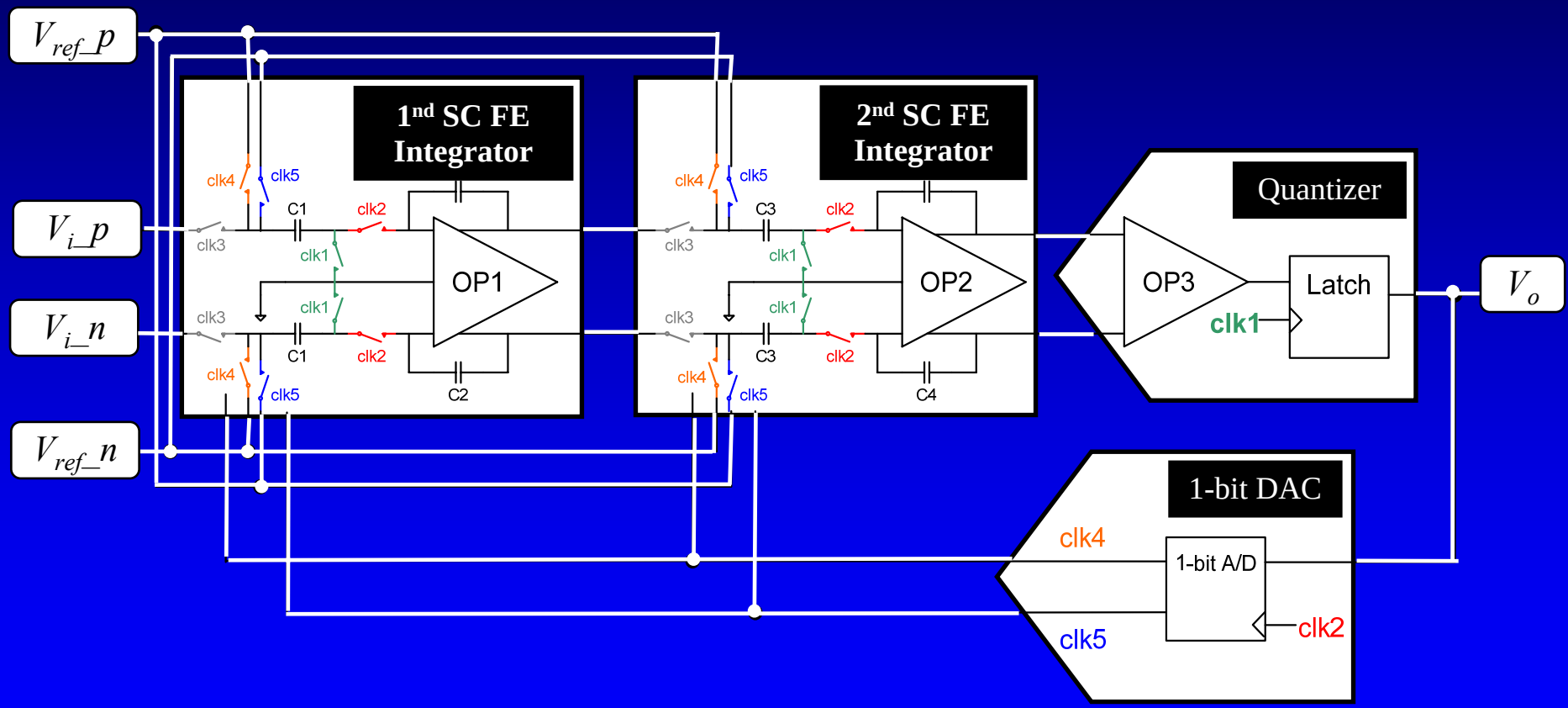


Outline

- Introduction
- Second-Order Delta-Sigma (ΔΣ) Modulator
  - Top-down Ideal Behavioral Model
- Our Bottom-Up Extraction Flow for Non-Ideal Effects
- Experimental Results
- Conclusions

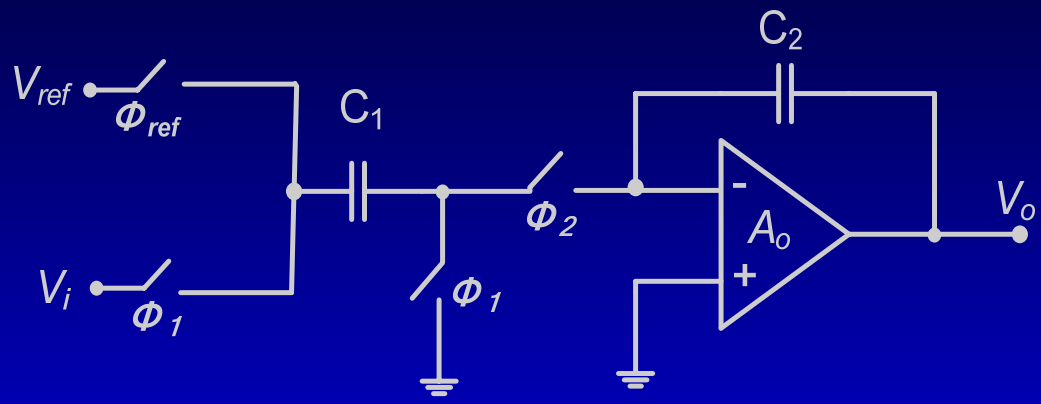
Second-Order SC ΔΣ Modulator

- Five clock signals to control this operation



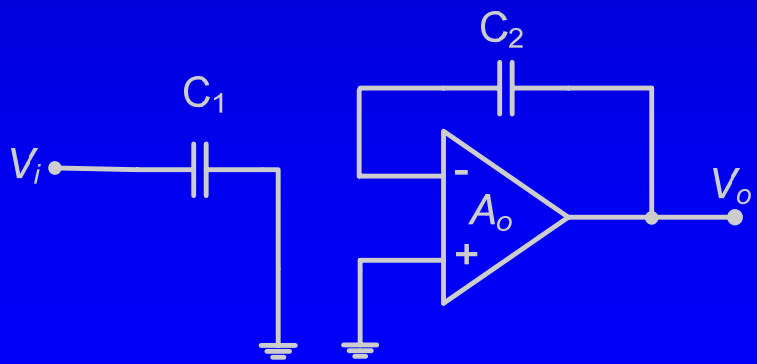
SC FE Integrator

Architecture



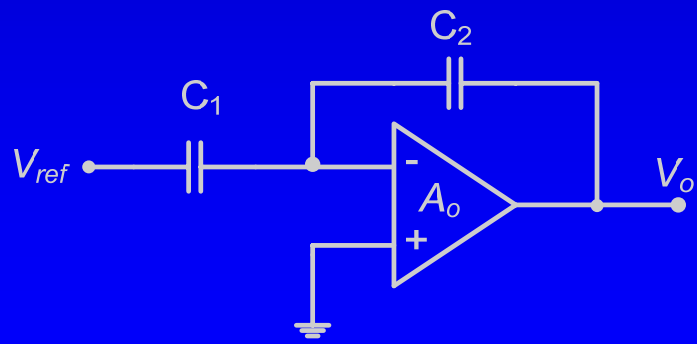
Sampling mode

- Φ_1 on ; Φ_2, Φ_{ref} off



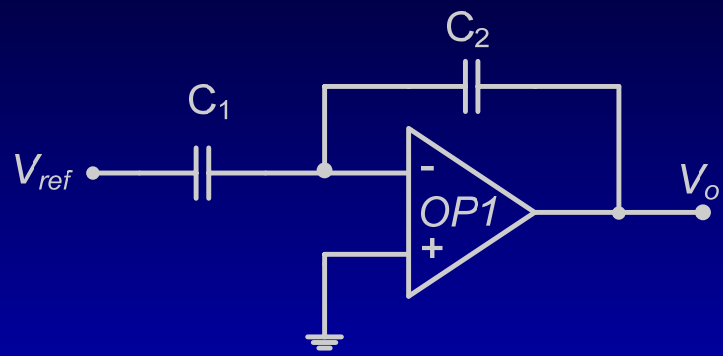
Integration mode

- Φ_1 off ; Φ_2, Φ_{ref} on



Ideal Behavioral Model

- SC Integrator
  - Integration mode



- Time-domain transfer function

$$C_1 \cdot V_i^o(t_n) - C_1 \cdot V_{ref}^e(t_n + \frac{T}{2}) = C_2 \cdot [V_1^e(t_n + \frac{T}{2}) - V_1^o(t_n)]$$

$$C_1 \cdot V_i^e(t_n + \frac{T}{2}) - C_1 \cdot V_{ref}^e(t_n + \frac{T}{2}) = C_2 \cdot [V_1^e(t_n + \frac{T}{2}) - V_1^e(t_n - \frac{T}{2})]$$

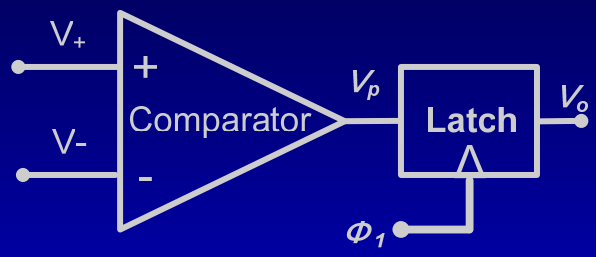
- Z-domain transfer function

$$C_1 V_i^e(z) - C_1 V_{ref}^e(z) = C_2(1 - z^{-1}) V_1^e(z)$$

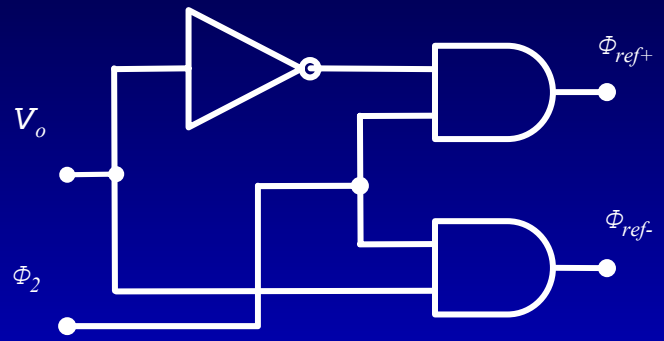
$$V_1^e(z) = \frac{C_1}{C_2} \frac{1}{1 - z^{-1}} \left[V_{in}^e(z) - V_{out}^e(z) \right]$$

Other Circuit Blocks

Quantizer



1-bit DAC



Circuit behavior

Comparator

If $V_+ > V_-$, $V_p = V_H$,

else $V_p = V_L$

Latch

If Φ_1 on , $V_o = V_p$,

else $V_o = V_o$

If Φ_2 on , $\Phi_{ref+} = \sim V_o$, $\Phi_{ref-} = V_o$

else $\Phi_{ref+} = 0$, $\Phi_{ref-} = 0$

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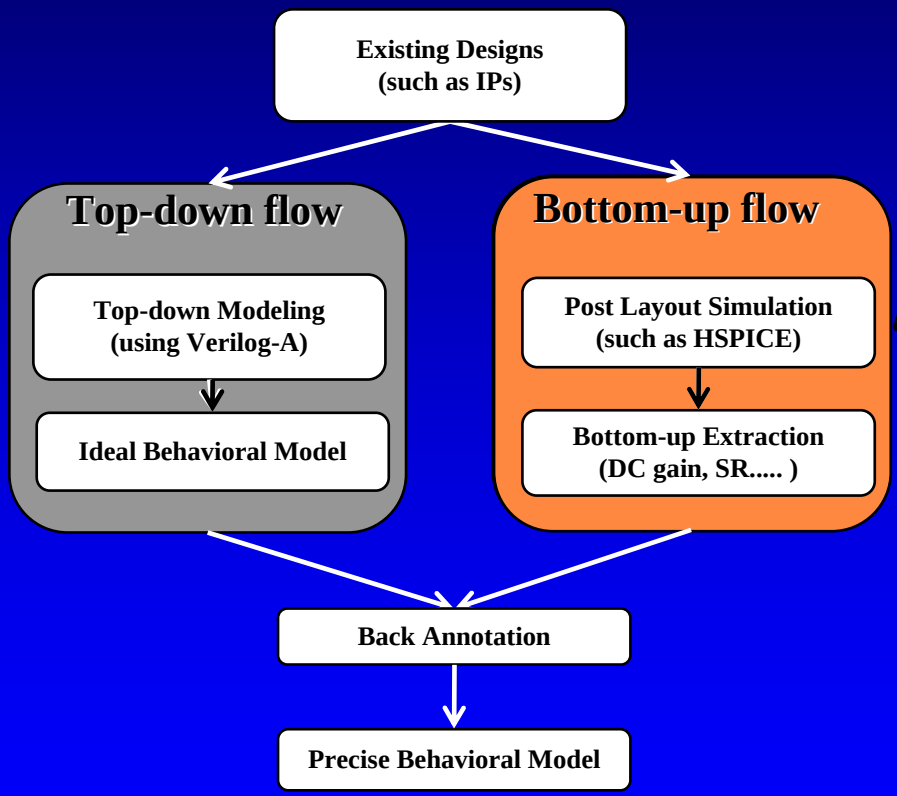
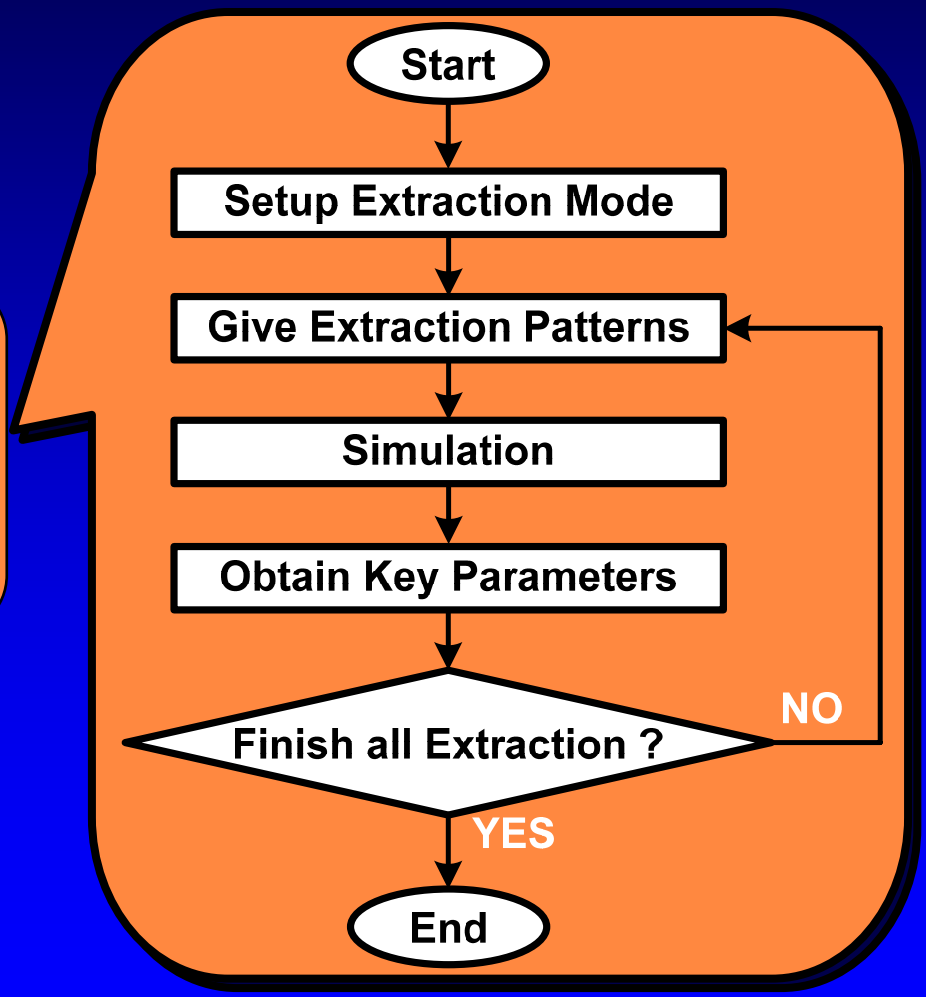
- Introduction
- Second-Order Delta-Sigma (ΔΣ) Modulator
- Our Bottom-Up Extraction Flow for Non-Ideal Effects
  - Extraction Flow
  - Finite DC Gain & DC-Level Offset
  - Settling Response
  - Switch Thermal Noise
- Experimental Results
- Conclusions

Our Bottom-Up Extraction Flow

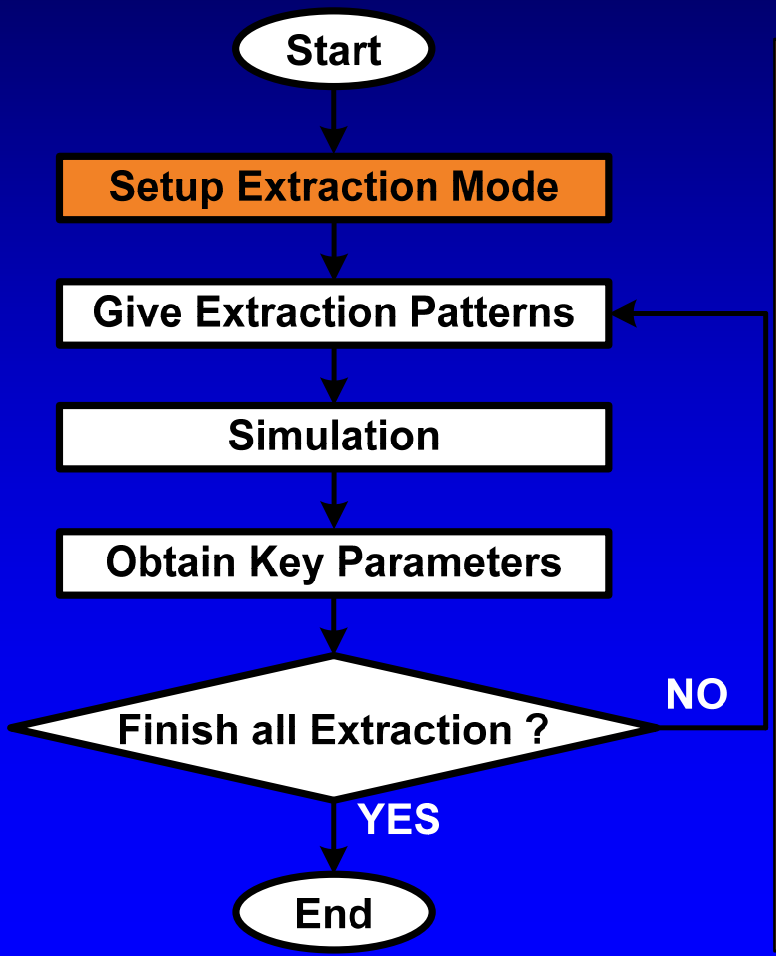
- Execute the bottom-up extraction flow for non-ideal effects

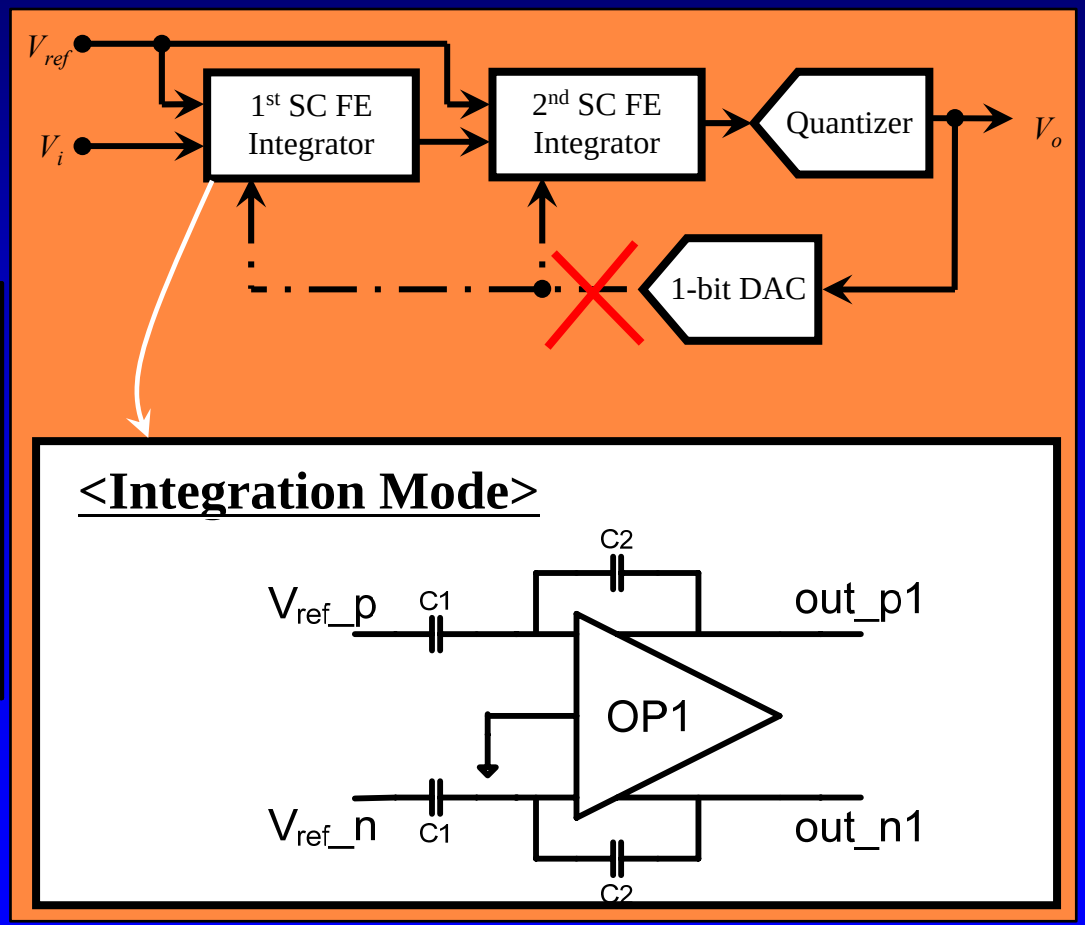




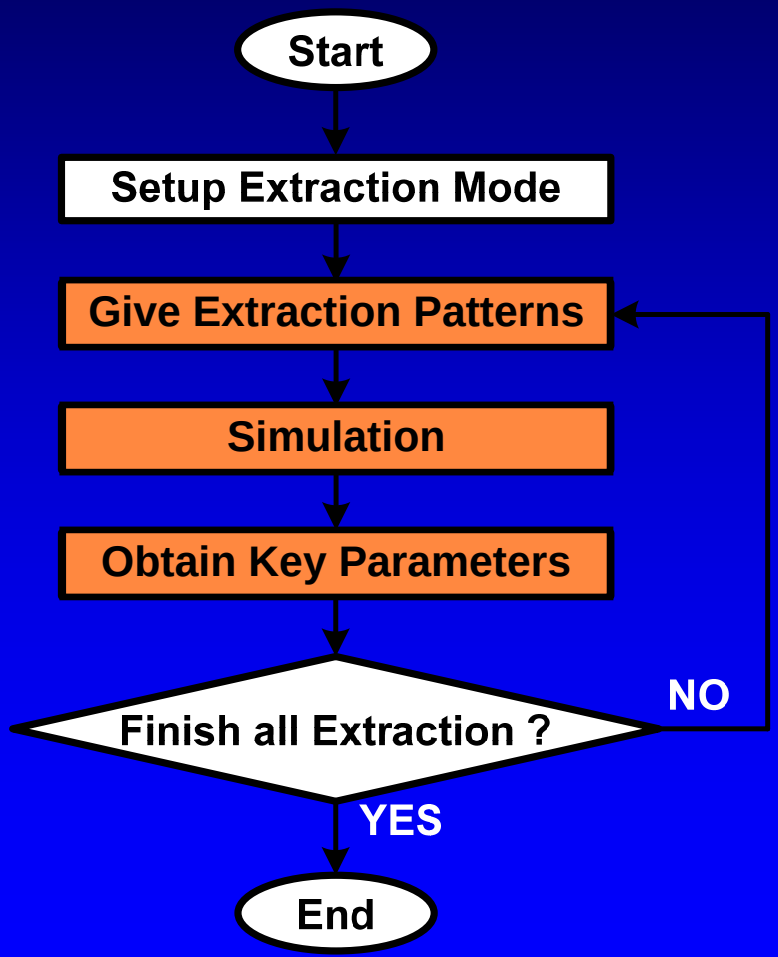
Extraction Mode

- Break the feedback loop of modulator
- Switch SC integrator to integration mode



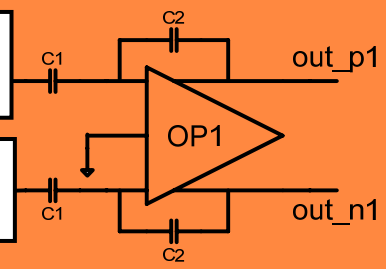


Extraction Patterns



$$V_{ref\_p} = V_{DD}/2 + \Delta V$$

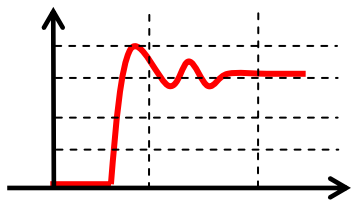
$$V_{ref\_n} = V_{DD}/2 - \Delta V$$



Extraction Pattern

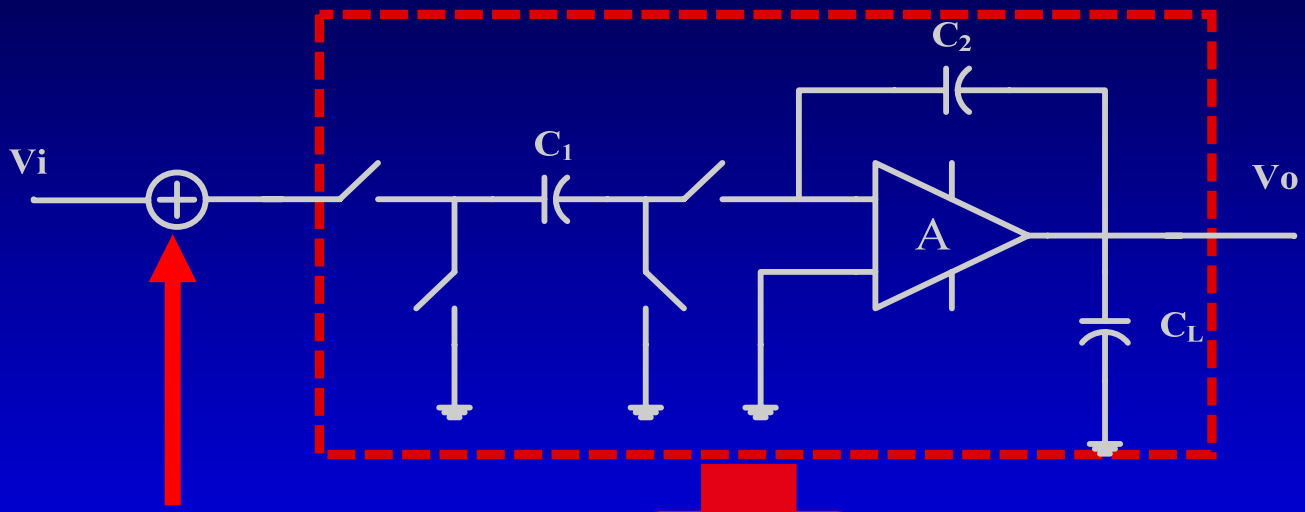
1. $\Delta V = V_1$
   - Finite DC Gain
   - DC-Level Offset
   - Slew Rate : SR_1
2. $\Delta V = V_2$
   - Slew Rate : SR_2
3. $\Delta V = V_3$
   - Max Slew Rate : SR_{Max}
   - Finite bandwidth : ξ, ω_o
   - Switch Delay : T_{d_sw}

key parameters (DC gain, SR.....)



Non-Ideal Effects

- SC integrator seriously affects the performance of ΔΣ modulator



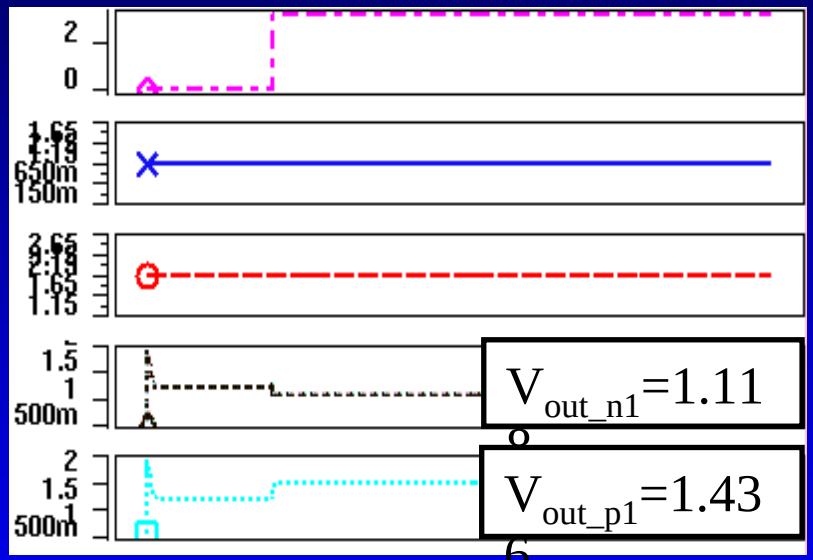
Switch Thermal Noise

Finite DC Gain
+
Slew Rate
+
Finite Bandwidth
+
DC-Level Offset
+
Switch Delay

Extraction – Finite DC Gain

- Extraction patterns : Vref = 1.65 ± 0.4

1st SC Integrator



V_{ref_n}=1.25

V_{ref_p}=2.05

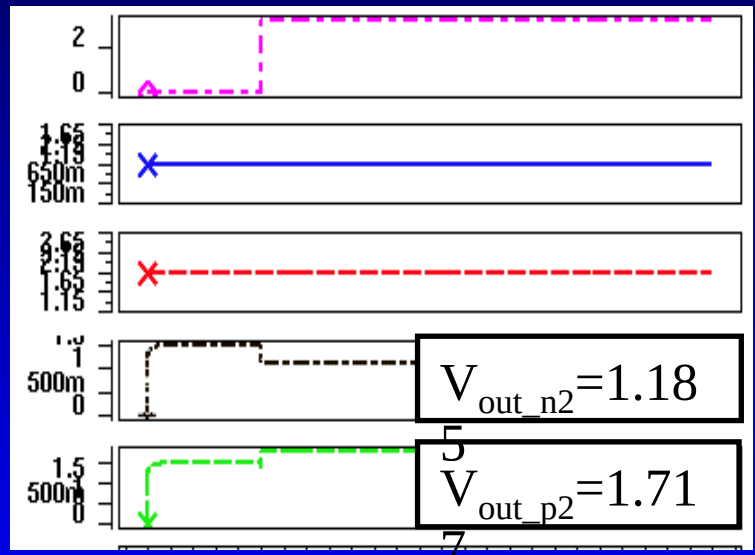
V_{out_n1}=1.118

V_{out_p1}=1.436

$$DC\ Gain_{SC1} = \frac{V_{out\_n1} - V_{out\_p1}}{V_{ref\_p} - V_{ref\_n}}$$

$$= \frac{(1.118 - 1.436)}{2.05 - 1.25} = -0.398$$

2nd SC Integrator



V_{out_n2}=1.185

V_{out_p2}=1.717

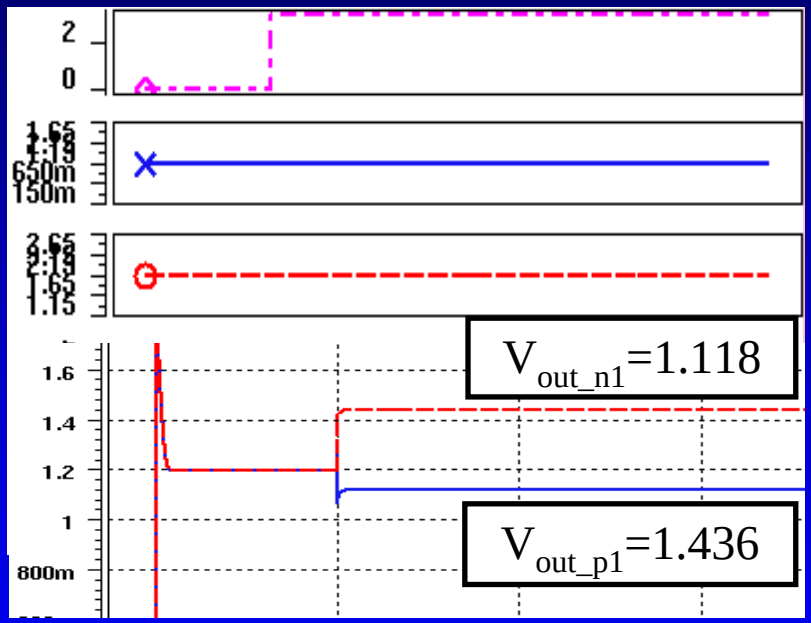
$$DC\ Gain_{SC2} = \frac{V_{out\_n2} - V_{out\_p2}}{V_{ref\_p} - V_{ref\_n}}$$

$$= \frac{(1.185 - 1.717)}{2.05 - 1.25} = -0.665$$

Extraction – DC-Level Offset

- Extraction patterns : Vref = 1.65 ± 0.4

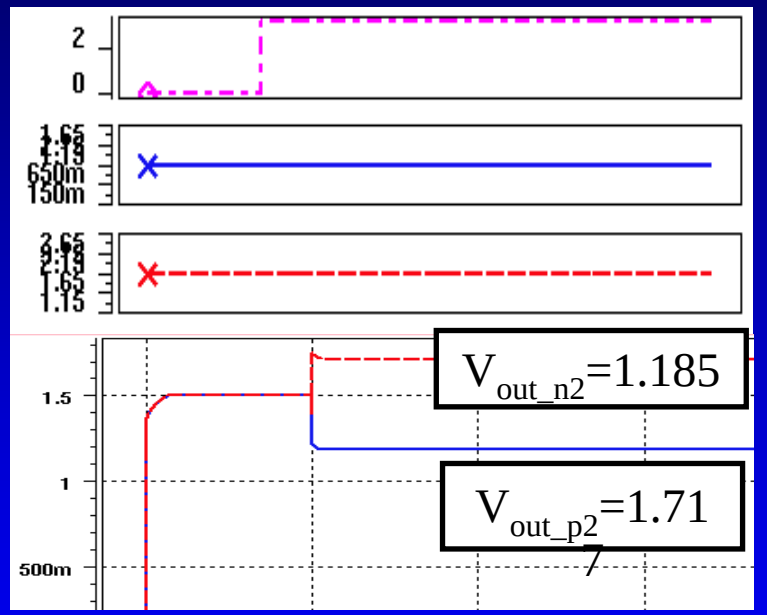
1st SC Integrator



V_{ref_n}=1.25

V_{ref_p}=2.05

2nd SC Integrator



$$V_{offset} = \frac{V_{DD}}{2} - \frac{V_{out\_n} + V_{out\_p}}{2}$$

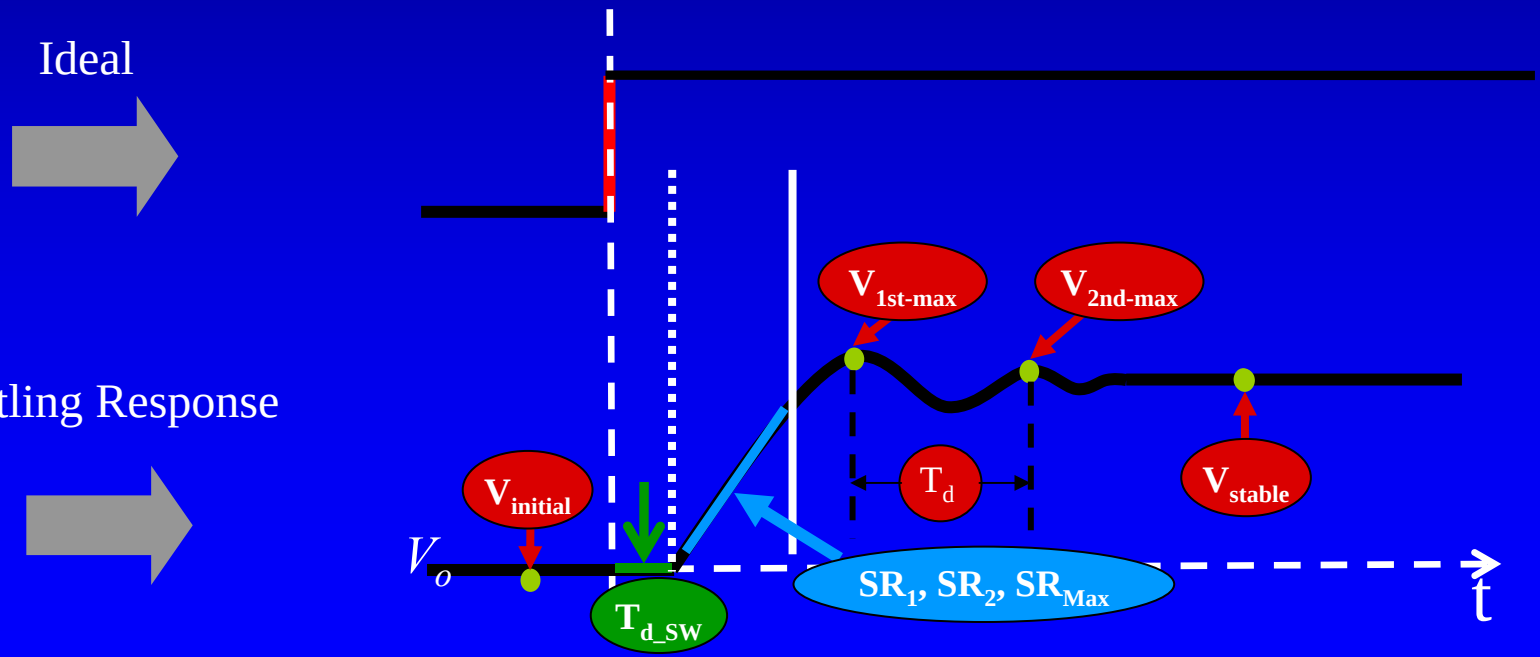
$$= \frac{3.3}{2} - \frac{1.118 + 1.436}{2} = 0.373$$

$$V_{offset} = \frac{V_{DD}}{2} - \frac{V_{out\_n} + V_{out\_p}}{2}$$

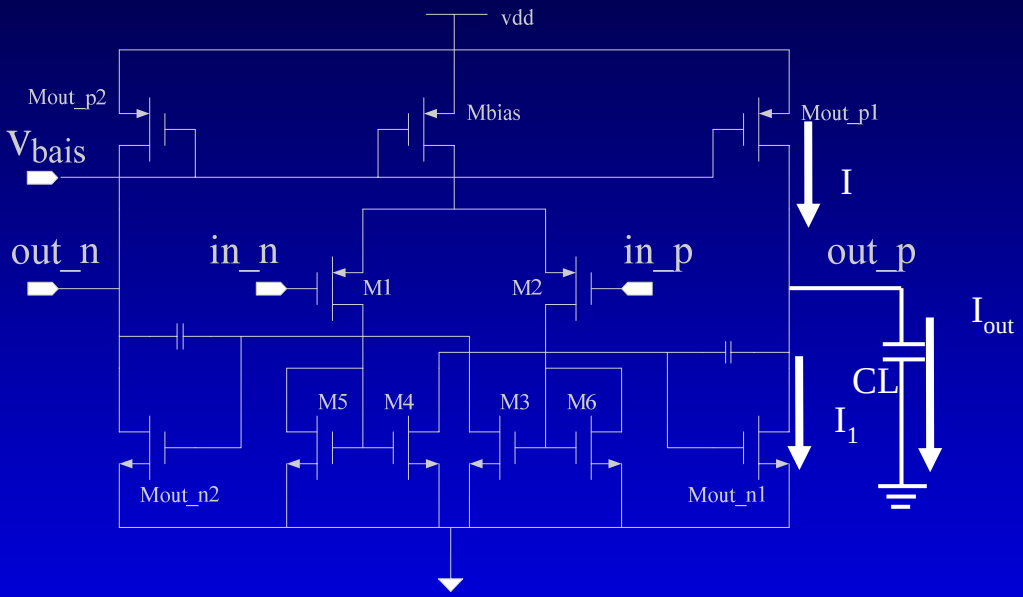
$$= \frac{3.3}{2} - \frac{1.185 + 1.717}{2} = 0.199$$

Settling Response

- Include switch delay, finite slew rate (SR) and output damping
- Two extraction patterns
  - Obtain two real SR value
- One extraction pattern
  - Obtain output damping, switch delay and Max. SR



Slew Rate



SR basic formula

$$SR = \frac{I_{out}}{C_L} = \frac{I - I_1}{C_L}$$

$$= \frac{I - \frac{1}{2}\beta(V_{in} - V_{tp} - V_{tn})^2}{C_L}$$

$$V_{ref1} \Rightarrow SR_1 = \frac{I - \frac{1}{2}\beta(V_{ref1} - V_{tp} - V_{tn})^2}{C}$$

$$V_{ref2} \Rightarrow SR_2 = \frac{I - \frac{1}{2}\beta(V_{ref2} - V_{tp} - V_{tn})^2}{C}$$

$$V_{ref} \Rightarrow SR = \frac{I - \frac{1}{2}\beta(V_{ref} - V_{tp} - V_{tn})^2}{C}$$

Dynamic SR calculation equation

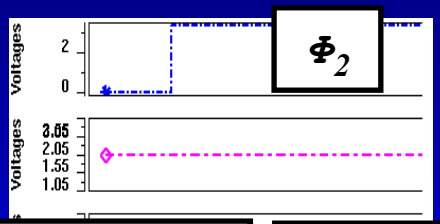
$$\frac{SR_1 - SR_2}{SR_2 - SR_{in}} \approx \frac{V_{ref1} - V_{ref2}}{V_{ref2} - V_{in}} \Rightarrow SR_{in} \approx SR_2 - \frac{V_{ref2} - V_{in}}{V_{ref1} - V_{ref2}} \times (SR_1 - SR_2)$$

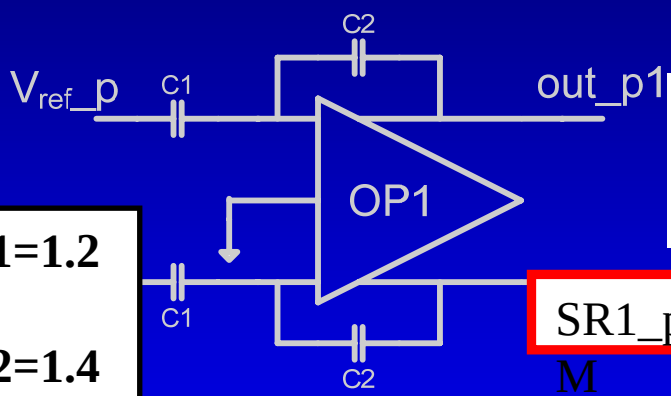
(V_{ref1},V_{ref2} : Extraction Pattern, SR_1,SR_2 : Extraction Value)

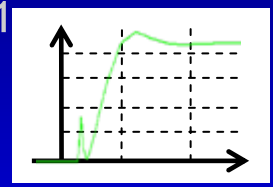
Extraction – SR

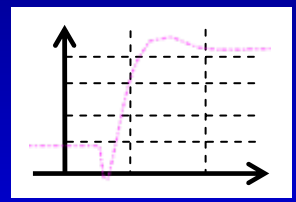
- Extraction patterns : Vref = 1.65 ± 0.4 / 1.65 ± 0.2

1st SC Integrator









Vref_p1=2.05
Vref_p2=1.85

Vref_p1=1.25
Vref_p2=1.45

SR1_p1=94.74M

SR1_p2=50.75M

$$SR_1 \approx 94.74M - (50.75M - 94.74M) \times \frac{2.05 - V_{ref1}}{1.85 - 2.05}$$

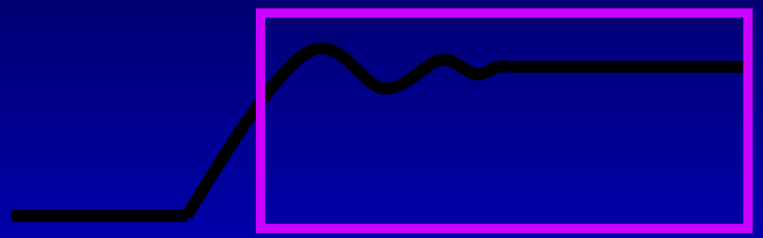
Input V_{ref1} → SR_1

Output Damping (1/2)

- Second-Order Integrator Transfer Function

$$\frac{V_o(s)}{V_i(s)} = \frac{C_1/C_2 \cdot \omega_o^2}{s^2 + 2\xi\omega_o s + \omega_o^2}$$

Finite bandwidth effect



- Hard to obtain damping ratio (ξ) and pole frequency (ω_o)

$$\xi = \frac{1}{2 \cdot \sqrt{\frac{\left(-\pi / ln(OS\%)\right)^2 + 1}{4}}} \quad ; A\omega_0 = \frac{2\pi}{T_d\sqrt{1-\xi^2}}$$

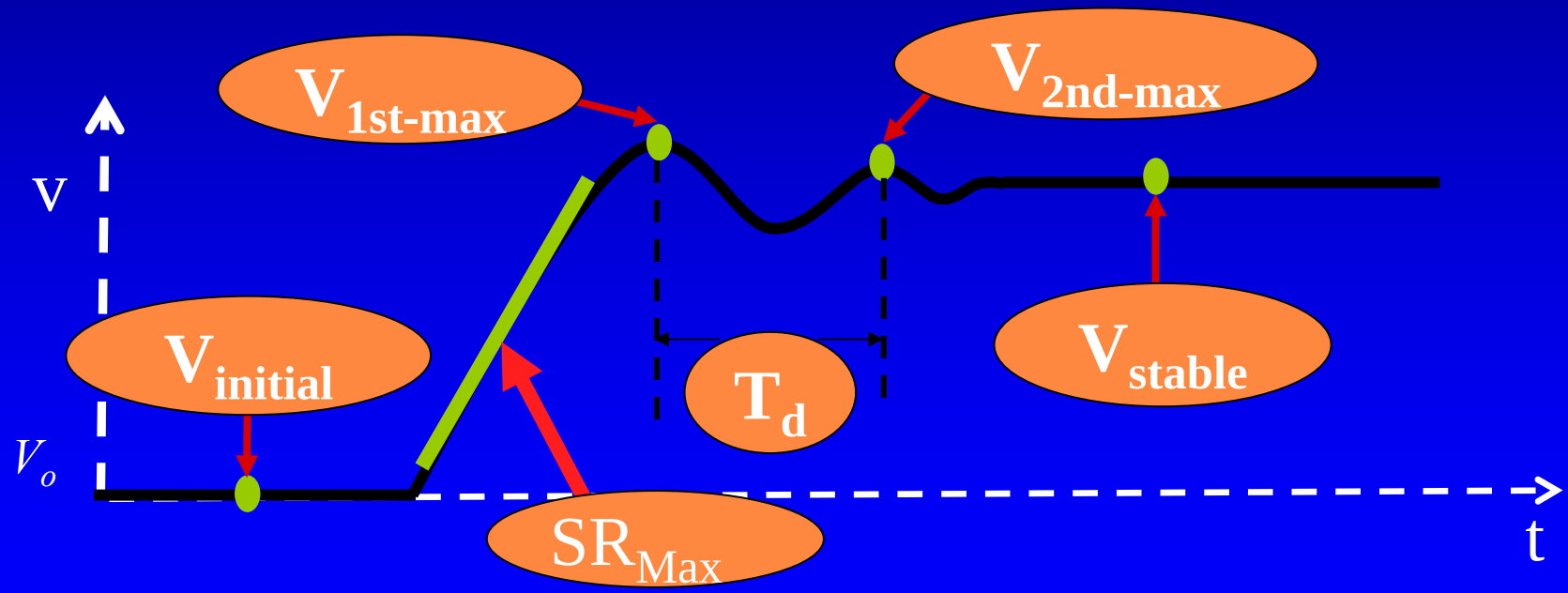
- How to obtain overshoot percent (OS%) and period oscillation (T_d)
  - Easier to be measured from the output waveform

Ref P. E. Allen, D. R. Holberg “CMOS Analog Circuit Design” 2nd ed. New York Oxford, 2002

Output Damping (2/2)

- Obtain overshoot percent (OS%), period oscillation (T_d) and Max. slew rate (SR_{Max}) using one extraction pattern

$$OS\% = \left(\frac{V_{max} - V_{stable}}{V_{stable} - V_{initial}} \right) \quad \Delta V_{max} = V_{1st\text{-}max} - V_{stable}$$



Ref P. E. Allen, D. R. Holberg "CMOS Analog Circuit Design" 2nd ed. New York Oxford, 2002

Extraction – Output Damping

- Extraction patterns : Vref = 1.65 ± 0.5

1st SC Integrator

$$V_{initial} = 1.3921\,(v), V_{max} = 1.6052\,(v)$$
$$V_{stable} = 1.5808\,(v), T_d = 5\times10^{-9}\,(s)$$
$$SR_{Max} = 113.08M$$

$$OS\% = \left(\frac{V_{max} - V_{stable}}{V_{stable} - V_{initial}}\right) = \frac{1.6052 - 1.5808}{1.5808 - 1.3921} = 0.1293$$

$$\xi = \frac{1}{2\cdot\sqrt{\frac{\left(-\pi/\ln(OS\%)\right)^2 + 1}{4}}} \cong 0.6$$

$$\omega_0 = \frac{2\pi}{T_d\sqrt{1-\xi^2}} \cong 1.5\times10^9$$

2nd SC Integrator

$$V_{initial} = 1.5012\,(v), V_{max} = 1.81\,(v)$$
$$V_{stable} = 1.7741\,(v), T_d = 0.772\times10^{-6}\,(s)$$
$$SR_{Max} = 19.56M$$

$$OS\% = \left(\frac{V_{max} - V_{stable}}{V_{stable} - V_{initial}}\right) = \frac{1.81 - 1.7741}{1.7741 - 1.5012} = 0.1316$$

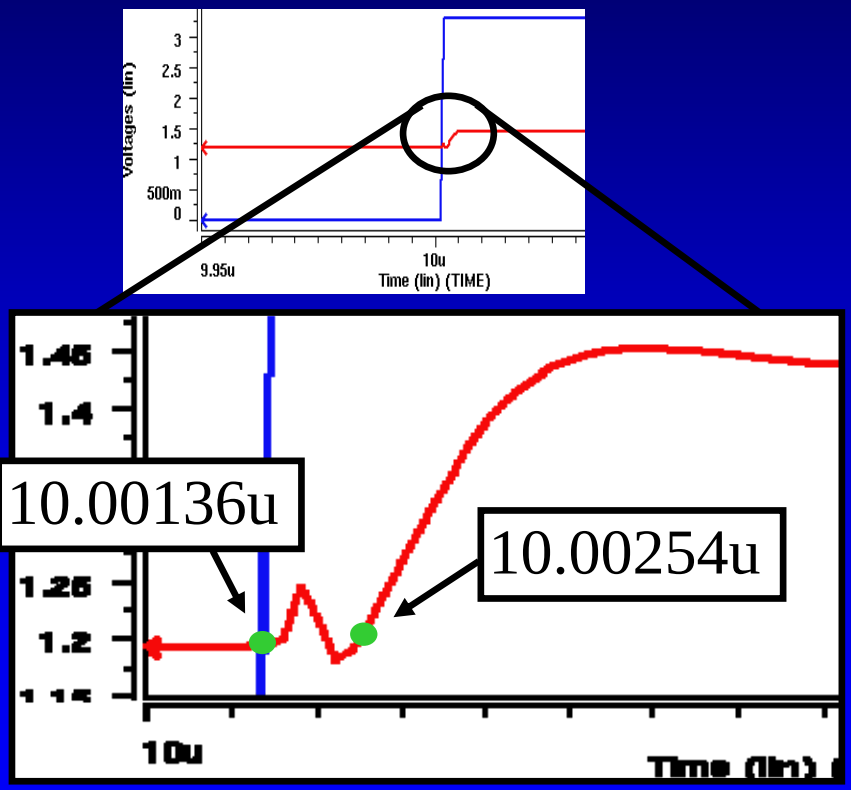
$$\xi = \frac{1}{2\cdot\sqrt{\frac{\left(-\pi/\ln(OS\%)\right)^2 + 1}{4}}} \cong 0.6$$

$$\omega_0 = \frac{2\pi}{T_d\sqrt{1-\xi^2}} \cong 1.02\times10^7$$

Extraction – Switch Delay

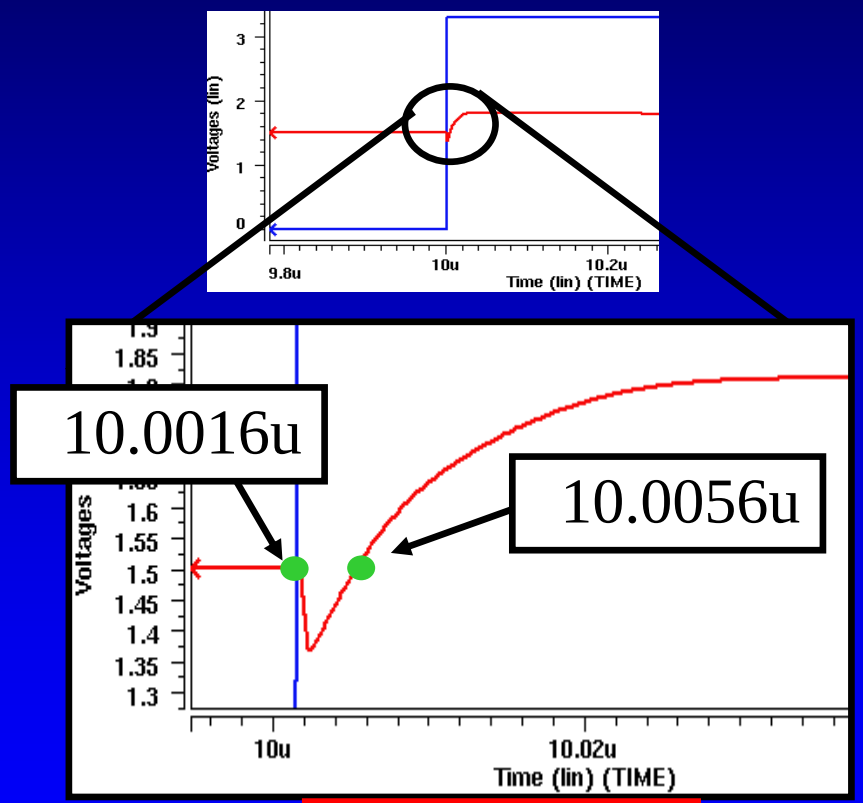
- Extraction patterns : Vref = 1.65 ± 0.5

1st SC Integrator



$T_{d\_SW} = 1.18n$

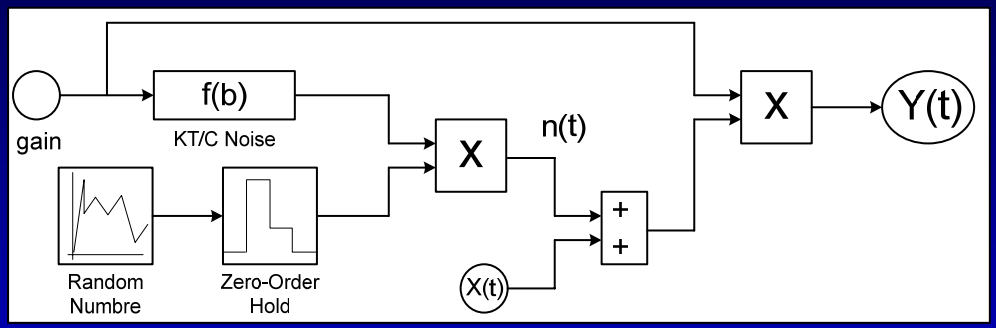
2nd SC Integrator

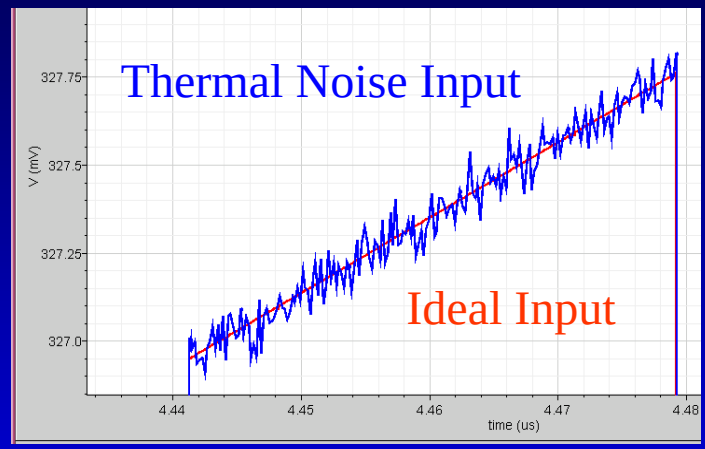


$T_{d\_SW} = 4n$

Switch Thermal Noise

- Gaussian random variable





$$e_T^{\,2} = \int_0^{\infty} \frac{4kTR_{on}}{1+(2\pi 2\pi_{on} C_s)^2} df = \frac{kT}{C_s}$$

$$V_o(t) = \left[V_i(t) + e_T(t)\right] \times DC\ Gain$$

$$V_o(t) = \left[V_i(t) + \sqrt{\frac{kT}{Cs}} \cdot n(t)\right] \times DC\ Gain$$

n(t): Gaussian random process with $\mu=0, \sigma=1$

Ref□P.Malcovati ,S.Brigati, F.Francesconi, F.Maloberti, P.Cusinato, A.Baschirotto, ”Behavioral modeling of switched-capacitor sigma-delta modulators” , IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS□I :Fundamental Theory and Applications, VOL. 50, NO. 3, MARCH 2003

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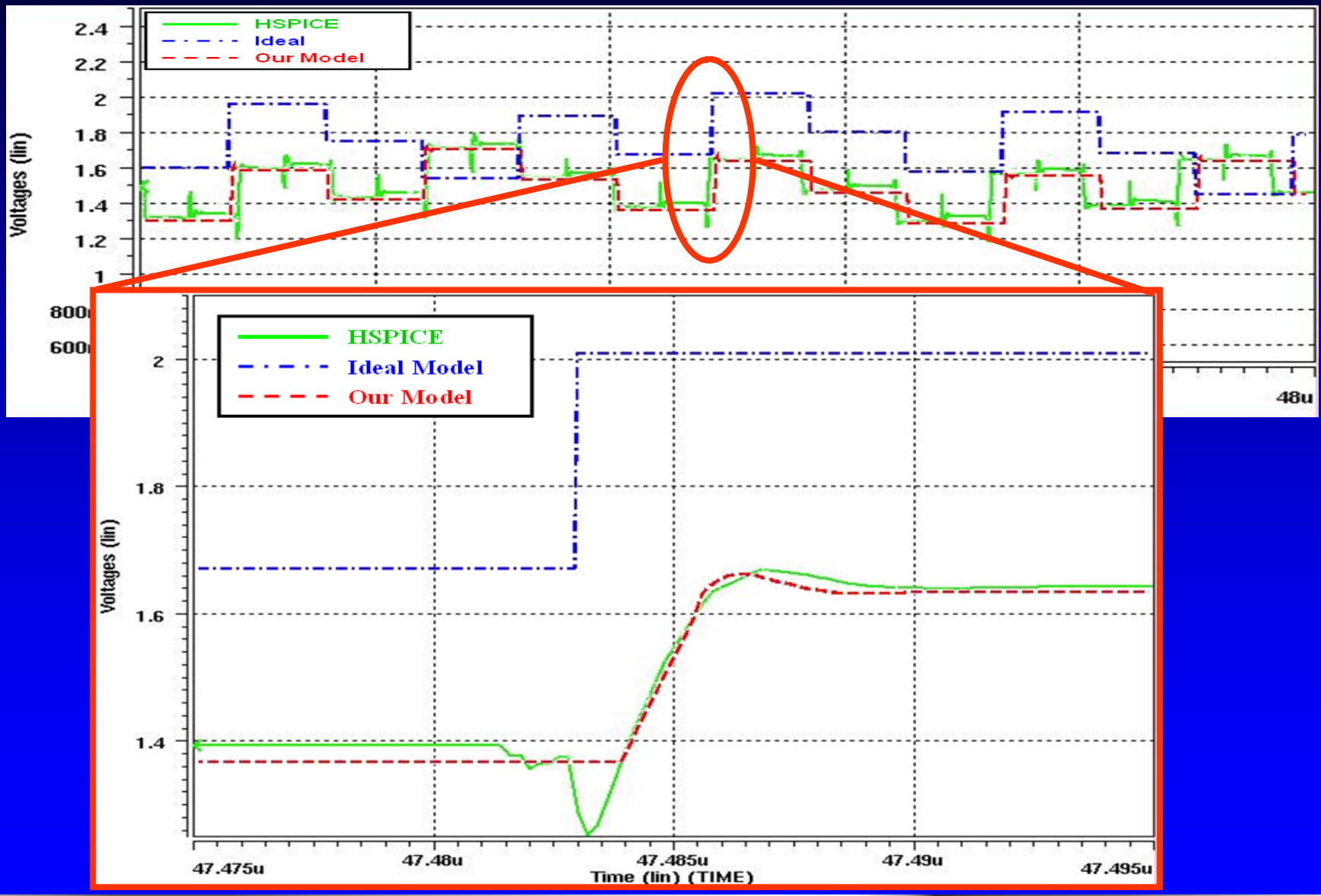
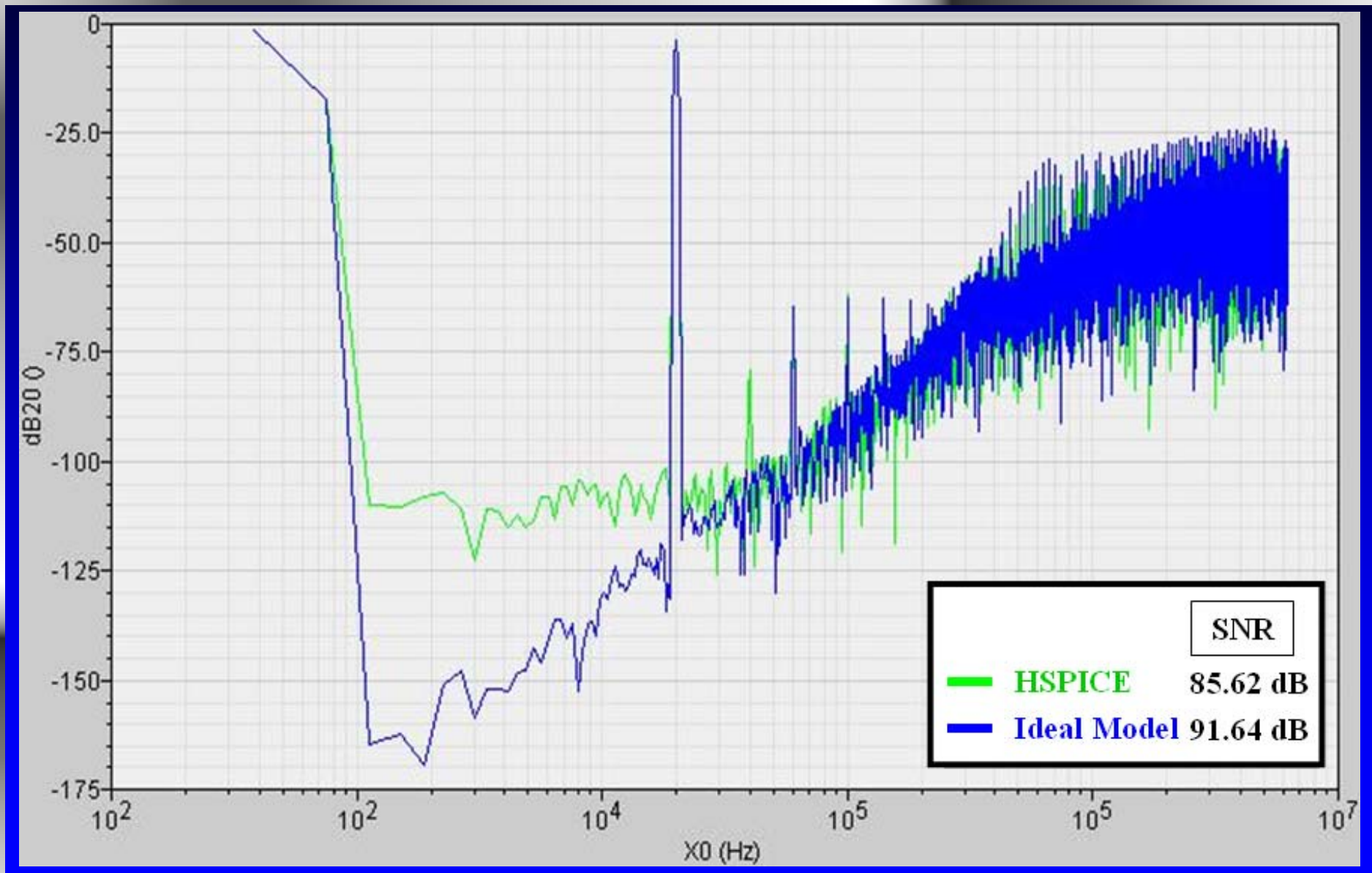
Setup Environment

- Second-order ΔΣ modulator
  - Implement in TSMC 0.25um TT_3V CMOS process
  - Oversamping ratio (OSR) = 303
  - Sampling frequency = 12.5MHz
  - Signal frequency = 20.6 KHz
- Our developed behavioral model
  - Verilog-A language
  - Simulated in Analog Artist (Cadence) using Spectre
- Use “ wavescan ” tool to
  - Show the timing and frequency waveform
  - Calculate Fast Fourier Transform (FFT) and Signal-to-Noise Ratio (SNR)
- FFT & SNR setup parameters
  - Timing range : 800 ns ~ 2622.24 us
  - Signal range : 19.073 KHz ~ 21.362 KHz
  - Noise range : 1.5259 KHz ~ 40.054 KHz
  - Sampling point : 32768

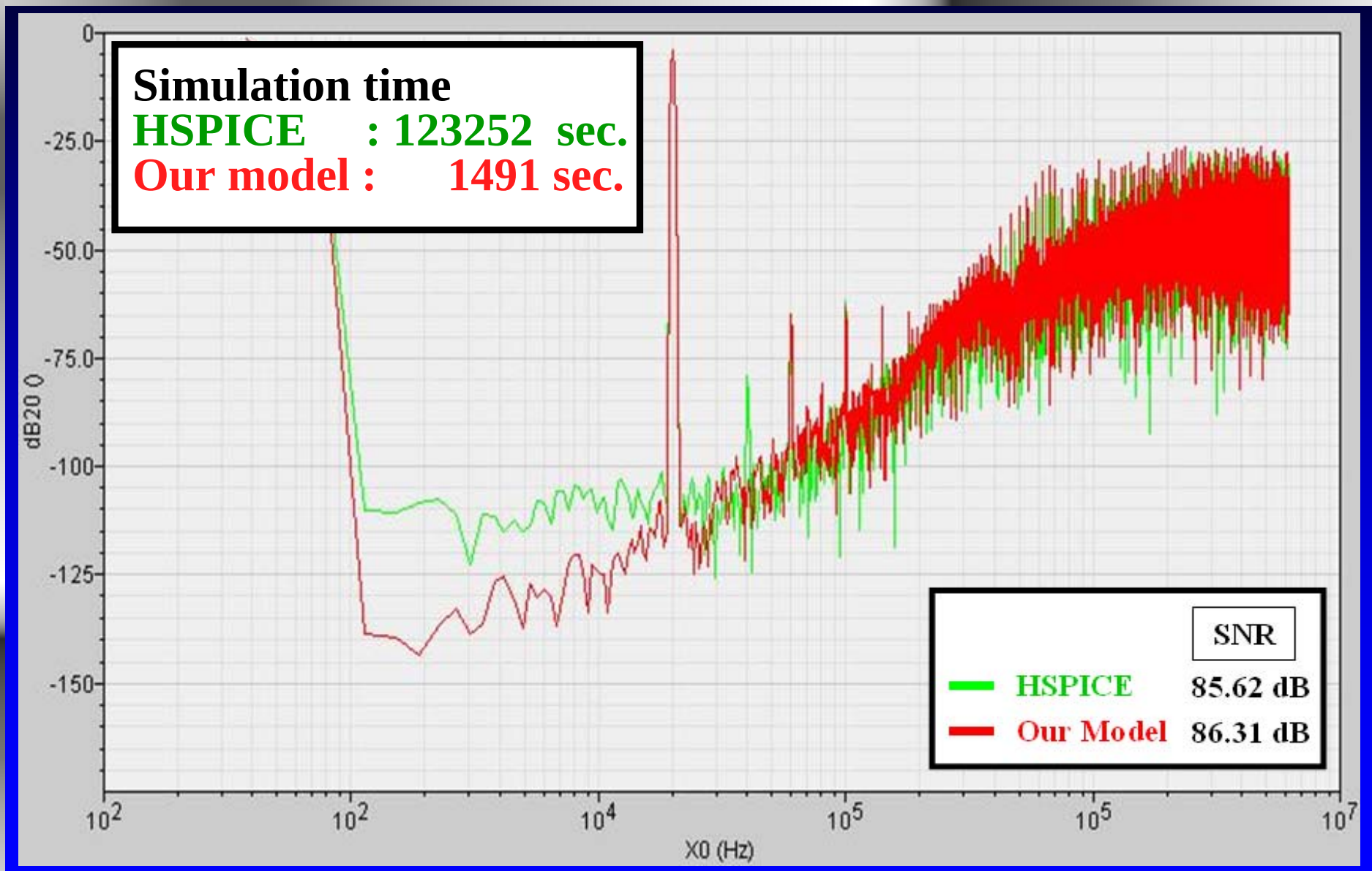
Timing Waveform



FFT & SNR (HSPICE VS Ideal)



FFT & SNR (HSPICE VS Our)



Conclusions

- Our bottom-up extraction approach is suitable for IP-based design
- Switch to extraction mode instead of separating into several sub-blocks
  - Actual loading effects and parasites can be considered automatically
  - Non-ideal effects can be extracted easily using some extraction patterns
- Can include the following non-ideal effects
  - Finite DC gain & DC-level offset
  - Settling response
  - Thermal noise
- Our model is very close to HSPICE results with less simulation time.

Thanks for your attention ~