Event Driven Modeling of RF Frontends

Stefan Joeres, Hans-Werner Groh *, Prof. Stefan Heinen
Chair of Integrated Analog Circuits
Aachen University of Technology
http://www.ias.rwth-aachen.de
mailbox@ias.rwth-aachen.de
* Atmel Germany GmbH

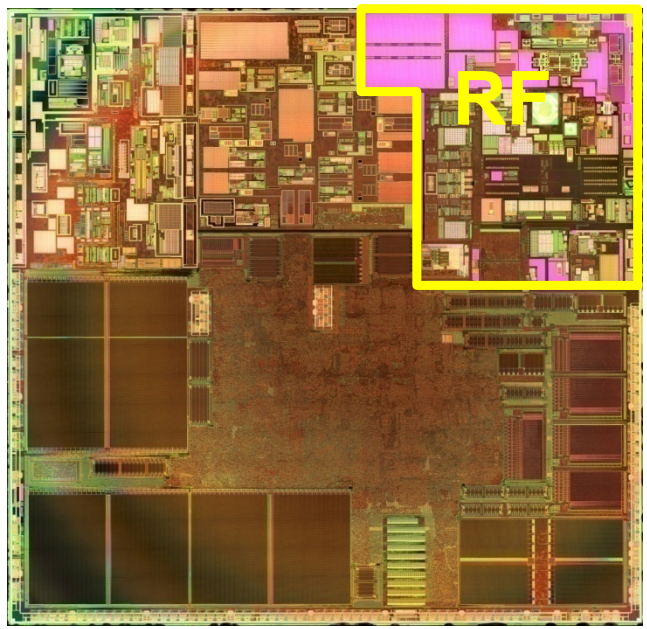
Outline

- Motivation
- Target
- Verification Problem in RF SoCs
- Necessity of wreal Modeling
- Problems
- Tips'n'Tricks
- Conclusion and Future Work

Motivation

Modern transceiver systems feature:

- analog frontend
- digital enhancements
- digital calibration
- digital control loops
- digital predistortion
- digital interfaces
- digital programming



Several 100k gates are supporting and controlling the analog RF functions.
RF verification consumes lots of manpower & money.

Targets

- **Short Term : Functional Verification of Tape Out DB**
  - Verify a complete transmission burst for different modes
    - Necessity to define a simulation strategy that covers all possibilities
  - Pin accurate compatible for all implementation levels !
  - Common database for verification and tape out
  - Just in time – always.

- **Long Term : Executable Specification**
  - Close the gap between
    - RF Engineer (Noisefigure, …)
    - System Engineer (BER, PER, …)

Verification Problem for Complex RF-SoC

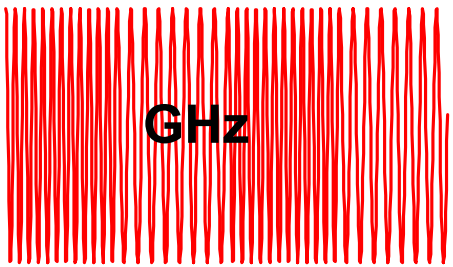
- **Simulation speed aspects**
  - A complete transmission burst including power up sequence, calibration routine, frequency and bias settling is necessary (long transient).
  - Traditional VerilogA model takes several days to complete
  - It is necessary to include the digital control logic and biasing structures.
  - Analog stepsize is inversely proportional to the highest frequency

- **Connectivity and functionality**
  - „Simply“ has to be ensured – more difficult than one may think… (passband models are more practical, although awfully slower than baseband)

Necessity of wreal modeling

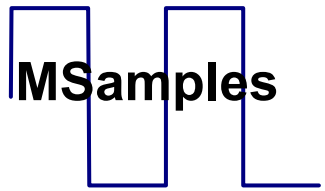
Main Problem :

Frequency difference between RF carrier and signal data/rest of chip



RF – carrier
typ. 1-10 GHz

< 1 % of Transistorcount



Payload
typ. 0.1–100 MHz

> 99 % of Transistorcount

Possibility with wreal modeling :

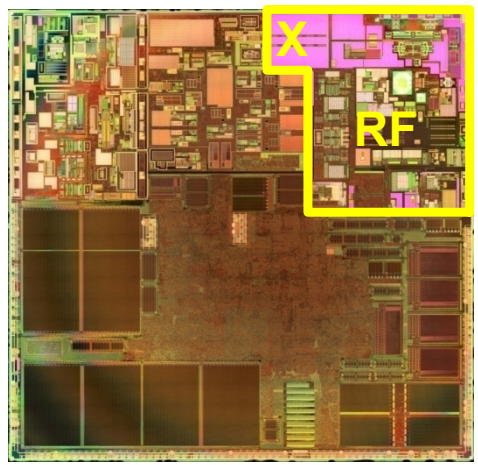
Seperate high frequency signal components from real analog components.

Necessity of wreal modeling

- Up to now, split solution of schematic parts is only possible in the discrete time domain (using event driven simulation).

- Analog solvers still solve the whole matrix everytime (approaches for seperation do exist, but have not shown to be fully functional)

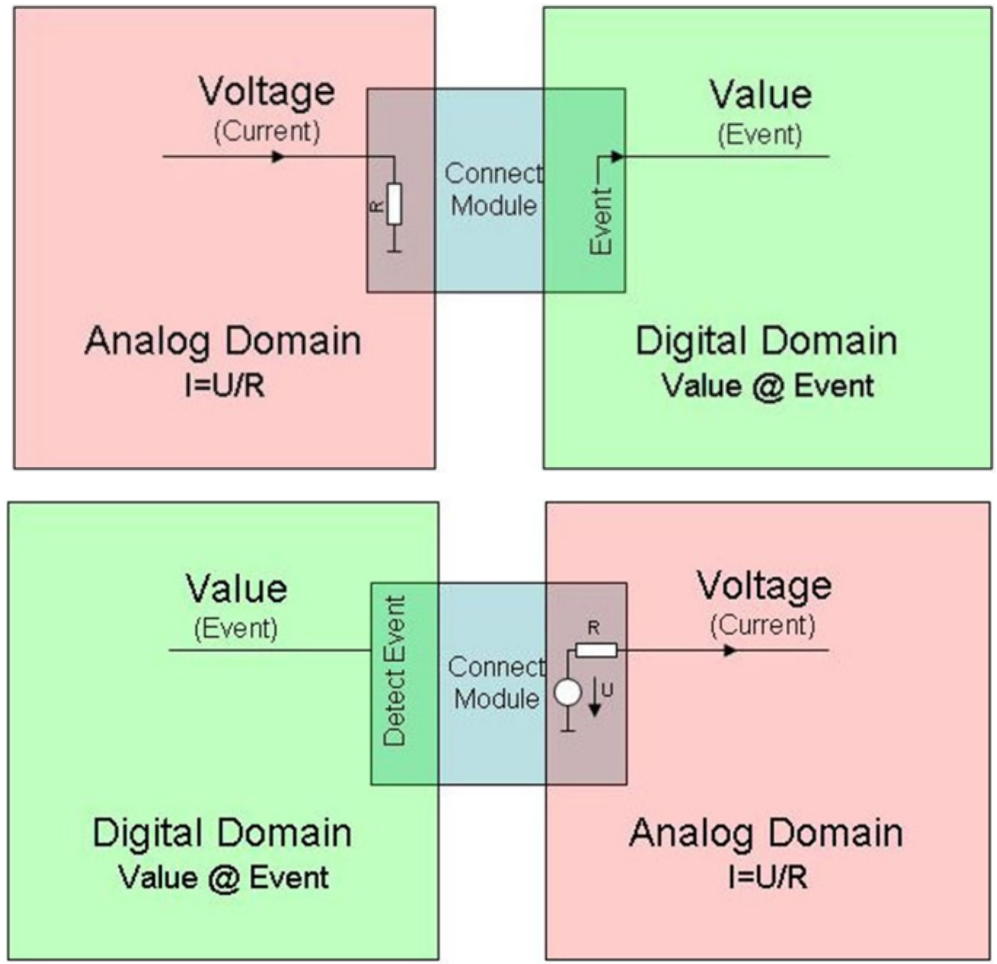
- To focus on the desired verification parts, a transformation from the analog to the digital domain is useful for the rest of the chip.



Comparison of available Tools

Tool	Matlab	VerilogAMS wreal	Verilog Logic	VerilogA Electrical
Domain	N.A.	Discrete	Discrete	Analog
Simulation Time Steps	Clocked (Vector optimized)	Event driven	Event driven	Accuracy dependant
Sampling Type	Uniform	Nonuniform	N.A.	Nonuniform
Value	Continous	Continous	Discrete	Continous
Calculation Rate	Everything at clocked rate	Single Event	Single Event	Everything – always
Speed	++	+	+	--
Verification possibility	- (no relation to schematics)	+ (depending on accuracy)	o (true/false conn-ectivity only)	++

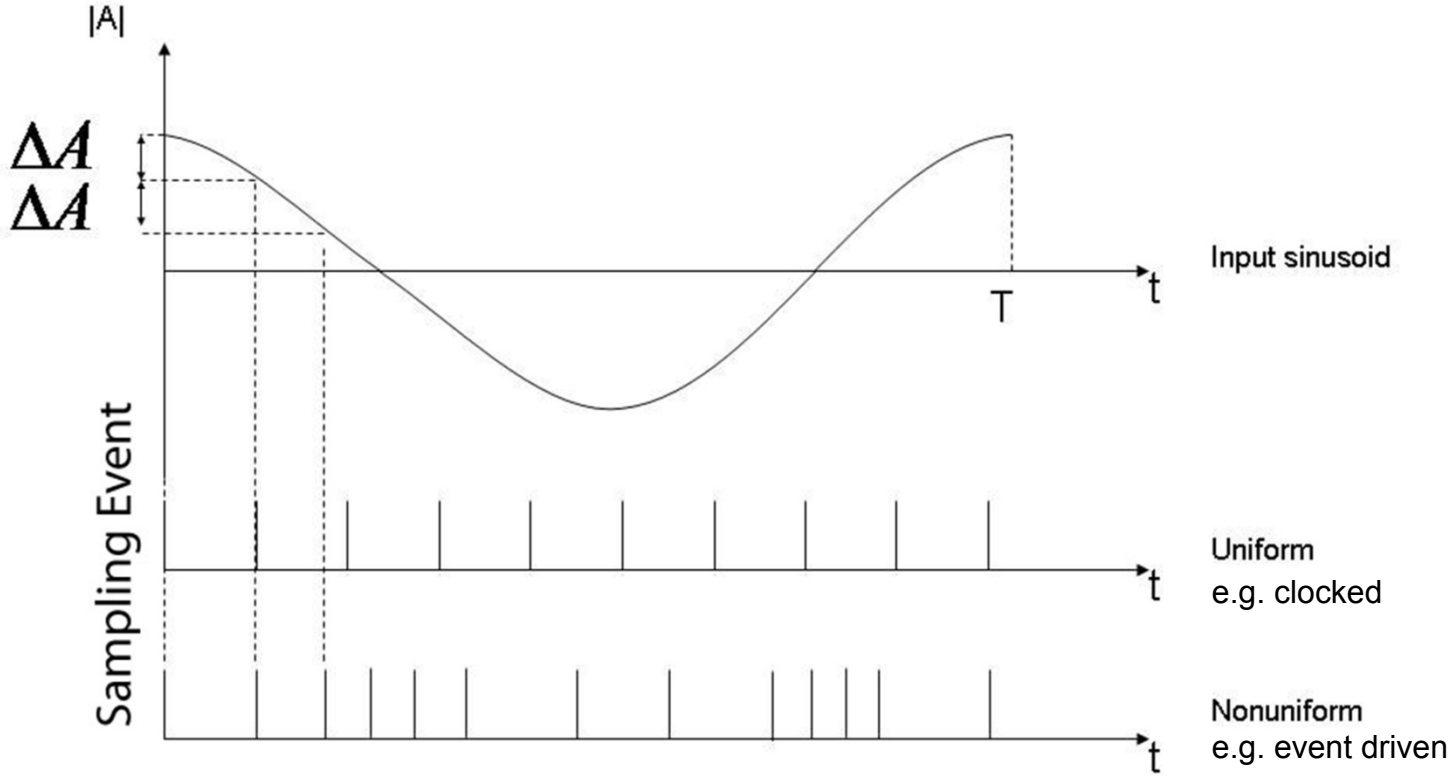
Implementation of Connect Modules (Cadence)



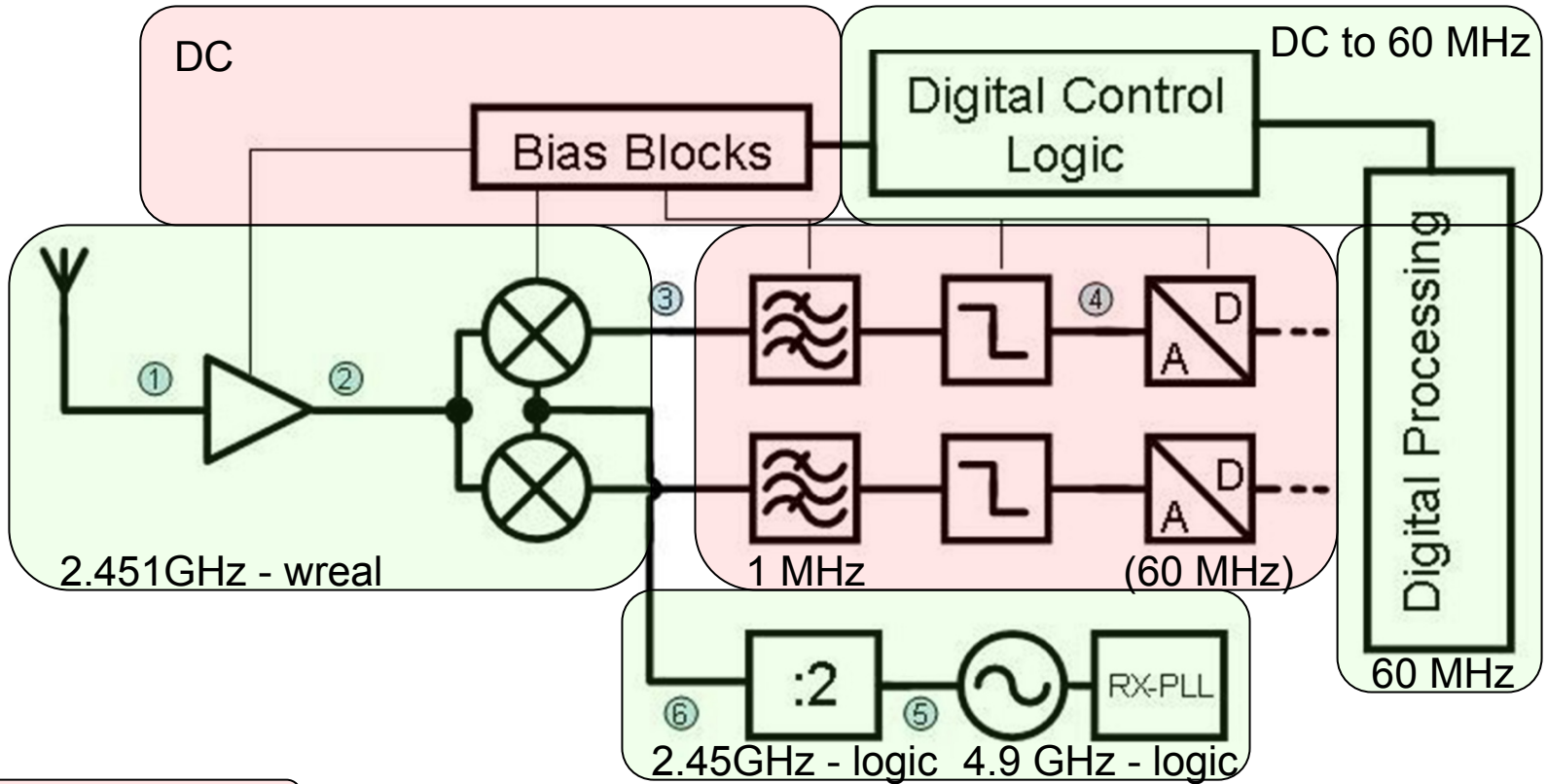
Voltage change of ΔA leads to event (either digital or analog)

Uniform and Nonuniform sampling

- Events are triggered when specified voltage difference between analog time points is exceeded.
- Triggered events release analog change only when value changes specified amount.



BT Receiver Example



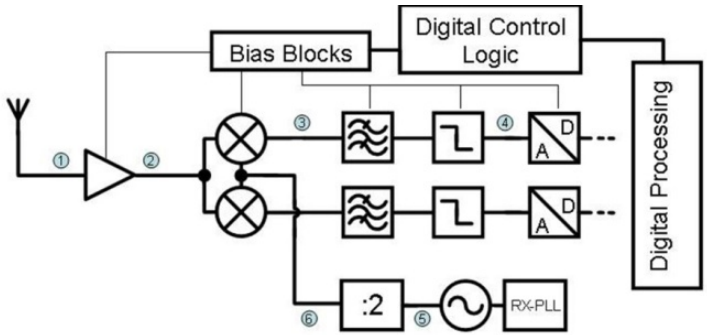
Analog Domain

Discrete Domain

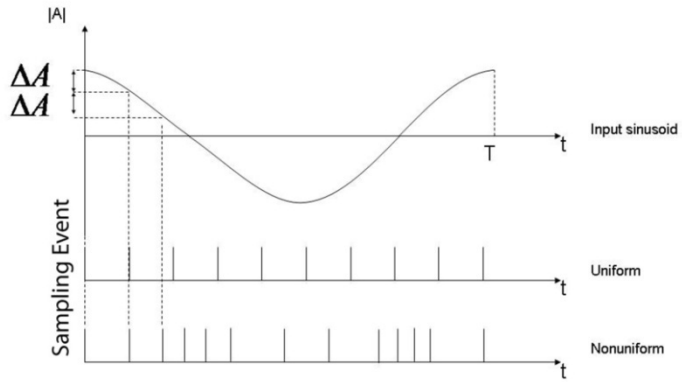
Critical Point 1 – Signal Input

Assumed to be the lowest signal voltage on chip :

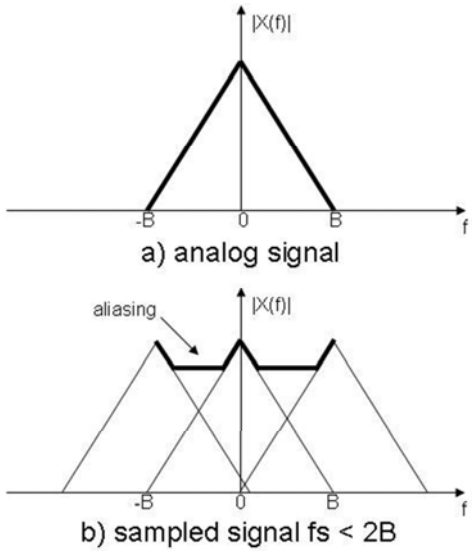
LNA input ~ 5 µVpp



How to specify voltage difference ΔA that has to be detected to trigger wreal sampling event ?



Sampling Theorem (Nyquist)



Designers Rule of Thumb :

Use highest frequency of interest *10 to include filter characteristics

So we define the desired OSR to be = 10

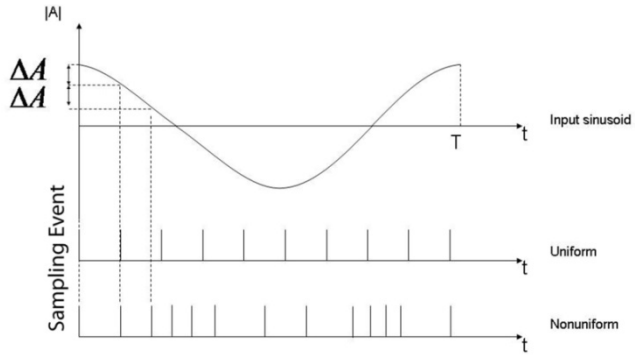
But … this results from a uniform sampling approach !

Formulas

$$\Delta A = A_0 \cdot [\cos(\omega t) - \cos(\omega(t + \Delta t))]$$

$$\Delta t = \frac{T}{N} = \frac{2\pi}{\omega_0 \cdot N}$$

OSR N for clockycle



$$\Delta A_{T,\min} = A_0 \cdot (1 - \cos(\frac{2\pi}{N}))$$

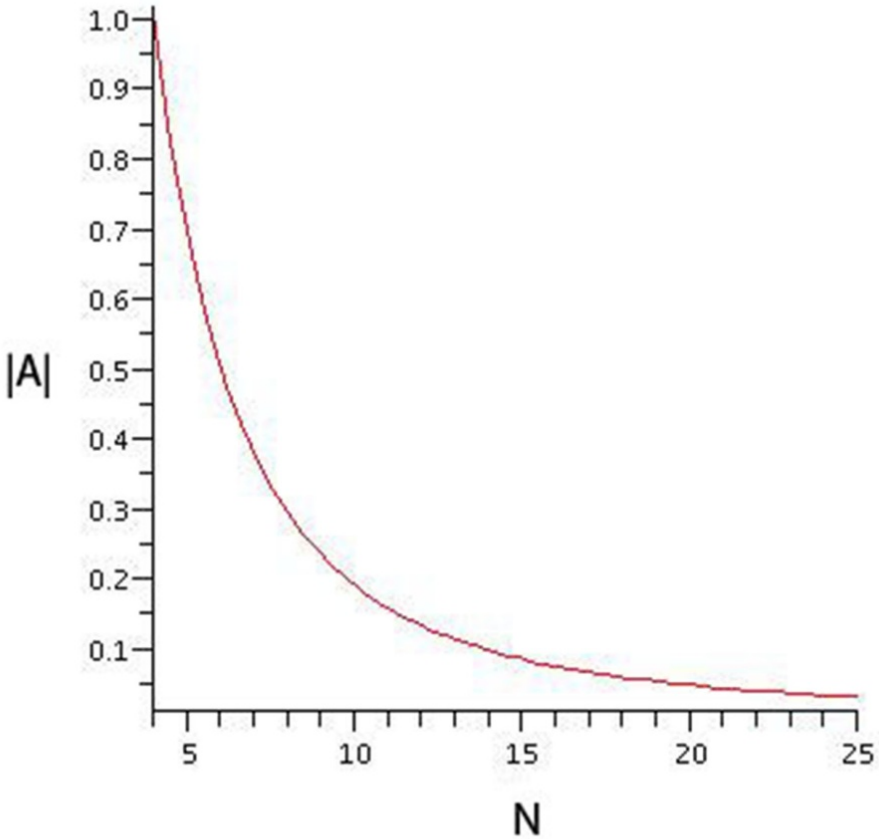
minimum change of amplitude during one cycle (independent of frequency)

$$OSR_{nUn} = 4 \cdot \frac{A_0}{\Delta A_{T,\min}} = \frac{4}{1 - \cos(\frac{2\pi}{N})}$$

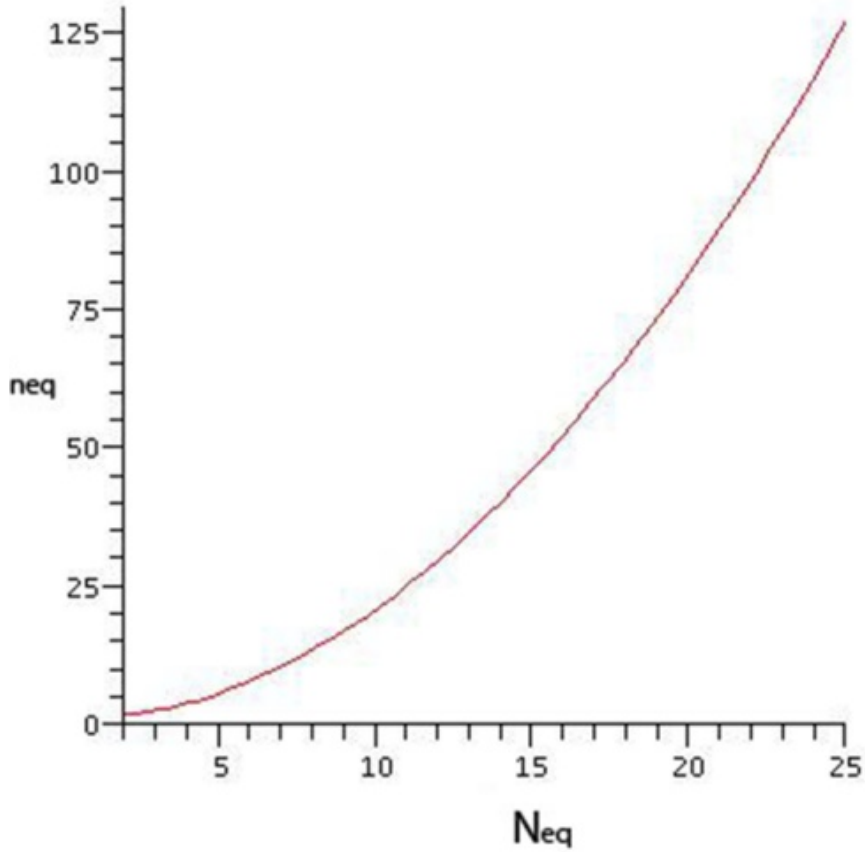
Example :
Input Signal of -40dBm @ 50 Ohm
=> ΔA=0.1uV for N=10

OSRnUn=21

Voltage difference and additional oversampling



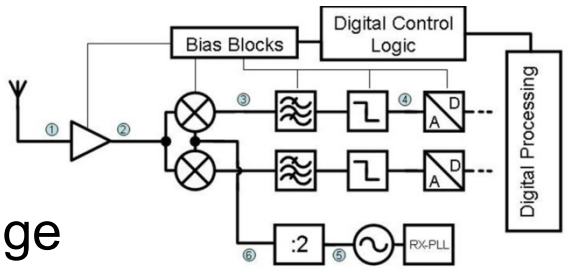
Normalized value of ΔA and resulting OSR



Resulting Non-uniform OSR vs. uniform OSR

Critical Point 2 – Different Voltages (Vpp) on Chip

- Remember :



LNA input voltage - several µV

Gain of LNA + Mixer - >30 dB = mV Range

Using the same resolution with wreal modeling leads to unneccessary oversampling!

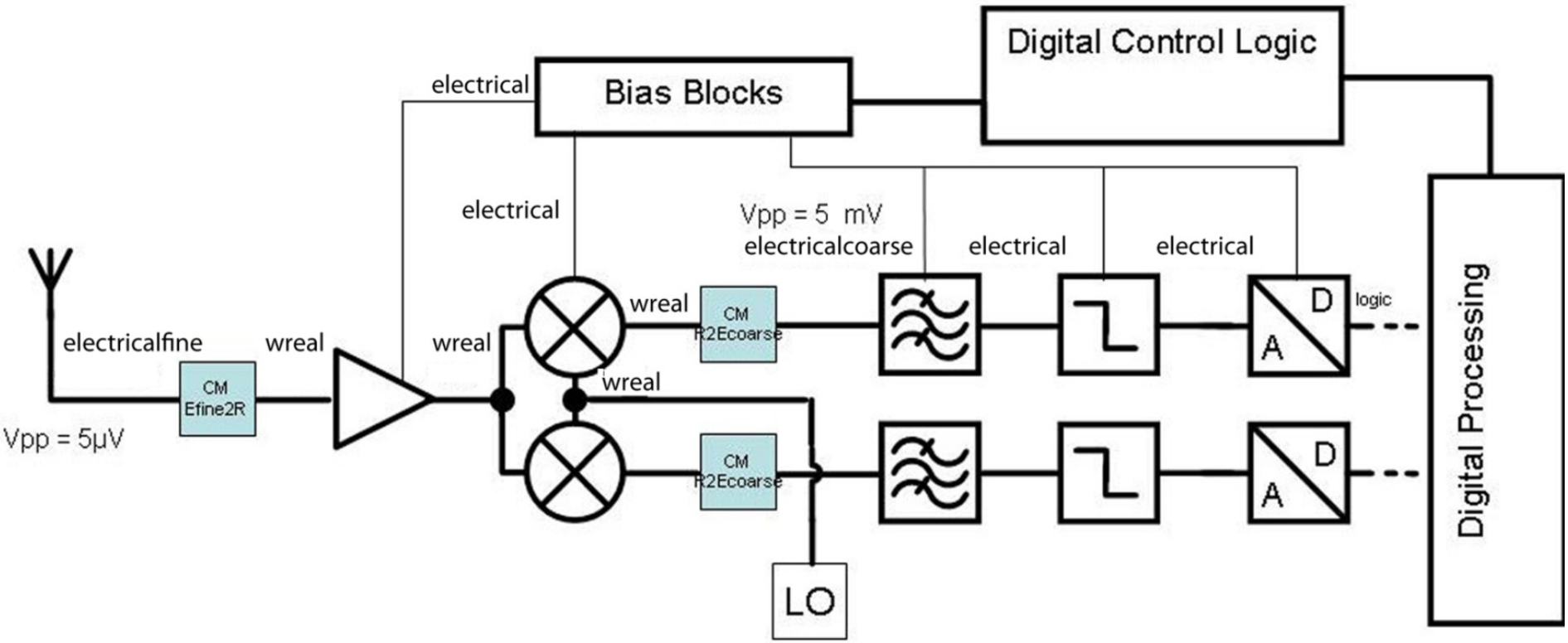
Example :

Block	Voltage	Uniform SR	Nonuniform SR	ΔA
LNA	5 µVpp	2.4 GHz * 10	2.4 GHz * 21	0.955 µV
Mixer	5 mVpp	4.8 GHz * 10	4.8 GHz * 21000	0.955 µV

Additional oversampling after the mixer : 21k -> impossible!

Solution : Use different disciplines for CM nets !

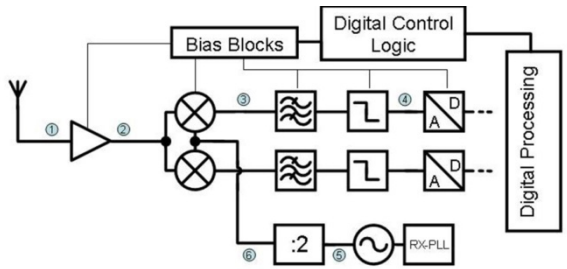
Net Disciplines



Block	Voltage	Uniform	Nonuniform	ΔA
LNA	5 µVpp	2.4 GHz * 10	2.4 GHz * 21	0.955 µV
Mixer	5 mVpp	4.8 GHz * 10	4.8 GHz * 21	0.955 mV

Critical Point 3 – Mixer output

Frequencies that occur during mixing process
(first order only)



2.41GHz – 2.4GHz = 1 MHz

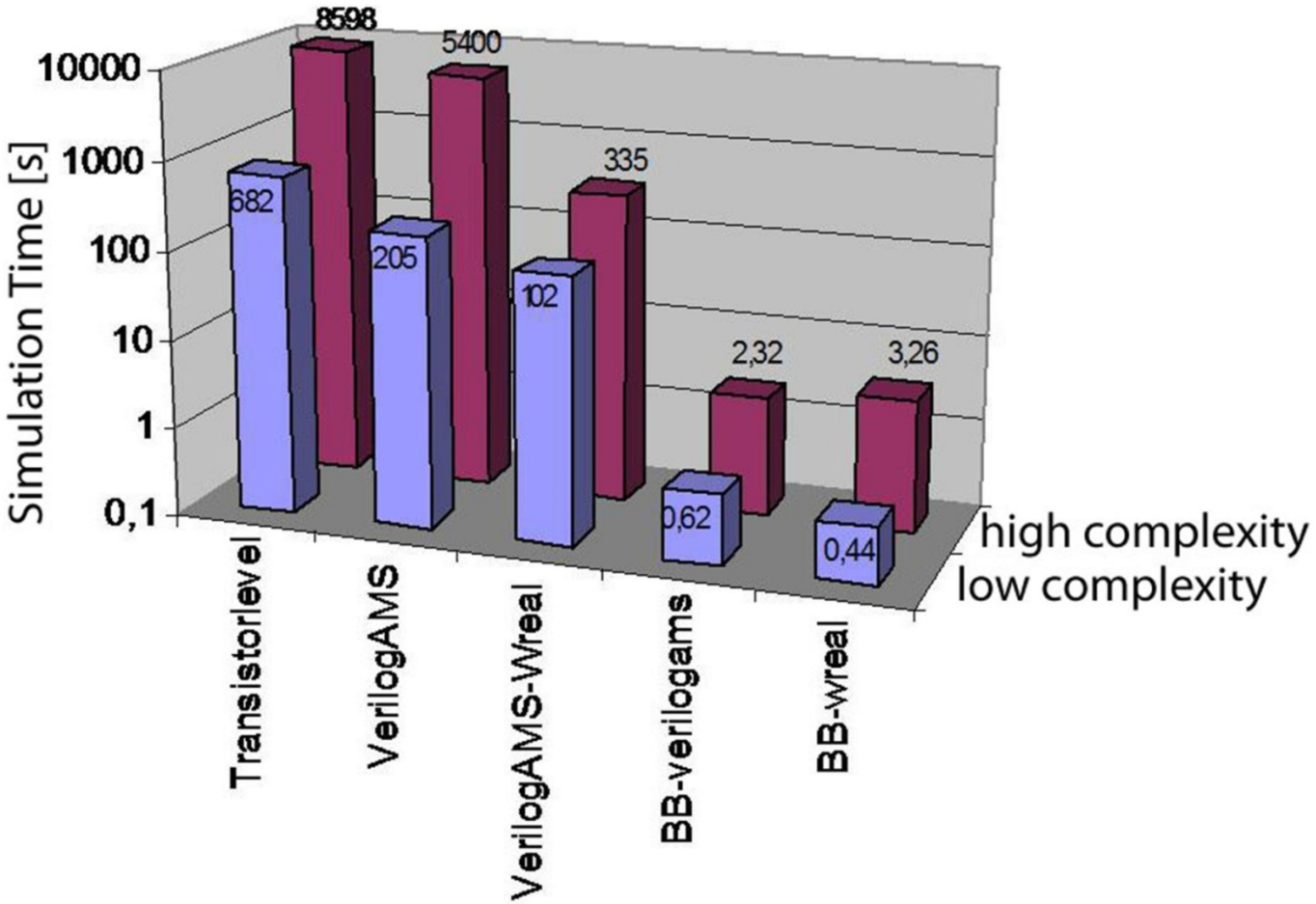
2.41GHz + 2.4GHz = 4.801 GHz

It is clear that 4.801GHz are filtered by the output stage of the mixer, or at least with the first lowpass filter in the next stage.

Solution : Integrate adequate filtering and choose voltage resolution at output wisely !

Block	Voltage	Uniform	Nonuniform	ΔA
LNA	5 µVpp	2.4 GHz * 10	2.4 GHz * 21	0.955 µV
Mixer	5 mVpp	1 MHz * 10	1 MHz * 21	0.955 mV

Simulation Results for (parts of) a commercial available BT-Receiver FE



Conclusion and Future Work

- Methods to use wreal modeling for RF frontends with different voltage levels and different oversampling demands have been proposed.

- The simulation time for the RF Frontend of a large receiver was reduced by about a factor of 26.

To Do :

- Define FOM for accuracy/speed tradeoff of modeling
  - Analog measures (NF, Gain, …) are not possible to be simulated with the proposed approach – no AC analysis, no sensitivity, noise, pss, pnoise …
  - „Digital“ measures (BER, EVM) are difficult to be simulated with the original schematic

- So – what to compare, if necessary ?

End

I would be glad to have a discussion
on this and accompanying questions
to continue my PhD work.

Email: joeres@ias.rwth-aachen.de

Special thanks to the german government, which is supporting this work as part of the VeronA-Project 01M3079.