BMAS
Behavioral Modeling and Simulation Conference
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IEEE

RF Library based on Block Diagram and Behavioral descriptions

Benjamin Nicolle [1,2], Jean-José Mayol [2],
William Tatinian [1], Jean Oudinot [2], Gilles Jacquemod [1]

1. Laboratoire d'Electronique Antennes et Télécommunications – UNSA CNRS UMR 6071 – 06560 Valbonne, France
2. Mentor Graphics – ZIRST Montbonnot – 38334 Saint Ismier, France

Contact : benjamin.nicolle@unice.fr

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Mentor Graphics®

Agenda

- **Introduction**
  - Classical simulation support
  - Proposed simulation support
  - ... and EDA Softwares ?
  - One solution with ADVance System Model Extractor (SME)
- **RF Library presentation**
  - Noise Figure implementation
  - Phase Noise implementation
  - RF blocks modeling summary
- **Transceiver simulation results**
  - Specifications extraction
  - Transceiver results
  - Focus on Transmitter
- **Conclusion**

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Mixing description languages to reduce development time, increase model accuracy

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Mixing description languages to simulate a complete application, reduce system complexity

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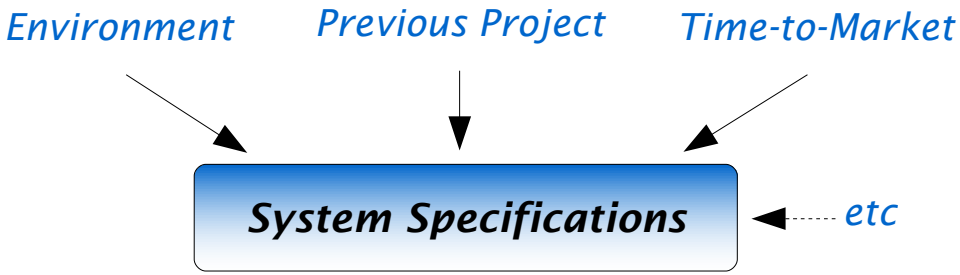
- *Classical simulation support*

Wireless application :



- *Classical simulation support*

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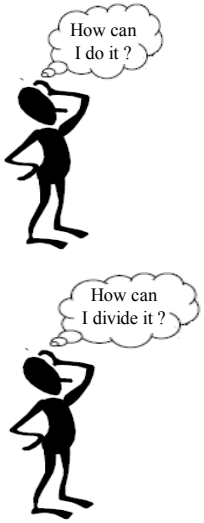
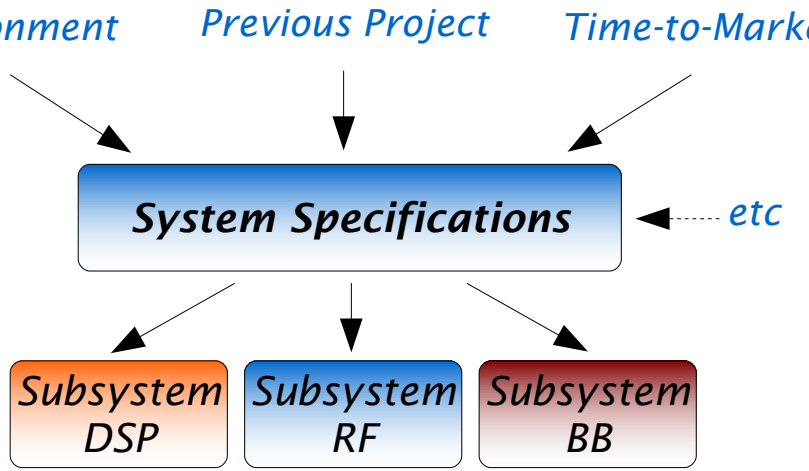
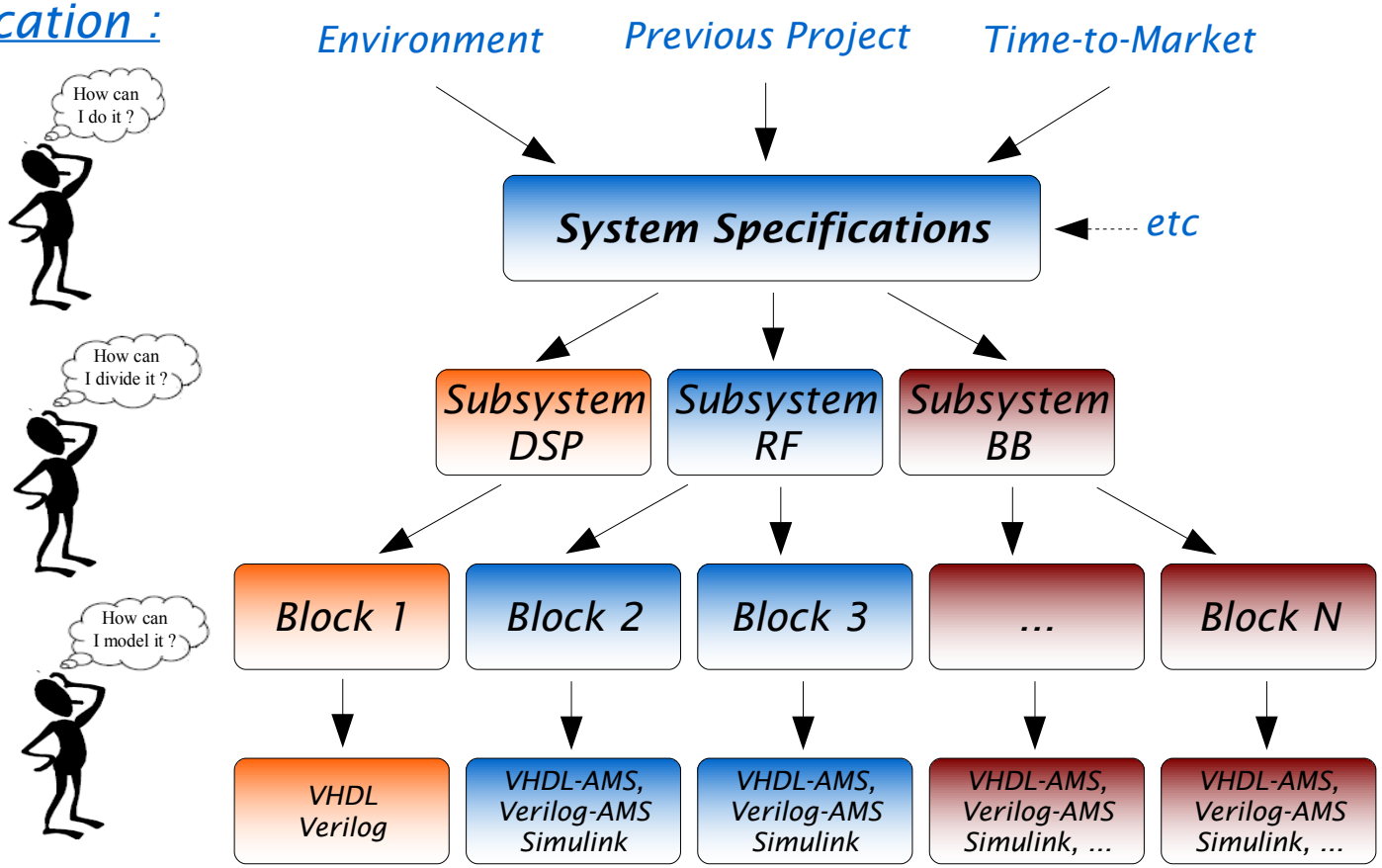




- Classical simulation support

Wireless application :



- Classical simulation support

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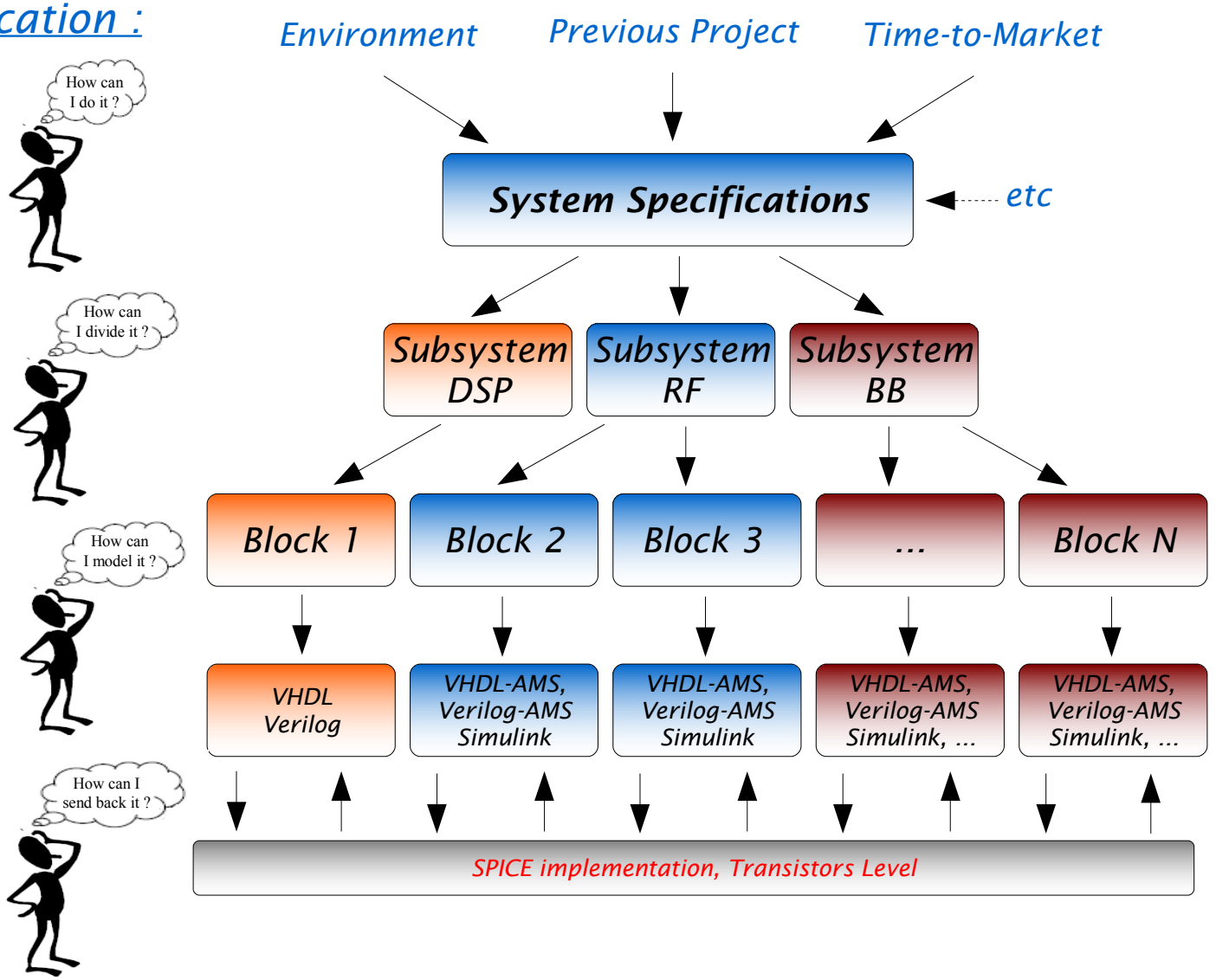
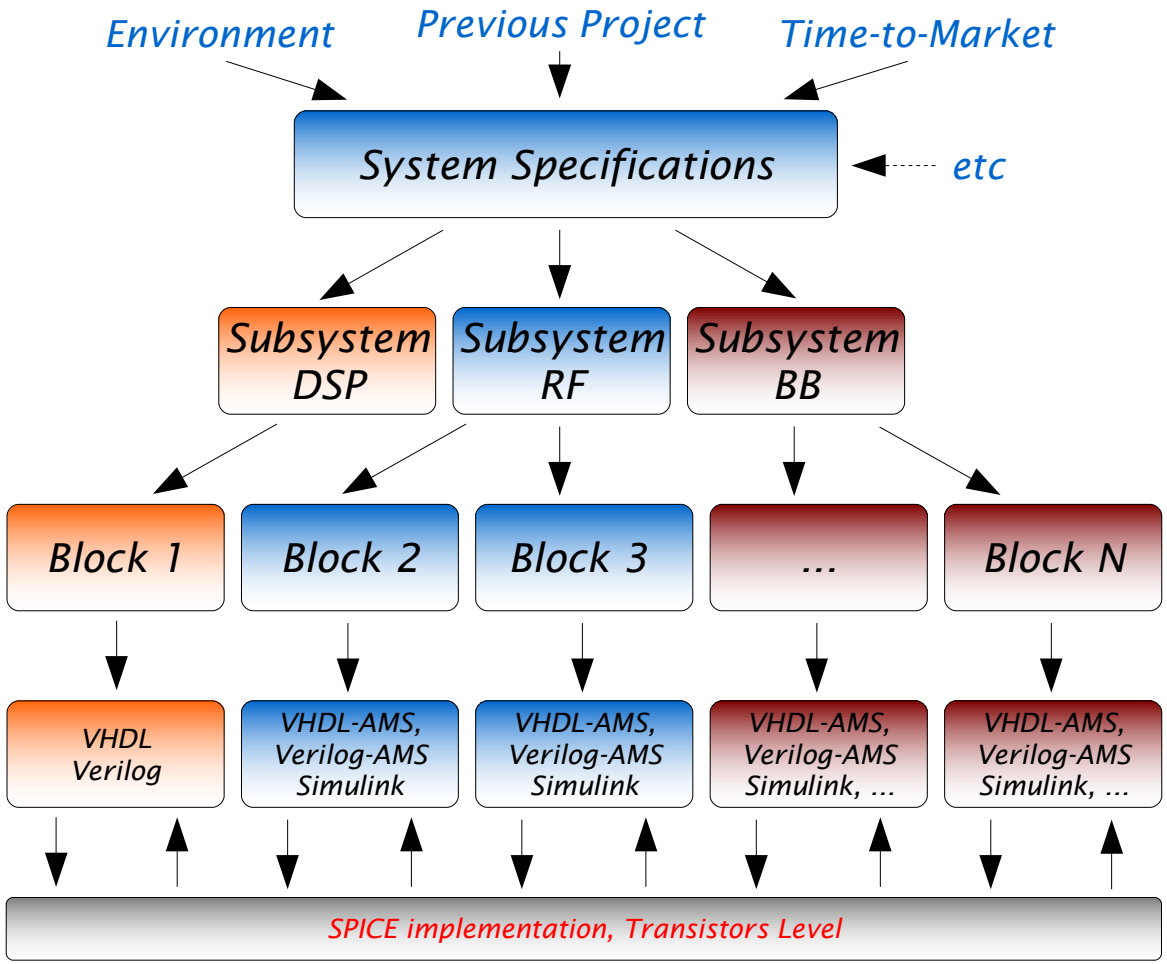


Classical simulation support



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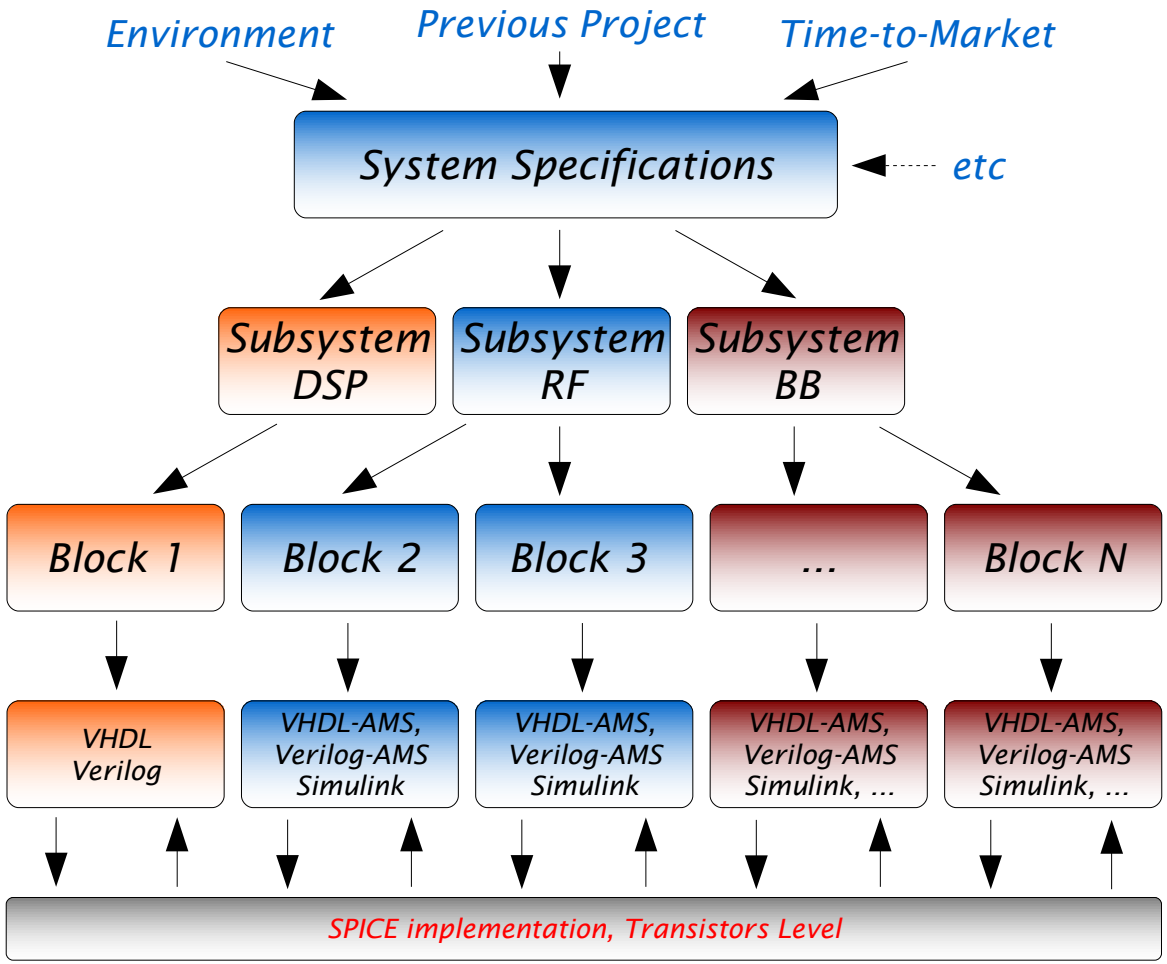
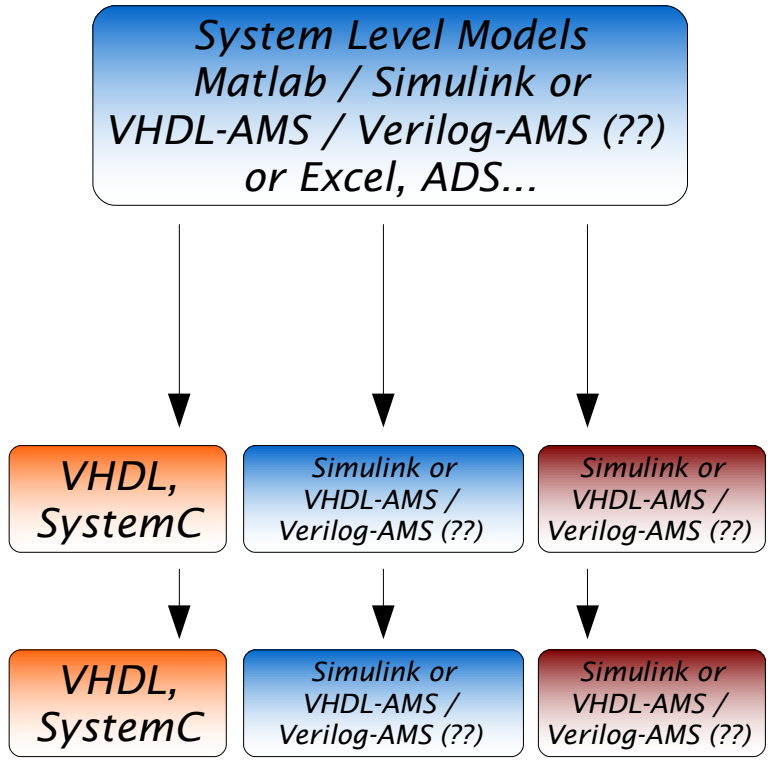
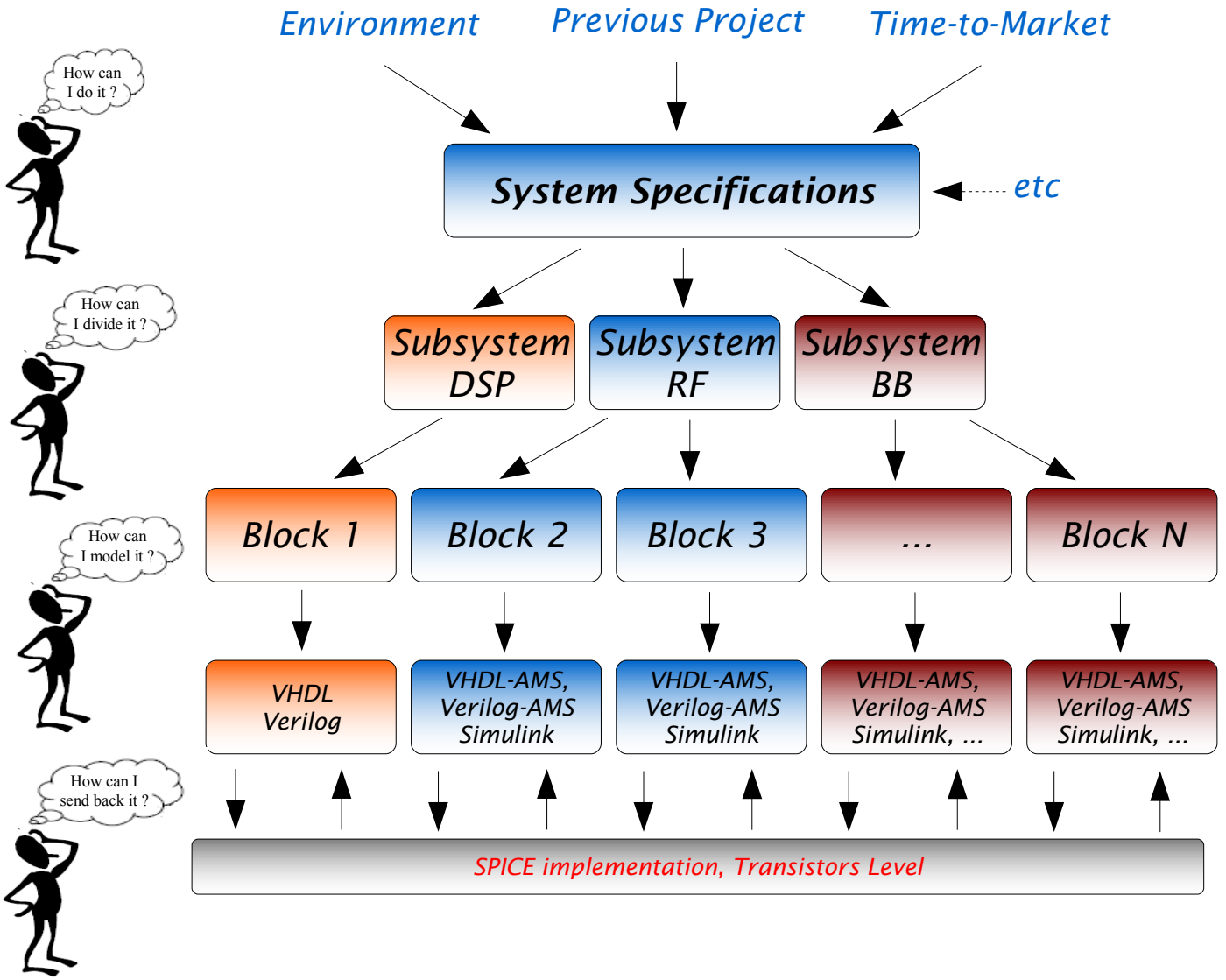




Proposed simulation support



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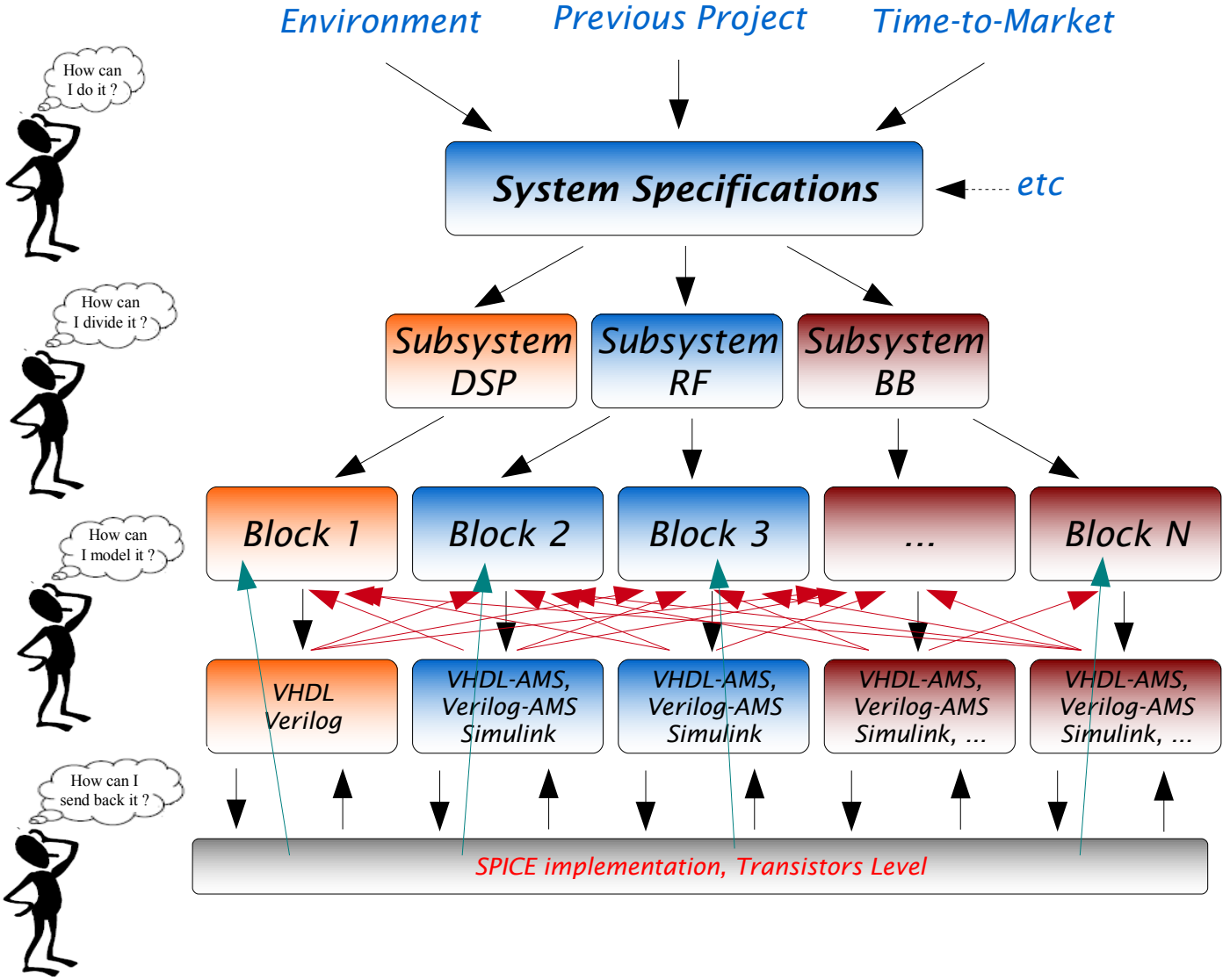
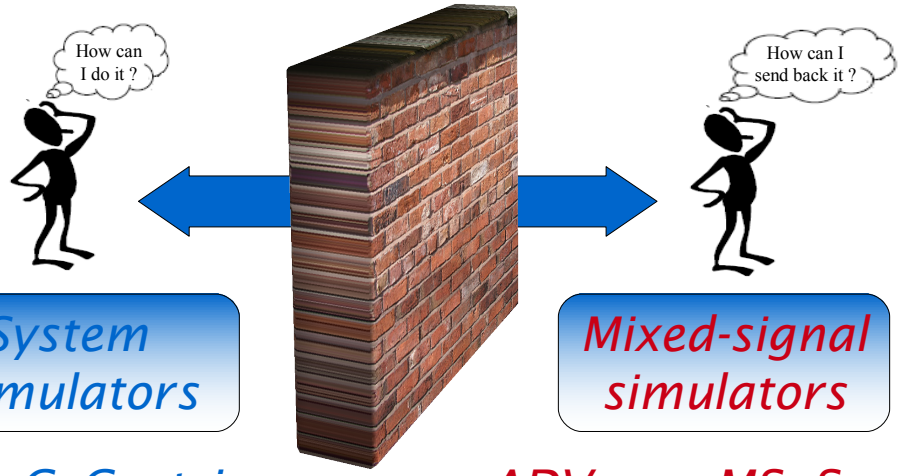
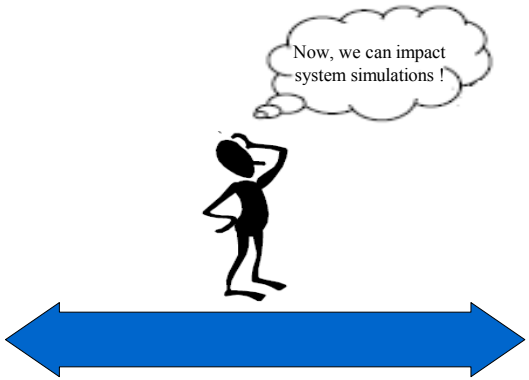


... and EDA Softwares ?



System Simulators	Mixed-signal simulators	Circuit Simulators	Layout Simulators
ADS, CoCentric, Matlab, Simulink, SPW, Excel ...	ADVance MS, Smash, AMS Designer, Saber ...	Eldo, Spectre, Spice, ADS ...	Assura, Calibre, Hercules ...

- *... and EDA Softwares ?*



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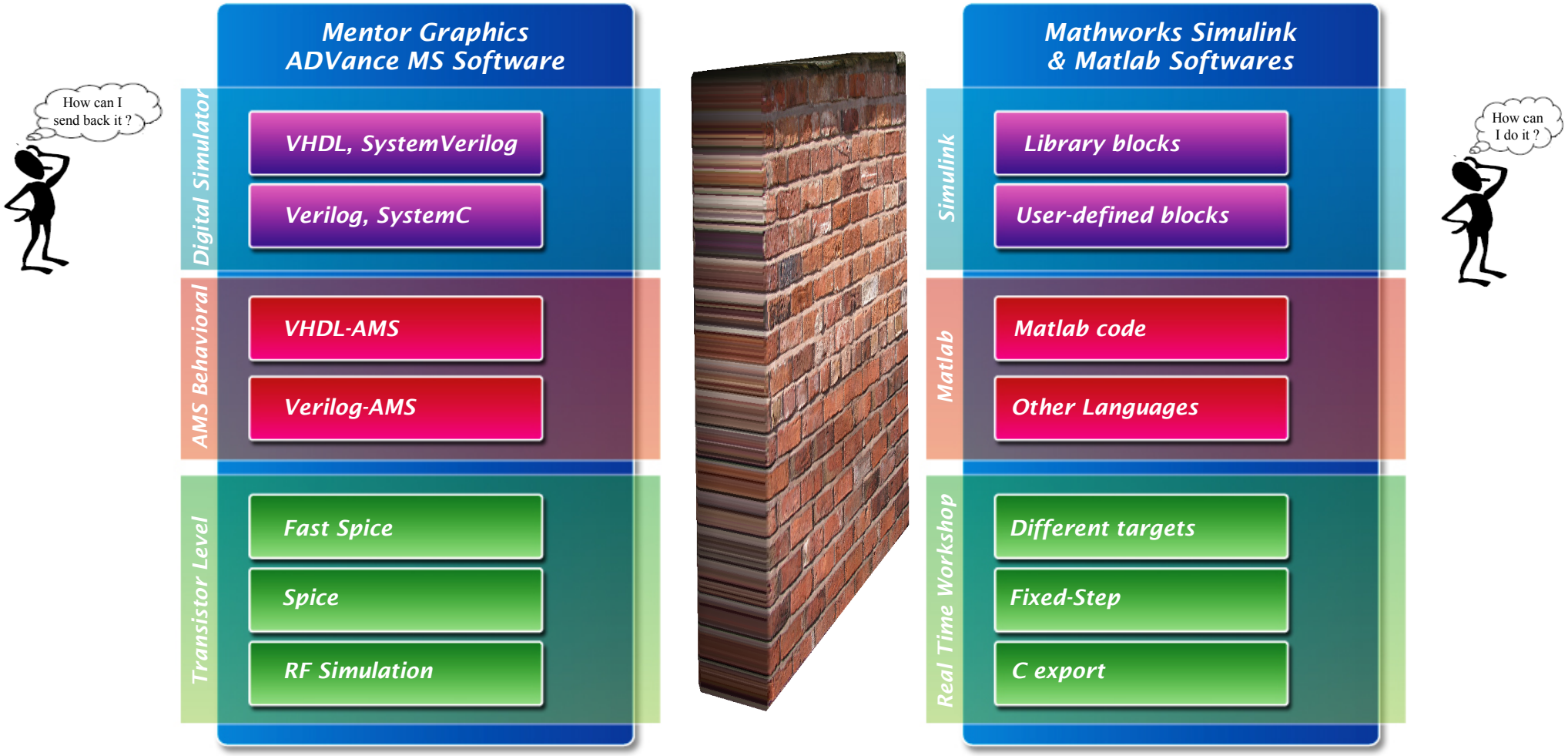
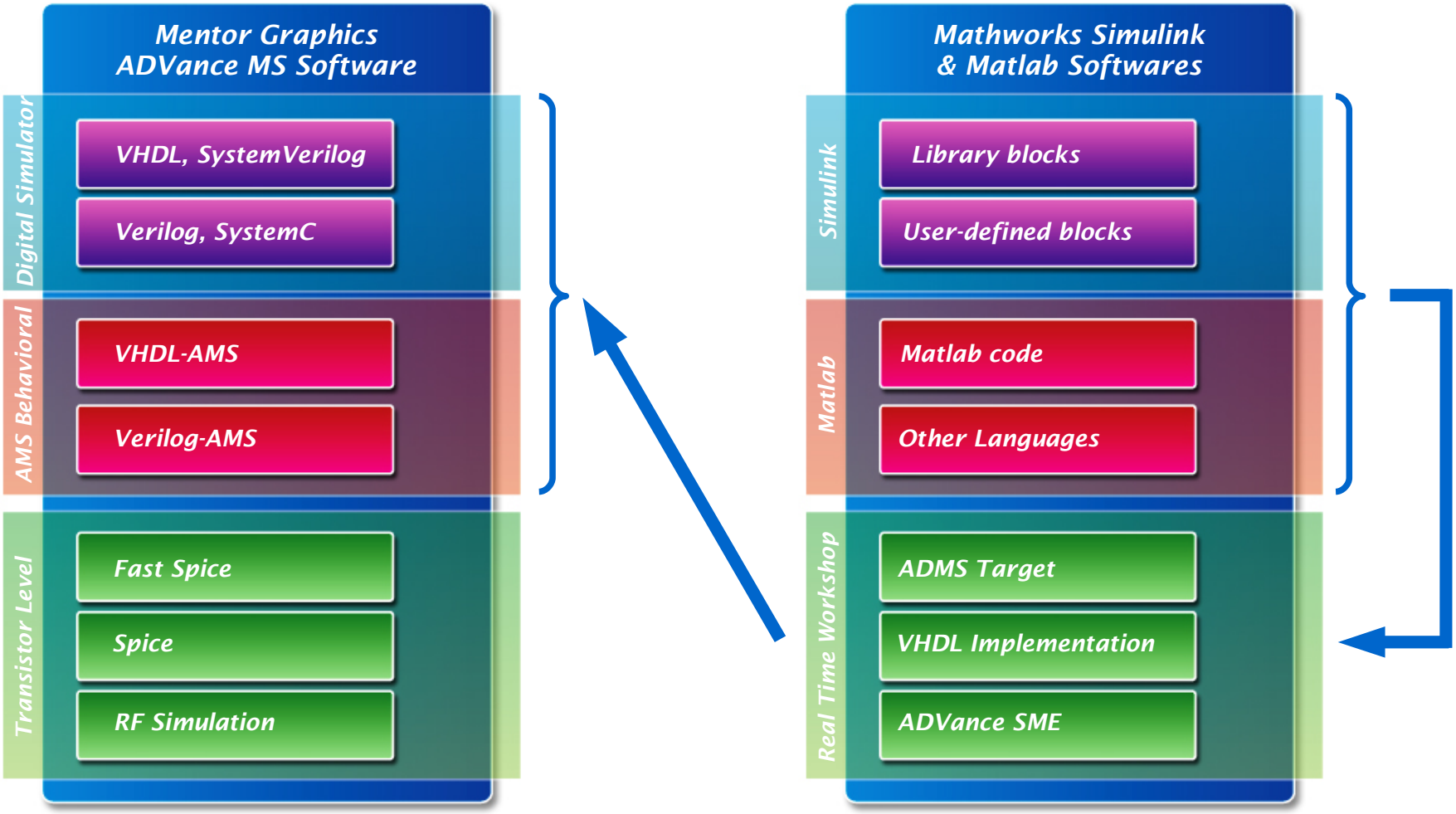
One solution with ADSME



One solution with ADSME



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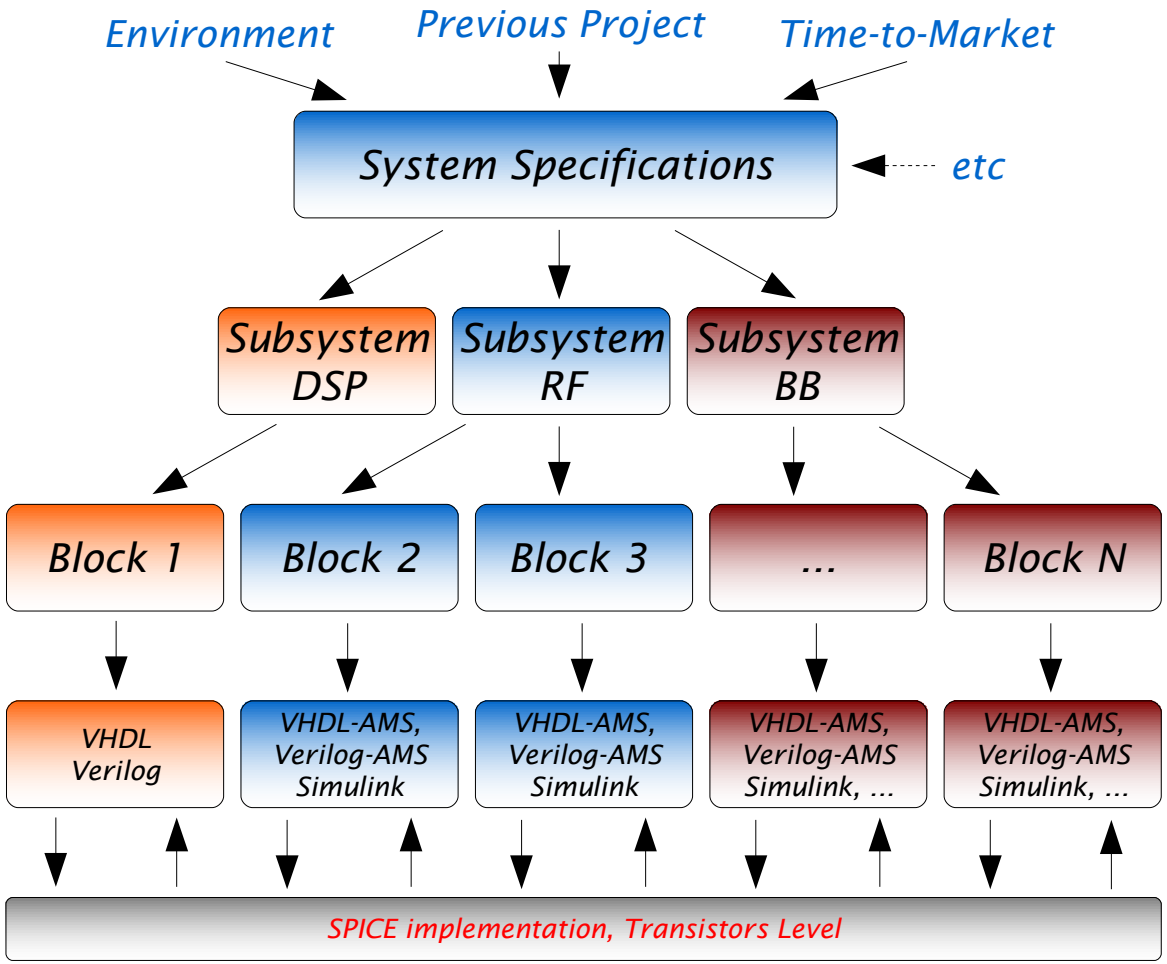

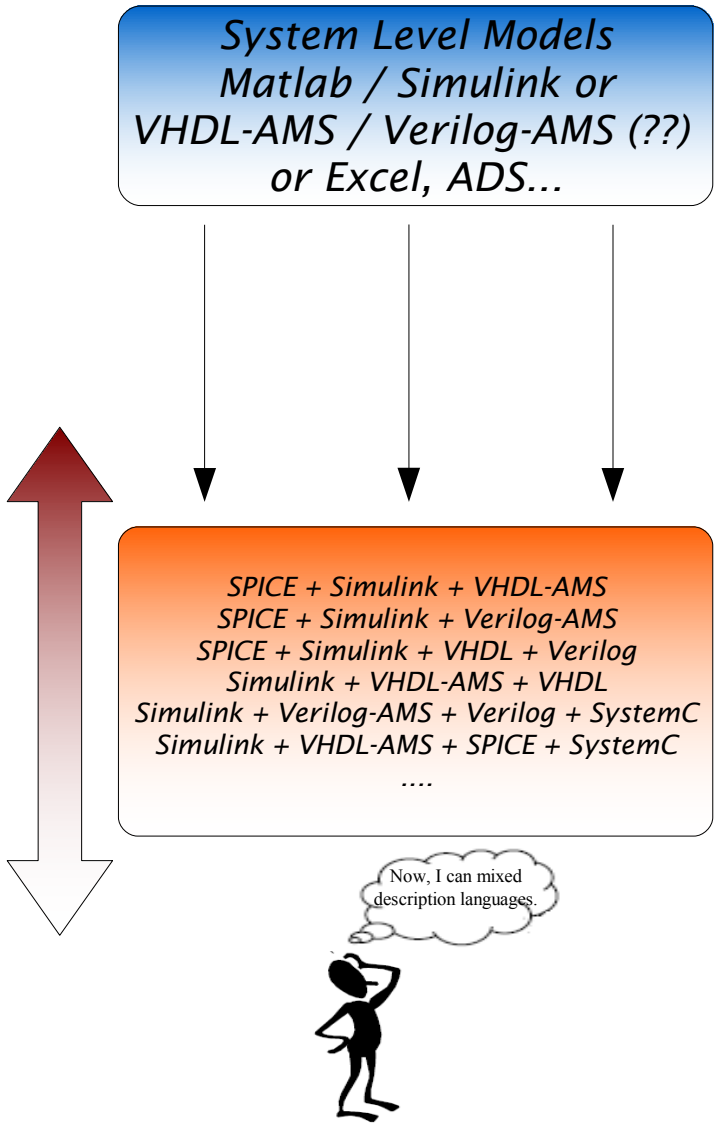

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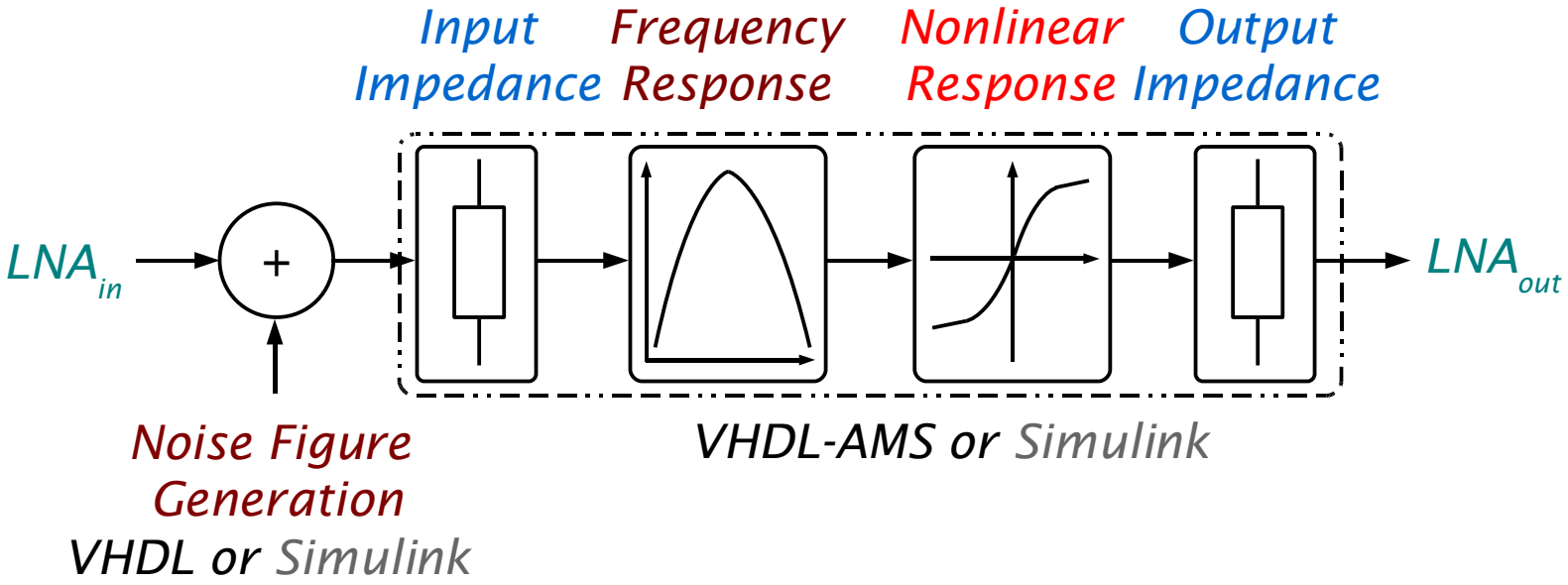
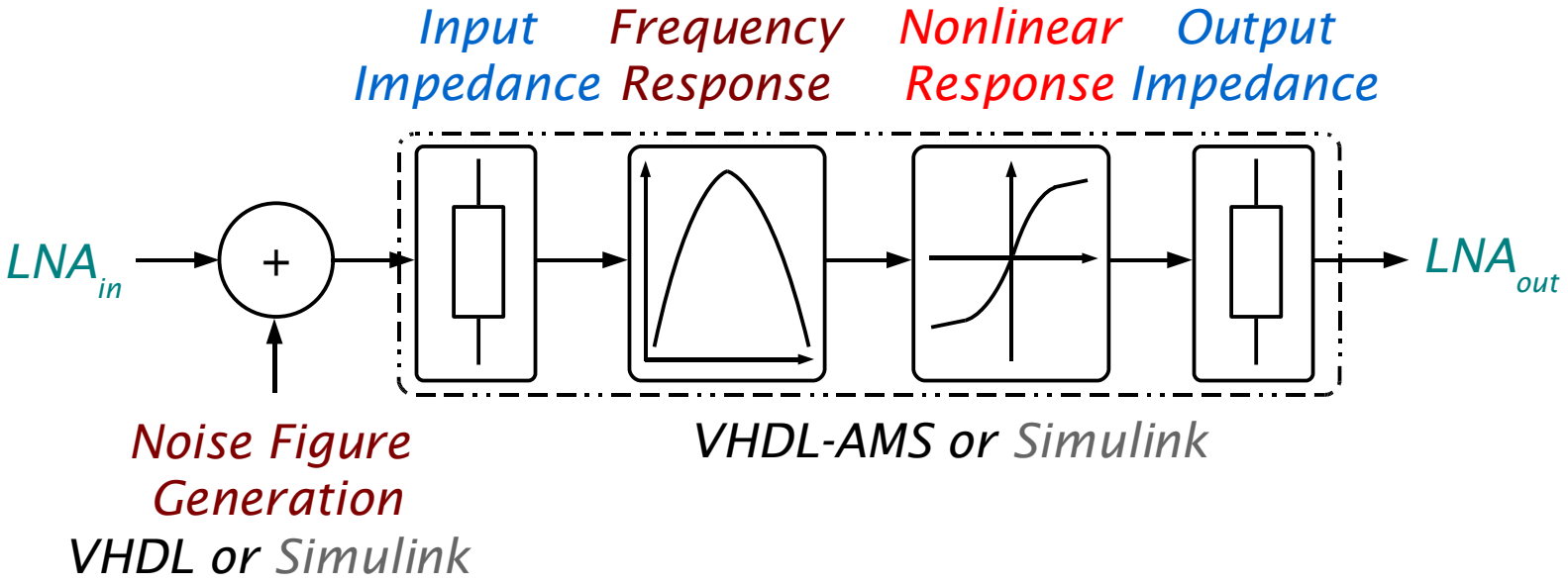
LNA (1) :


Input Impedance
Frequency Response
Nonlinear Response
Output Impedance
LNA in
+
LNA out
Noise Figure Generation
VHDL or Simulink
VHDL-AMS or Simulink

LNA (1) :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LNA_in
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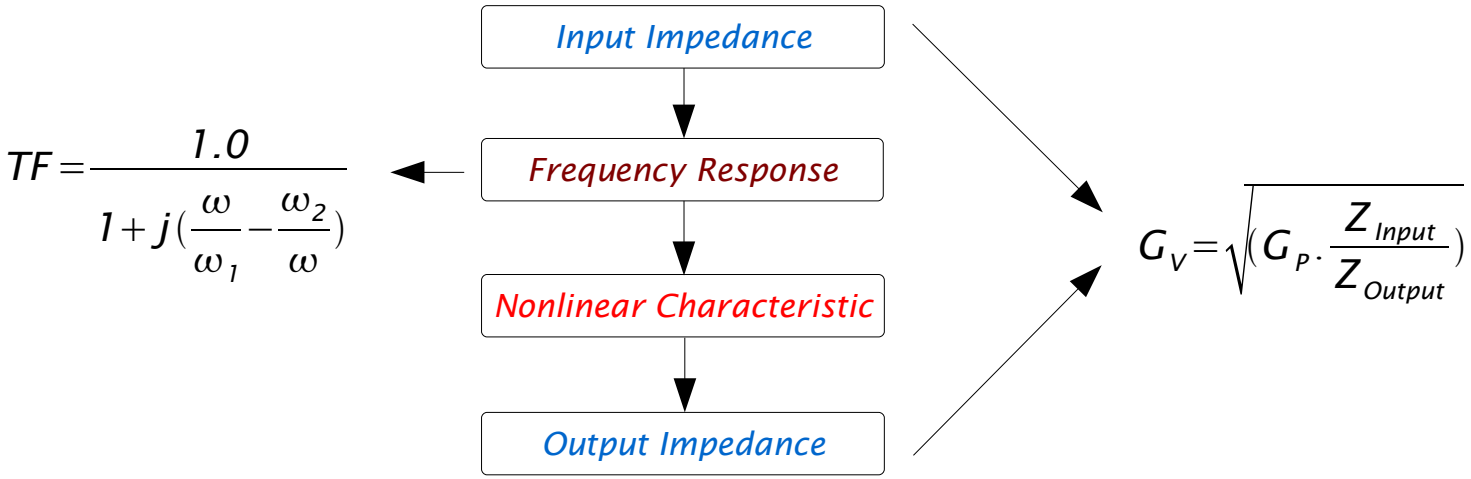
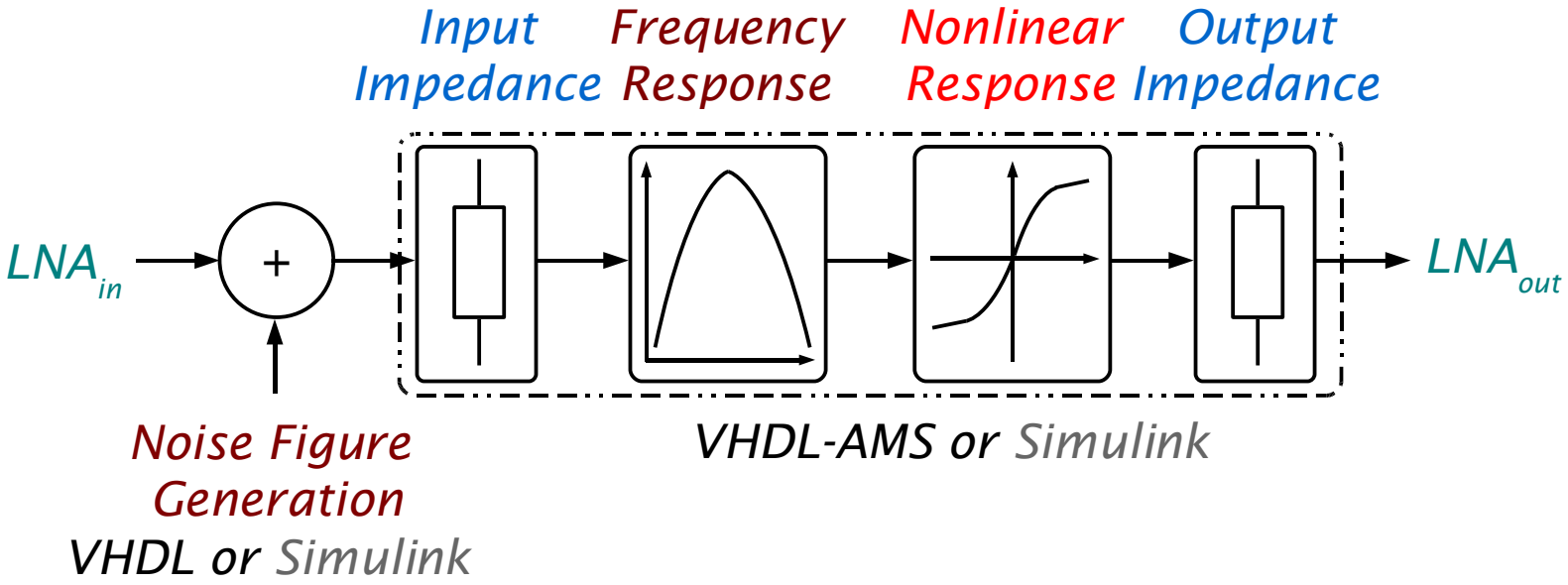

Input Impedance
Frequency Response
Nonlinear Characteristic
Output Impedance
$TF = \frac{1.0}{1 + j(\frac{\omega}{\omega_1} - \frac{\omega_2}{\omega})}$
$G_V = \sqrt{(G_P \cdot \frac{Z_{Input}}{Z_{Output}})}$

LNA (2) :


Input Impedance
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Output Impedance
LNA in
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VHDL or Simulink
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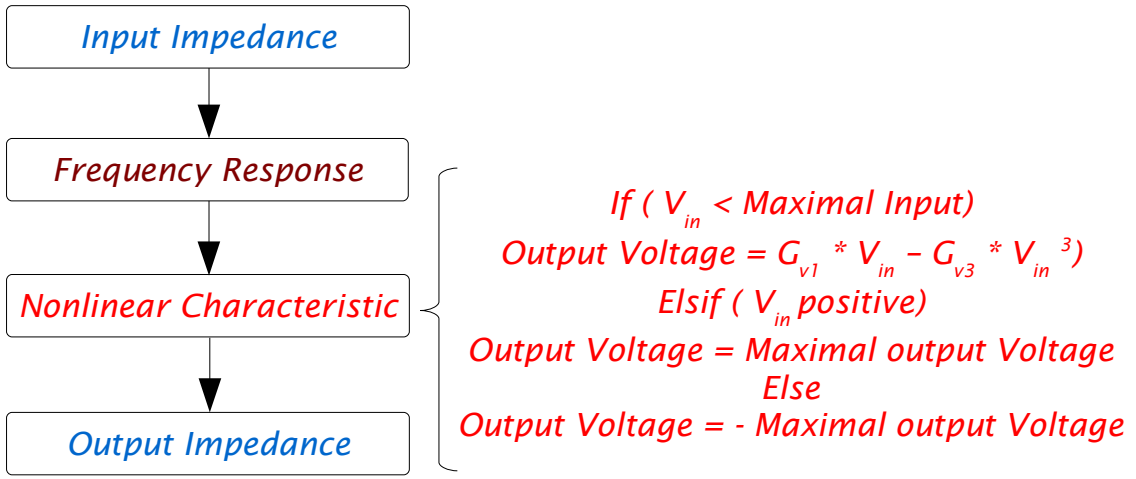
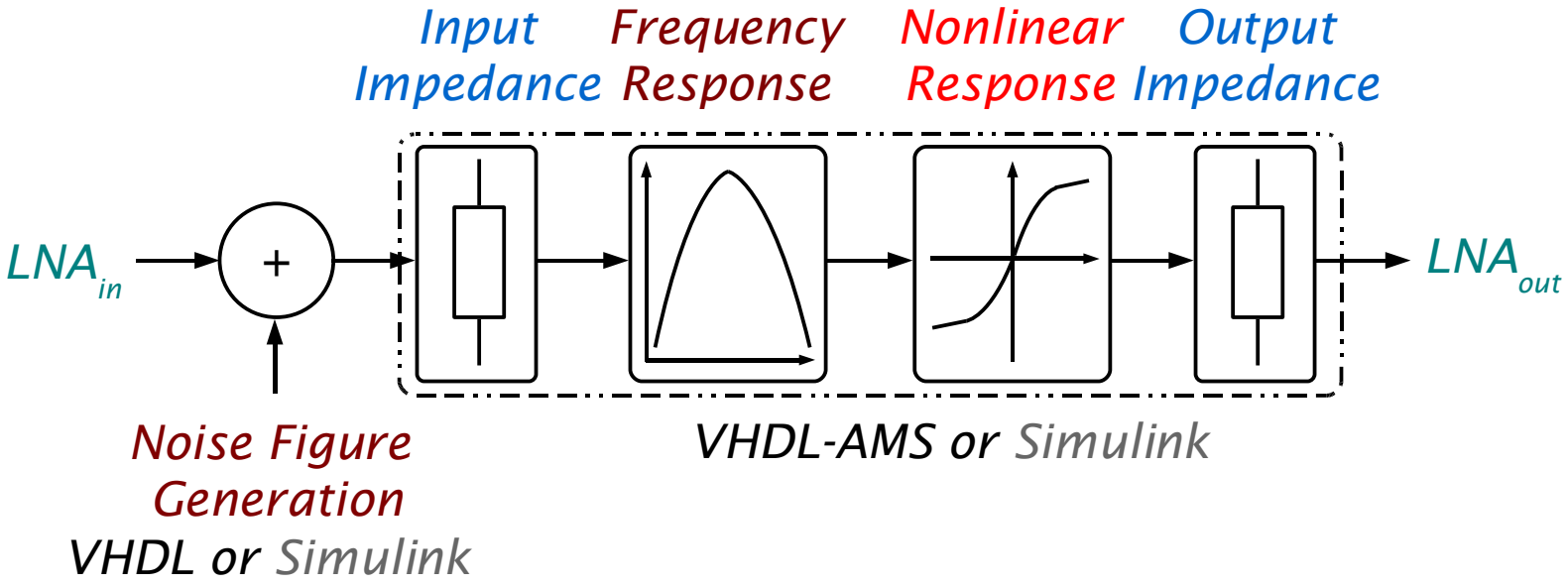
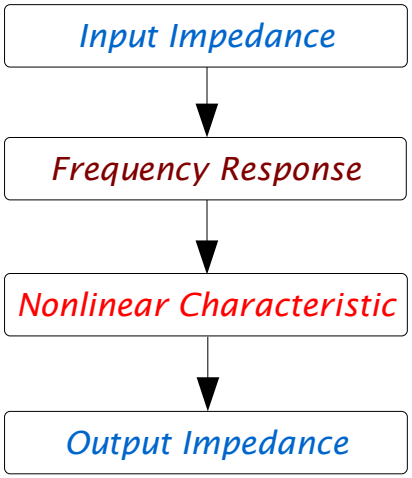

Input Impedance
Frequency Response
Nonlinear Characteristic
Output Impedance
If (V in < Maximal Input)
Output Voltage = G v1 * V in – G v3 * V in 3)
Elsif (V in positive)
Output Voltage = Maximal output Voltage
Else
Output Voltage = - Maximal output Voltage

LNA (3) :

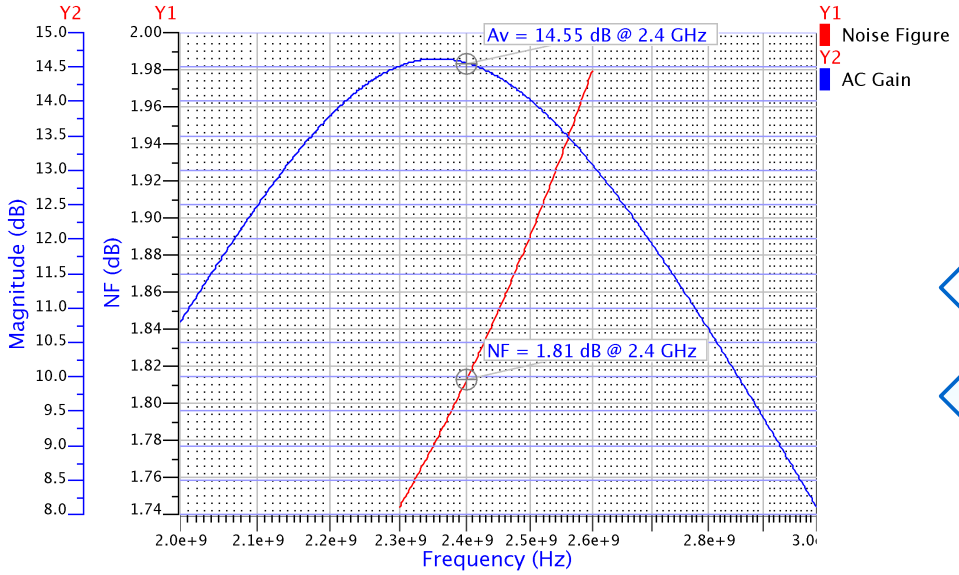


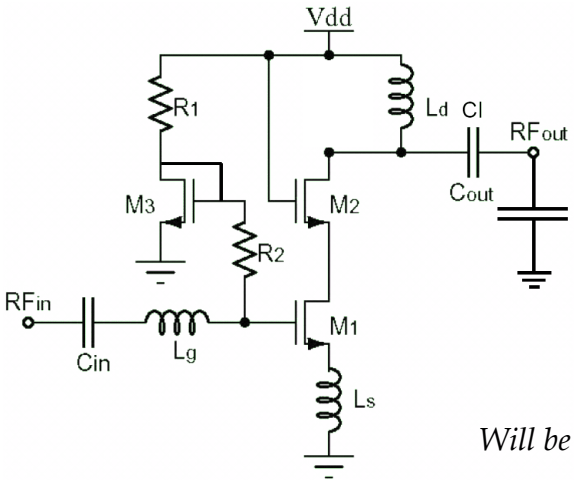
$$\overline{v_{noise}^2} = 4 \cdot k_B \cdot T_0 \cdot R_{Input} \cdot (F-1)$$



LNA (4) :

Voltage gain & NF extraction – SPICE Simulations

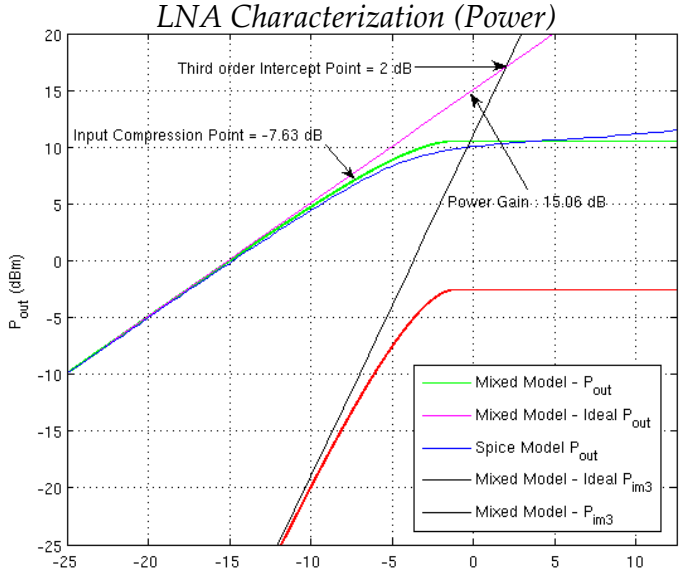




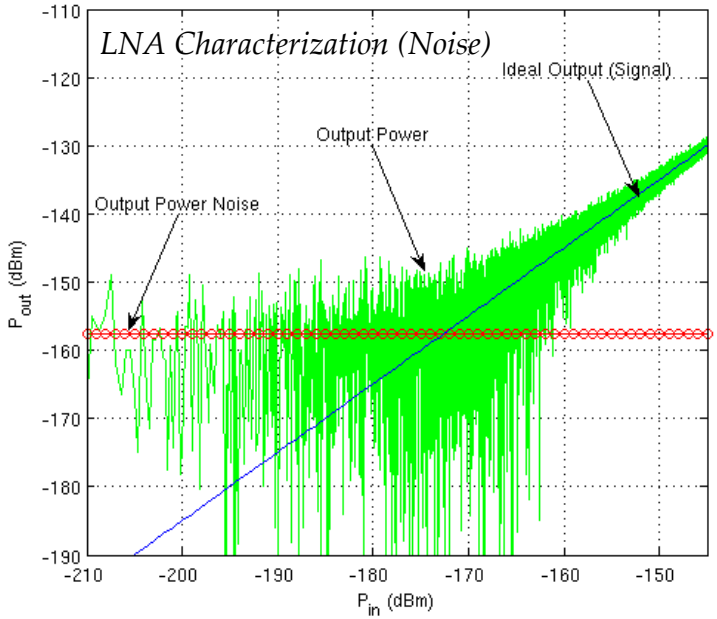
Parameters	Simulation
Power Gain	15.06 dB
ICP1	-7.63 dBm
Noise Figure	1.81 dB
Power	4.8 mW
Input Impedance	49.48 Ω
Output Impedance	50.09 Ω

Will be presented on IEEE ICECS 2007 - Morocco

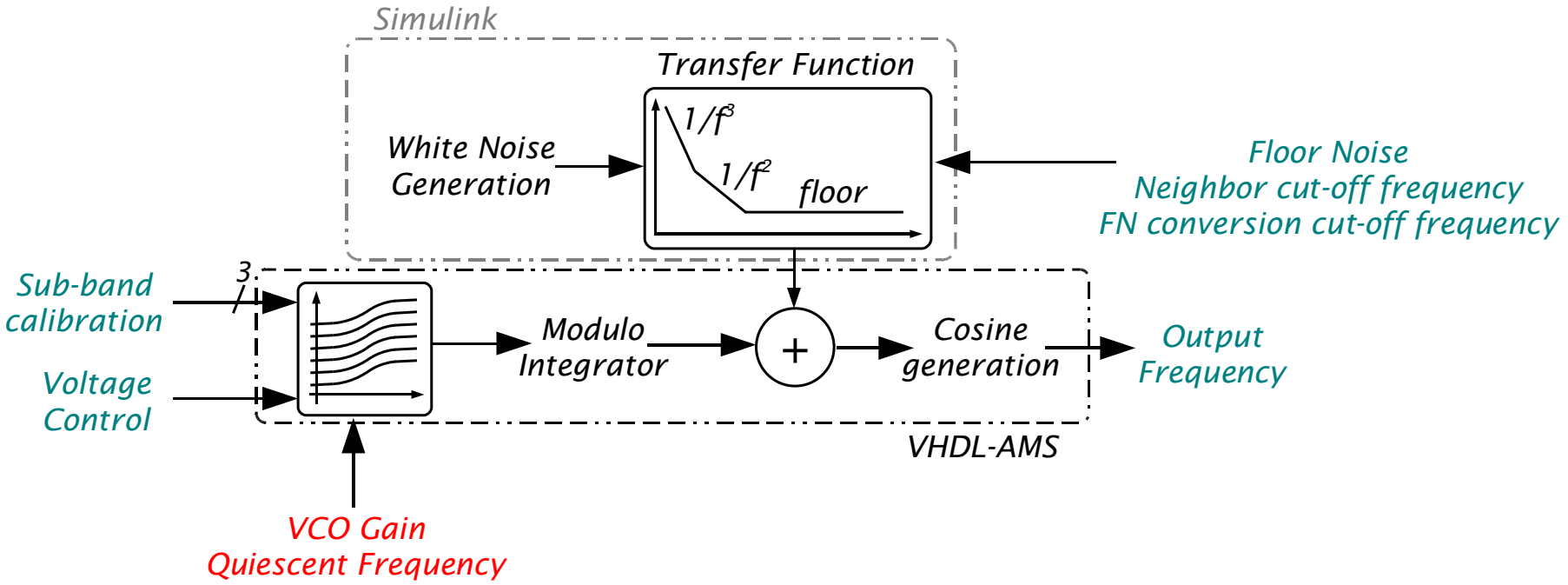
LNA Characterization (Power)



LNA Characterization (Noise)

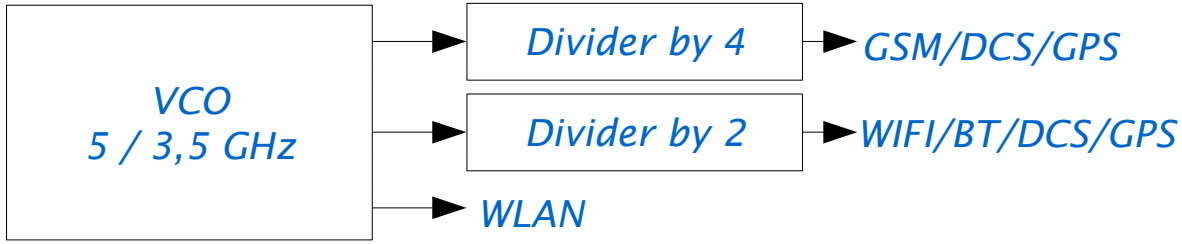


VCO (1) :

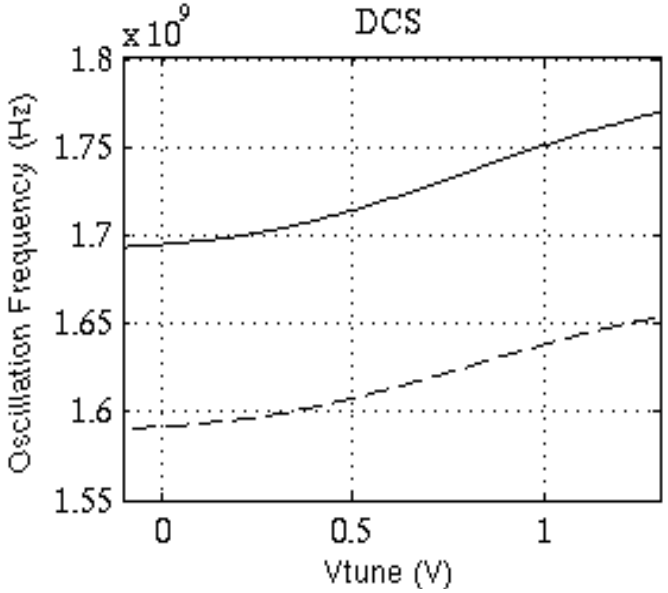

Simulink
Transfer Function
White Noise Generation
1/f³
1/f²
floor
Floor Noise
Neighbor cut-off frequency
FN conversion cut-off frequency
3
Sub-band calibration
Voltage Control
Modulo Integrator
+
Cosine generation
Output Frequency
VHDL-AMS
VCO Gain
Quiescent Frequency

VCO (2) :

VCO Architecture

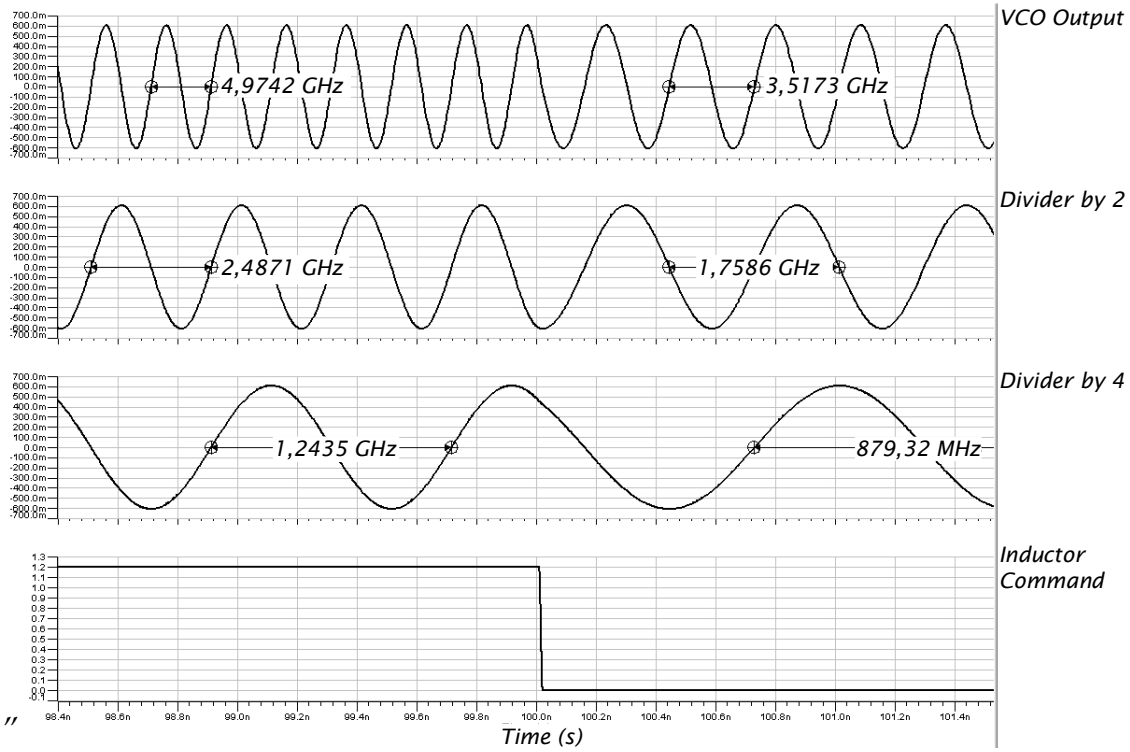


- Multiple VCO gains
- Multiple PN characteristics
- Multiple behaviors



Frequency Variation Modeling

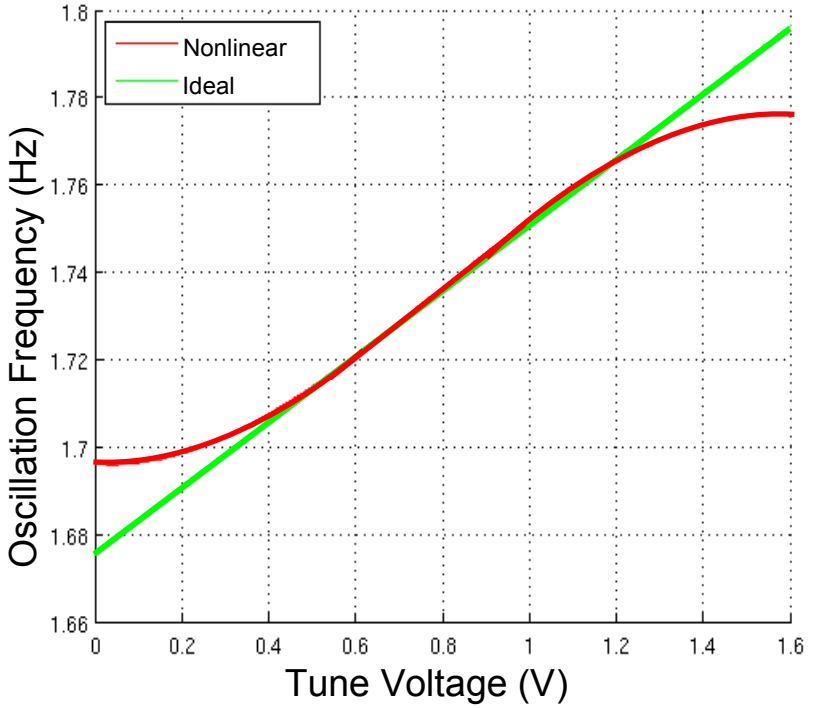
Transient VCO Modeling



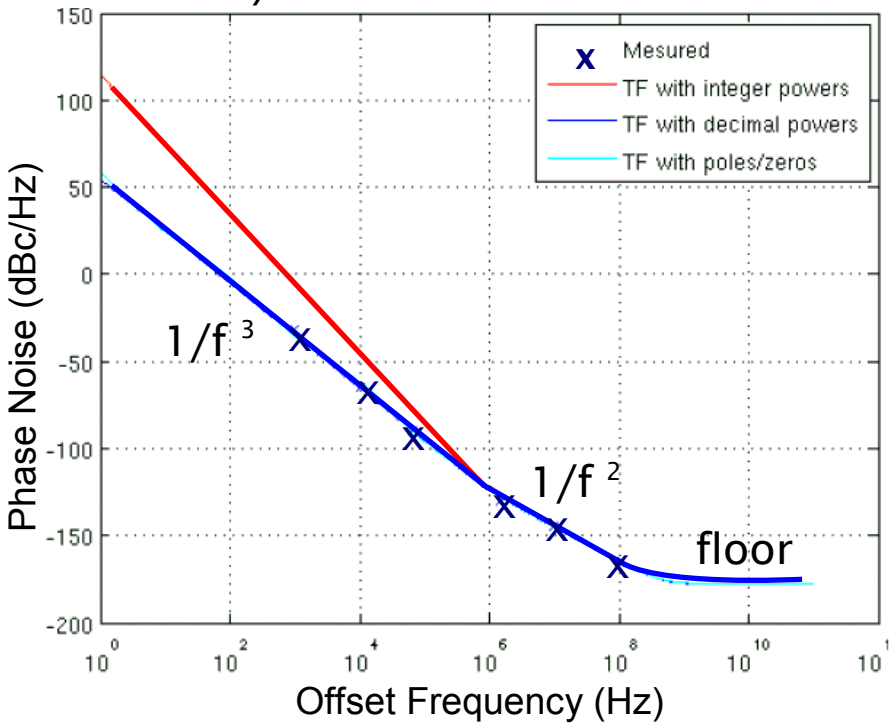
More details in SAME 2005 – B. Nicolle et al.
"High Level Modelling of ΣΔ Fractional PLL for Noise Estimation"

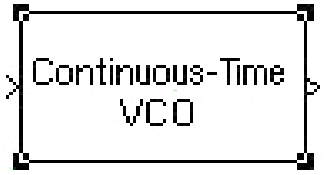
VCO (3) :

Simulink Model (included & user-defined)



Noisy VCO model in Simulink





- *Output Amplitude Voltage (V)*
- *Quiescent Frequency (Hz)*
- *VCO Gain (Hz/V)*
- *Initial Phase (rad)*
- *Neighbor Noise Frequency (Hz)*
- *Floor Noise Frequency (Hz)*
- *Floor Noise Level (dBc/Hz)*

More details in RFIC 2007 – B. Nicolle et al.
"Top-Down PLL Design Methodology combining Block Diagram, Behavioral and Transistor Level Simulators"

Low Noise Amplifier :	Power Gain, 3rd order Intercept Point, Input – Output impedance matching, Frequency, Noise figure	
Power Amplifier :	Power Gain, 3rd order Intercept Point, Input – Output impedance matching, Frequency, Noise figure	
Mixer :	Power Gain, 3rd order Intercept Point, Input – Output impedance matching, Frequency, Noise figure and Phase Noise	
Filter :	Laplace modeling (or Z transform) Input – Output impedance matching, Noise figure	
Channel :	Input – Output impedance matching, Noise figure, Phase Noise, Distance, Frequency, IQ imbalance	

RF Library Presentation

Low Noise Amplifier :	Power Gain, 3rd order Intercept Point, Input – Output impedance matching, Frequency, Noise figure	2nd order Intercept Point
Power Amplifier :	Power Gain, 3rd order Intercept Point, Input – Output impedance matching, Frequency, Noise figure	2nd order Intercept Point
Mixer :	Power Gain, 3rd order Intercept Point, Input – Output impedance matching, Frequency, Noise figure and Phase Noise	2nd order Intercept Point, losses between ports
Filter :	Laplace modeling (or Z transform) Input – Output impedance matching, Noise figure	Any idea ??
Channel :	Input – Output impedance matching, Noise figure, Phase Noise, Distance, Frequency, IQ imbalance	(work in progress) Radiation pattern

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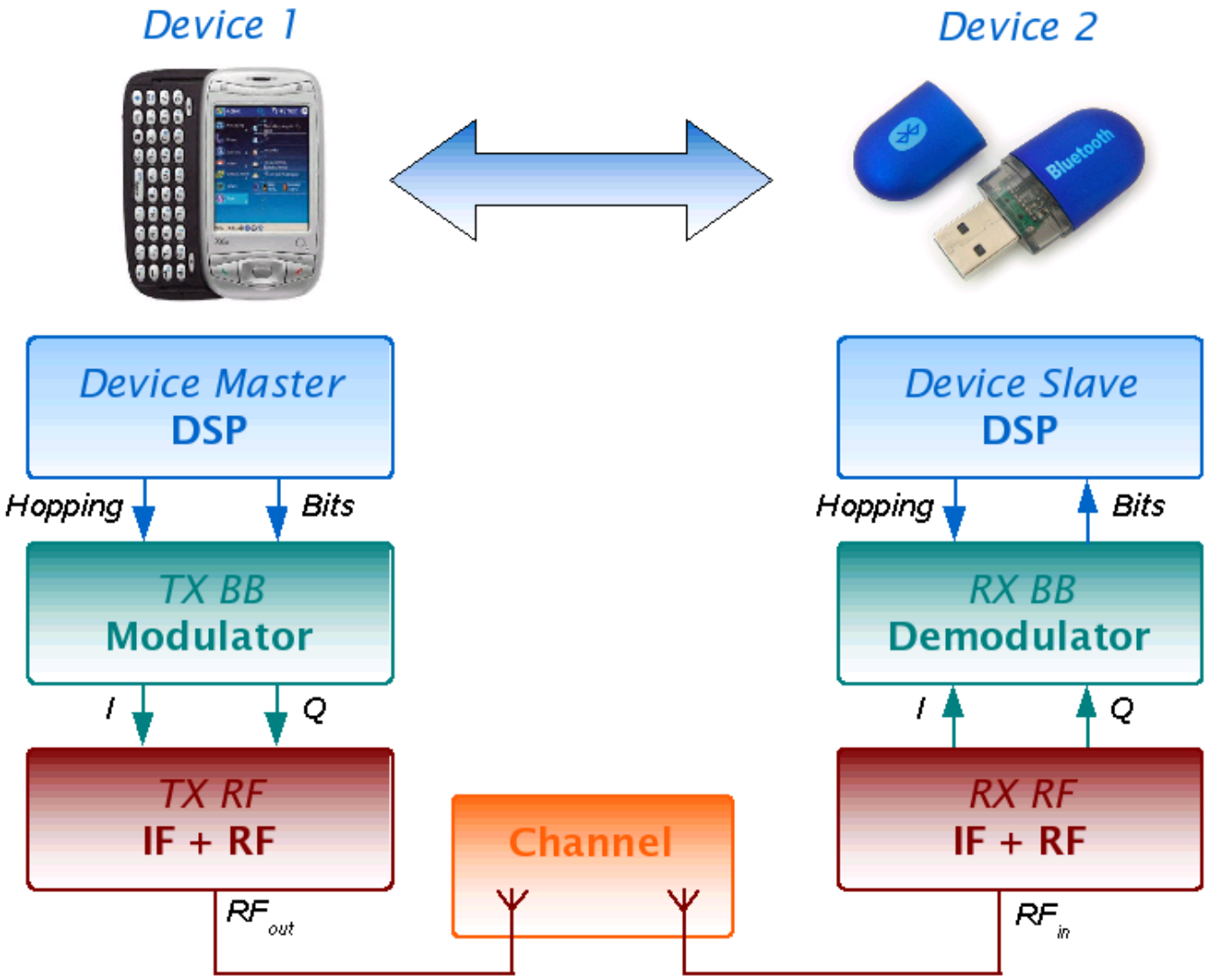
Bluetooth Transceiver (1) ?

Device 1

Device 2

Bluetooth Transceiver (2) ?



Transceiver simulation results

Requirements & objectives

- **Bluetooth RF Transceiver modeling => Block specifications extraction**

- **Bluetooth Baseband Transceiver modeling => Modulation & BER**

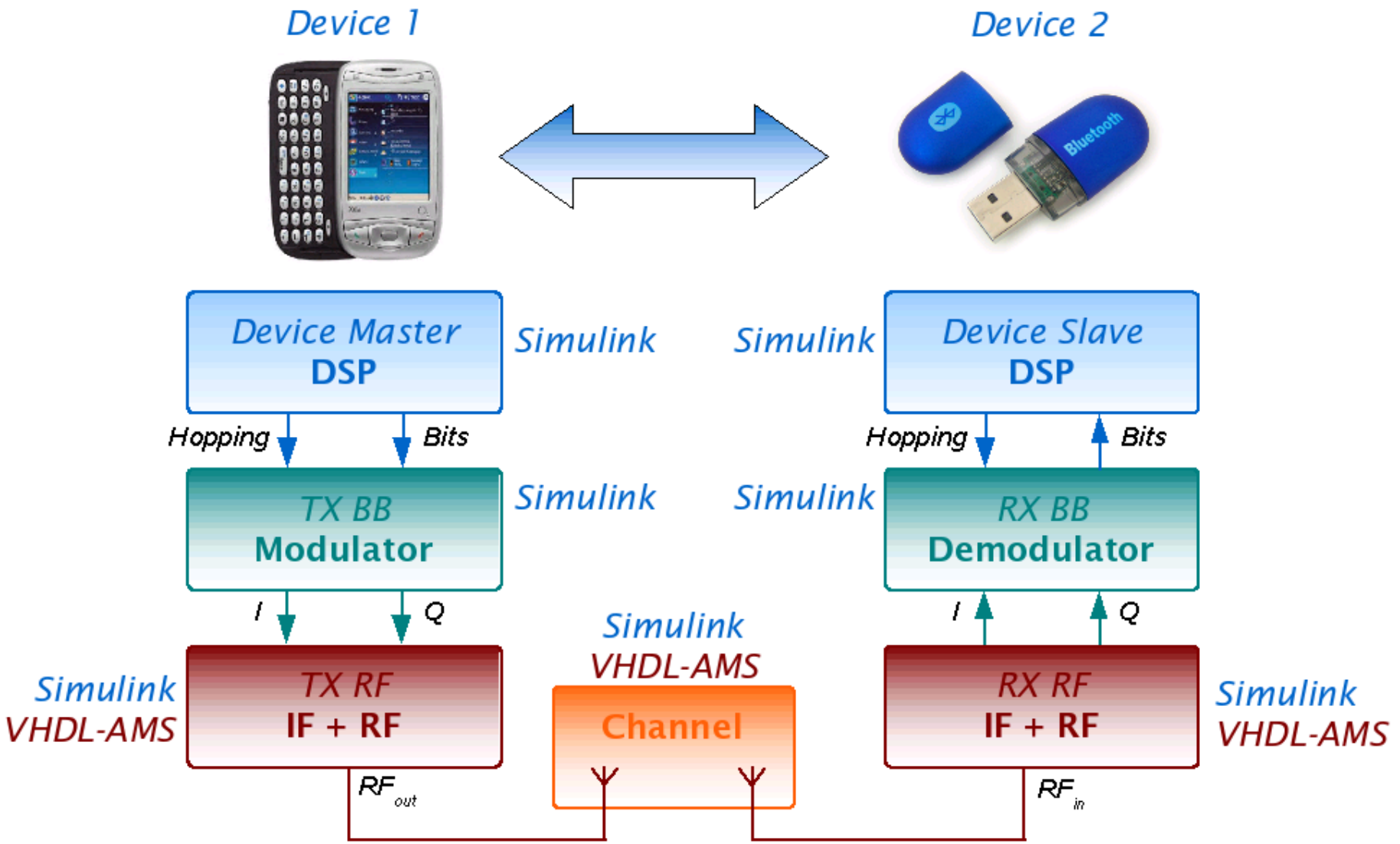
- **Objectives :**

Transceiver simulation results

Requirements & objectives

- ***Bluetooth RF Transceiver modeling => Block specifications extraction***
  - *2.4 GHz ISM Band – Receiver Sensitivity : -73 dBm - Power : 1mW to 100 mW*
  - *Quadrature waveforms I/Q – Data Rate : 1 Mbps (1,2,3 bits symbol)*
  - *Transmitter & Receiver with dual-conversion technique (2,4 / 1,6 / 0,8 GHz)*
  - *Need of a RF library with key generic and critical parameters :*
    - *LNA : Gain, IP3 & Noise Figure, Impedance Mismatches*
    - *PA : Gain, IP3 & Impedance Mismatches*
    - *Mixers : Gain, IP3 & Noise Figure, Phase Noise & Impedance Mismatches*
    - *Channel : Distance, Frequency & Attenuation, Phase Noise, White Noise Adjunction*
- ***Bluetooth Baseband Transceiver modeling => Modulation & BER***
  - *Bit Error Rate = 0.1%*
  - *Gaussian Frequency Shift Keying (GFSK) + Frequency Hopping (from -39 to 39 MHz)*
- ***Objectives :***
  - *Adjust the RF Block Specifications to match BER*
  - *BT Transceiver Model with hierarchical level (Simulink / ADMS / SPICE)* ***and mixes it !***
  - ***Bonus : Combines it with SystemC (protocol / baseband)***

Transceiver simulation results



Transceiver simulation results

Required Specifications for each blocks along the BT signal in the transceiver

	RF Transmitter				RF Receiver			
Blocks name	IF Mixers	RF Mixer	RF Filter	PA	LNA	IF Mixers	RF Mixer	IF Filters
Gain (dB)	5	5	0	15	20	4	4	-2
IIP3 (dBm)	25	25	x	30	-5	10	10	x
Noise Figure (dB)	15	15	x	x	1.8	x	x	2

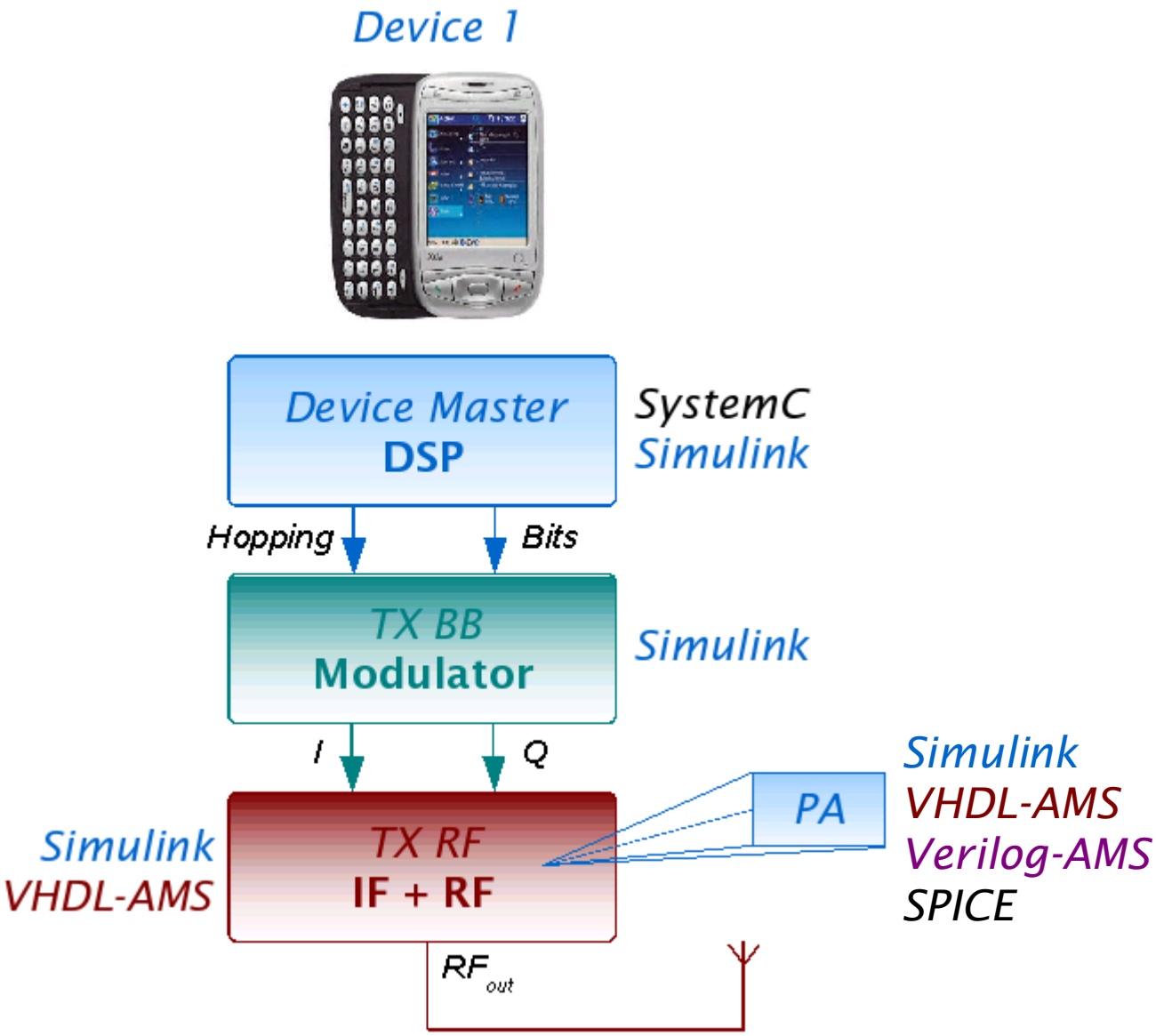
Transceiver simulations results (work in progress)

Software	MAC	Channel	PA	RX Mixers	TX Mixers	LNA	Elapsed	Bits	BER	1 bit	Obs.
Simulink	Simulink	Attenuation	Ideal	Ideal	Ideal	Ideal	30'	1211	0.0	1.49"	Ts=1e-10
Simulink	Simulink	Attenuation	Real	Ideal	Ideal	Ideal	38'	1051	0.0	2.17"	Ts=1e-10
Simulink	Simulink	Attenuation	Real	Real	Ideal	Ideal	49'	1033	0.0	2.84"	Ts=1e-10
Simulink	Simulink	Attenuation	Real	Real	Real	Ideal	14h17'	10780	0.0	4.77"	Ts=1e-10
Simulink	Simulink	Attenuation	Real	Real	Real	Real	81h	4270	0.0	68.29"	Ts=1e-11
Simulink	Simulink	Attenuation	Real	Real	Real	Real+NF	110h	6067	0.034	64.85"	Ts=1e-11
Simulink	Simulink	Attenuation	Real	Real	Real	Real+NF	96h	5495	0.469	62.89"	Ts=1e-11
ADMS	Simulink	No	No	No	No	No	67'	4333	0.0	0.928"	Without RF
ADMS	Simulink	Simulink	Sim.	Real	Real	Real	11h37'	3133	0.0	13.34"	Without NF
ADMS	Simulink	Simulink	Sim.	Real	Real	Real+NF	7h53'	2600	0.02	10.91"	With NF

Simulation time decreases by 5 ~ 6 x ratio

Allows mixed SPICE / Behavior / Simulink description levels (and SysC...) → (next point)

Transceiver simulation results



Transceiver simulation results

Bluetooth Emitter – Simulations comparison – 75 µs simulation time

Software	Bit – Hopping	Baseband part	RF part	Power Amplifier	Simulation Type	CPU Time (sec)	Elapsed Time (sec)	Ratio
Simulink	Simulink	Simulink	Simulink	Simulink	Fixed Step	NC	2755	1
ADMS	Simulink	Simulink	Simulink	Simulink	Transient – Dig.	309	473	5,82
ADMS	Simulink	Simulink	Simulink	VHDL-AMS (Our)	Transient	1171	1493	1,85
ADMS	Simulink	Simulink	Simulink	VHDL-AMS (Commlib)	Transient	1153	1397	1,97
ADMS	Simulink	Simulink	Simulink	Verilog-AMS (Commlib)	Transient	1180	1431	1,93
ADMS	Simulink	Simulink	Simulink	SPICE	Transient	3997	4386	0,63
ADMS	Simulink	Simulink	Simulink	VHDL-AMS (Commlib)	MODSST (RF + PA)	4301	5161	0,53
ADMS	Simulink	Simulink	Simulink	Verilog-AMS (Commlib)	MODSST (RF + PA)	5022	6026	0,46
ADMS	Simulink	Simulink	Simulink	SPICE	MODSST (RF + PA)	29570	29843	0,09
ADMS	SystemC	Simulink	Simulink	Simulink	Transient	276	378	7,29
ADMS	SystemC	Simulink	Simulink	VHDL-AMS (Commlib)	Transient	1108	1284	2,15
ADMS	SystemC	Simulink	Simulink	Verilog-AMS (Commlib)	Transient	1219	1400	1,97
ADMS	SystemC	Simulink	Simulink	SPICE	Transient	3891	4084	0,67

Conclusion (Simulink simulation basing)

- Simulink exported on ADMS → 6x faster
- Simulink exported on ADMS + SystemC → 7x faster
- Simulink exported plus behavioral languages and/or SystemC → 2x faster
- Simulink exported plus SPICE and/or SystemC → 1.4x slower but SPICE visibility (RF instructions)

Agenda

- **Introduction**
  - Classical simulation support
  - Proposed simulation support
  - ... and EDA Softwares ?
  - One solution with ADVance SME
- **RF Library presentation**
  - Noise Figure implementation
  - Phase Noise implementation
  - RF blocks modeling summary
- **Transceiver simulation results**
  - Specifications extraction
  - Transceiver results
  - Focus on Transmitter
- **Conclusion**

Conclusion

Combine description languages :

- To reduce system complexity,
- To increase model accuracy,
- To reduce some EDA software limitations (as Phase Noise for ADMS),
- To develop model faster !

Need a generic RF Library :

- To reduce simulation time,
- To allow model re-use with generic / critical parameters,
- To mix EDA softwares, mix system and circuit designers (utopia ?)

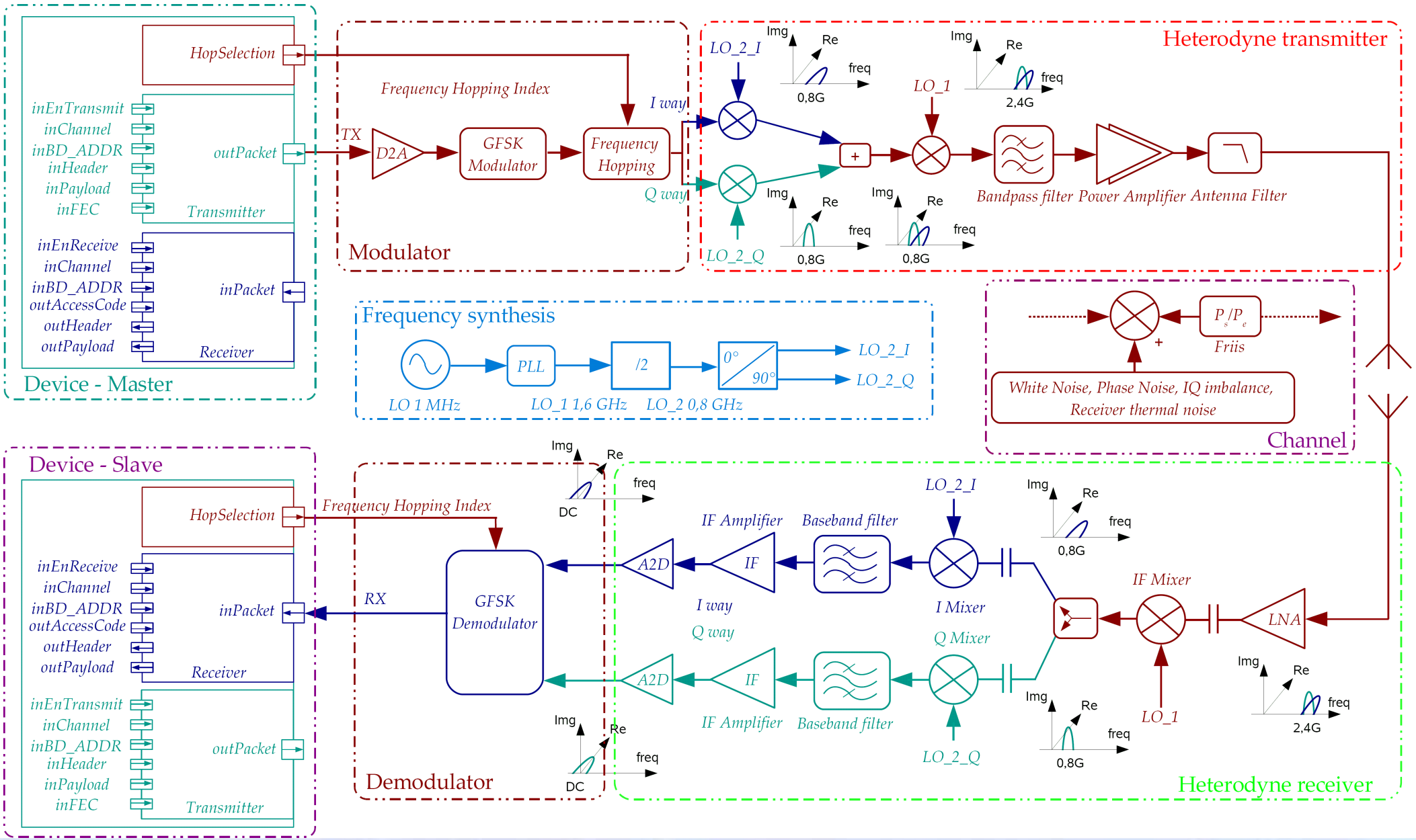
Conclusion on Transceiver Work :

- Simulink or SystemC exported on ADMS → 6 to 7x faster (Simulink to ADMS)
- Mixed Simulink/SystemC and SPICE on ADMS → 2x slower (ADMS)
- SPICE circuit simulation with MODSST algorithms → 34x faster than transient (Eldo RF)

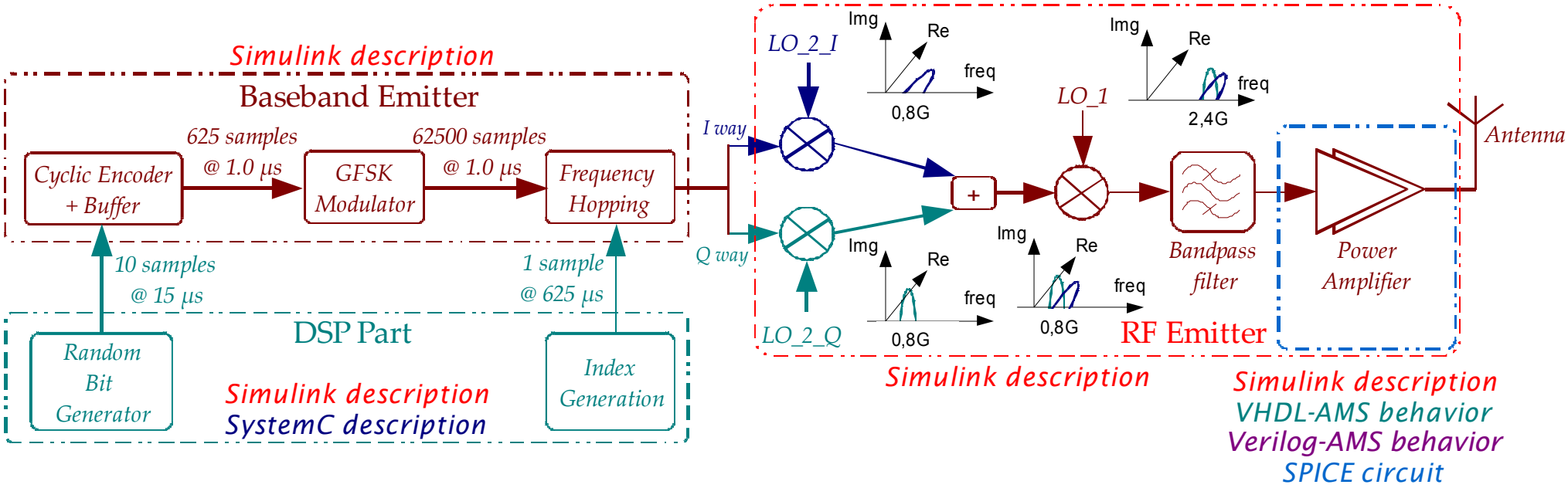
Next steps : - Combines RF instructions for SPICE and abstraction (SystemC and Simulink) acceleration to reduce simulation time !
- Validate this methodology with a ZigBee Transceiver Circuit

Thank you for your attention.
Any questions ?

Transceiver simulation results



Transceiver simulation results



Different descriptions but focused on key blocks :

- *DSP Part as Simulink or SystemC*
- *Baseband Part as Simulink*
- *RF Transmitter : Simulink + VHDL-AMS*
- *Power Amplifier : Simulink / Verilog-AMS / VHDL-AMS / SPICE circuit*