A Mixed-Mode behavioral model of a Controller-Area-Network bus transceiver: a case study

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ABSTRACT

This work presents a case study concerning a Controller-Area-Network (CAN) bus transceiver behavioral model. Three different model architectures have been developed in order to effectively tackle the speed-accuracy-convergence trade-off in CAN bus transceivers networks simulations. The model was implemented using the VHDL-AMS language. The model behavior has been fully validated. Extensive simulation results are reported: they demonstrate the effectiveness of the proposed model.

1. INTRODUCTION

Mixed-mode behavioral models allow the optimization of computational and human resources in the reliability and efficiency verification of complex electrical systems. Moreover, the nature of such models matches the intellectual property and reuse needs [1, 2, 3]. A great benefit is the possibility of designing full-featured models to be used by the end user (i.e OEM customers).

Mixed-mode models can be used in a variety of situations that can not be foreseen a priori. They have to be built in a structured way for flexibility reasons. Robustness and accuracy must be combined and many convergence issues must be faced. Digital circuits modeling has been successfully used for a long time; however, the use of analog models counterparts is still lagging behind. Indeed, much more still has to be done to achieve high level mixed-mode models integration [4].

In order to benefit of the behavioral modeling capabilities in Controller-Area-Network bus systems applications, a mixed-mode model of a CAN bus transceiver was developed. The previously cited issues were taken into account and addressed in the modeling case study that is presented in this work: the CAN transceiver AMIS-42668 [5] device behavior was modeled. The developed model allows the signal integrity and electrical behavior simulation of full CAN bus systems, even considering their intrinsic complexity due to the diversity of operating modes. Normal and faulty conditions are properly modeled. Accuracy, simulation speed and convergence issues are faced using different modeling approaches and abstraction levels [2, 3]. Indeed, three different model architectures were set to deal with such issues. All I/O transceivers signals are modeled in the analog domain, allowing an easy integration with transistor level circuit simulators. The model was implemented using the VHDL-AMS language.

Extensive simulation results are reported and they demonstrate the efficiency of the proposed model. Normal and fault operating conditions are illustrated by three detailed test case examples. Moreover, seven test cases are reported in order to illustrate the CPU computational effort when using the three model architectures.

This work is structured as follows: Section 2 presents the CAN bus transceiver device chosen as basis for the model development. Section 3 shows the mixed-mode behavioral model features. The methodology used to develop the model and the description of three proposed model architectures are also presented in this section. Section 4 presents the simulation results. Three test cases are shown in detail and the overall model performance is discussed as well. Section 5 reports the conclusions and future work.

2. THE CONTROLLER AREA NETWORK COMMUNICATION PROTOCOL

The Controller-Area-Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a very high level data integrity. Its domain of application ranges from high speed networks to low cost multiplex wiring. In automotive electronics, engine control units, sensors, anti-skid-systems, etc. are connected using CAN networks with bitrates up to 1.0 Mbps [6].

2.1 CAN bus general electrical characteristics

CAN standard [7] defines a differential voltage to represent recessive and dominant states (or bits) on a wired transmission bus. In the recessive state, the differential voltage is lower than a minimum threshold. On the other hand, in the dominant state the differential is greater than a maximum threshold. A dominant bit overdrives a recessive one on the bus to achieve nondestructive bitwise arbitration. In combination, dominant/recessive logic and the ability to compare the transmitted and the received bit guarantees that messages from competing transmitters will not collide during a transmission [8].

Reference [7] also specifies a number of electrical requirements intended to ensure the transceiver can survive harsh electrical conditions in order to guarantee an acceptable robustness on data transmission. For example, the transceivers must survive short circuits on the CAN bus inputs from 3V to +32V and transient voltages from -150V to +100V.

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2.2 The AMIS-42668 CAN bus transceiver

An example of available off-the-shelf transceiver fully compatible with CAN standard [7] is the AMIS-42668 [5]. It acts as interface between the CAN protocol controller device and the physical bus and may be used in both 12V and 24V supplied systems. It is primarily intended for high-speed applications and can achieve the maximum speed specified by [7] (i.e up to 1.0 Mbps). The device provides differential transmit capability to the bus and differential receive capability to the CAN controller. A block digram of the AMIS-42668 transceiver is shown in Figure 1 [5].

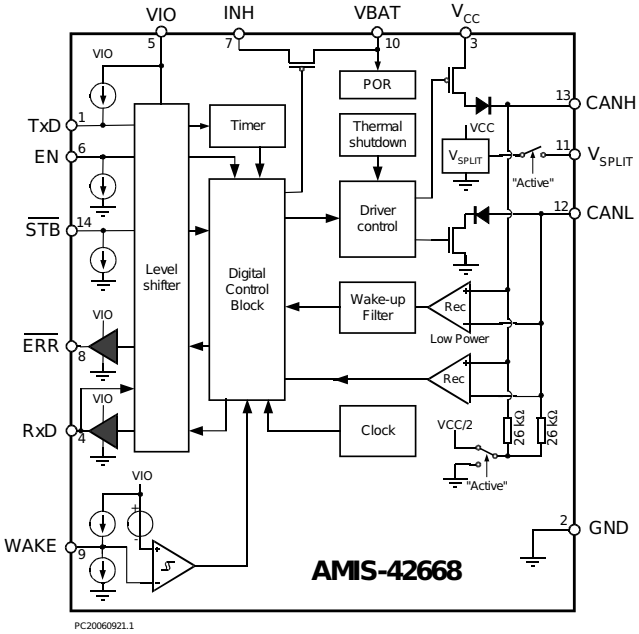

Figure 1: AMIS-42668 CAN transceiver block diagram

Some important features of the AMIS-42668 device are listed below for the reader convenience:

- Extremely low current standby mode with wake-up via the bus;
- Voltage source via VSPLIT pin for stabilizing the recessive bus level (EMC improvement);
- Thermal protection;
- Bus pins protected against transients in an automotive environment;
- Power down mode in which the transmitter is disabled;
- Bus and VSPLIT pins short circuit proof to supply voltage and ground;
- Logic level inputs compatible with 3.3V devices;
- No disturbance of the bus lines with un-powered transceiver nodes;
- Output voltages slope control to minimize EME.

The next sections will present the structure and the methodology used for the AMIS-42668 transceiver mixed-mode behavioral model development.

3. THE CAN BUS TRANSCEIVER MIXED-MODE BEHAVIORAL MODEL

CAN networks can be composed of a high number of transceivers (e.g. up to 40 nodes for the AMIS-42668), connected together, sharing the same bus line. Considering the entire system, a huge number of possible situations may occur. It is important to monitor the state of each single transceiver and the entire system performance as well. Undesired situations as, for example, bus line short-circuits, power supplies faults and transceivers over-temperature must be correctly modeled and detected when necessary. In such a complex scenario, precise modeling of the transceiver behavior is very important for signal integrity investigation issues. Moreover, the behavioral model simulation speed has a direct impact on the entire CAN system analysis computational effort. Therefore, the use of a dedicated behavioral model is almost mandatory in the system design and validation stage [4].

The block diagram of the CAN bus transceiver mixed-mode behavioral model is shown in Figure 2. The analog module converts the I/O signals, represented in the analog domain, to standard logic signals for the digital module. Digital output signals are also converted to analog. It means that all the I/O signals are represented in the analog domain. This feature allows the model to be mixed with transistor level models within electrical simulation tools that support both kinds of modeling approaches.

The analog module is also able to model the instantaneous power consumption based on the actual device operating mode. This feature permits the temperature behavior modeling and an accurate total power consumption estimation. The internal operating temperature is computed by the thermal module indicated in Figure 2.

The configuration package allows the user to easily set the transceiver model parameters. It also allows the analysis of the entire CAN system behavior at corner values of the device specifications.

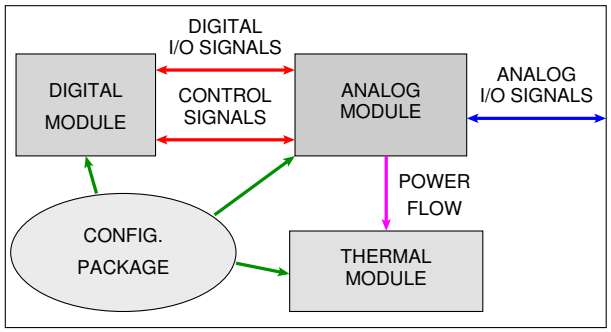

Figure 2: CAN transceiver Mixed-Mode behavioral model block diagram

The transceiver model implements all the real device functionalities (some of them are listed in Section 2.2) [5]. Besides, some particular analog domain related aspects are covered and discussed in this work due to the impact they have on the electrical characteristics of input and output signals (see Section 4).

The analog module comprises many internal blocks. Roughly, each block models the behavior of the ones shown in Figure 1. Examples of implemented internal structures are:

- 1bit D2A and A2D interfaces;
- Power supply voltage monitors;
- High-speed and low-power receivers;
- CAN bus transmitter drivers;
- Internal voltage references.

and, among others, the following characteristics were implemented as consequence:

- CAN bus bitwise arbitration;
- Output voltages slope control to minimize EME;
- Bus short-circuit conditions modeling;
- Maximum output current limiter;
- Voltage references reflect power-supplies states;
- Instantaneous power consumption estimation based on the operation mode;
- Temperature behavioral modeling and thermal shutdown based on the instantaneous power consumption estimation.

3.1 The behavioral model development methodology

The complex scenario where the transceiver model has to work claims for a special attention to the most important aspects of mixed-mode behavioral modeling. An accurate model is very important for signal integrity investigation. Simulation speed-up is a mandatory feature for behavioral models. At last but not least, the simulated system complexity needs an especial attention on convergence issues. It doesn't matter how fast and accurate the model is if it is not able to converge in all operating conditions [4]. These three concepts must be managed, and unfortunately their requirements go to different directions.

The methodology used in this work to face the mixed-mode behavioral modeling requirements consists of mixing different modeling abstractions levels and mathematical approximations in order to model each single block behavior within the transceiver structure (see Section 2.2). Piecewise linear, exponential functions and Taylor series approximations were used giving different performances in terms of accuracy, speed and convergence were noticed. Moreover, some transceiver functions were described using high level statements while others making use of hierarchical descriptions, using a low level abstraction modeling approach. As a consequence, a sort of basic building blocks set was obtained. A more detailed discussion about the development of the building blocks and the overall development methodology can be found in [4]. The methodology modularity property was exploited according to the Table 1.

The Table 1 shows that three different architectures were configured. Different approximations and features were arranged in each architecture: the user can arbitrarily choose one of them according to the accuracy level and simulations speed required for a given analysis. Nonetheless, a minimum set of features is present in all architectures allowing a meaningful signal integrity and/or devices behavior analyses for any combination of the model architectures inserted in a CAN bus system simulation.

4. RESULTS

The transceiver model was implemented using the VHDL-AMS hardware description language. The used CAD environment is included in *Cadence* mixed signal framework (IUS v5.7). The model fully matches the VHDL-AMS standard and it is completely portable to any other simulator that supports the language. The PC workstation used to performed the tests that will be described in this section is a Intel P4, 2.66GHz, 512MB RAM and Linux O.S.

4.1 CAN network set up

In order to validate the transceiver model, a simple network composed of two transceivers, TrA and TrB, was used as indicated in Figure 3. The resistors and the capacitor were included as indicated by the CAN standard [7]. This configuration allows the verification of each single device behavior, taking into account the operating modes (e.g wake-up, stand-by, normal mode, etc), the timing of I/O signals and the bus transceivers output impedances.

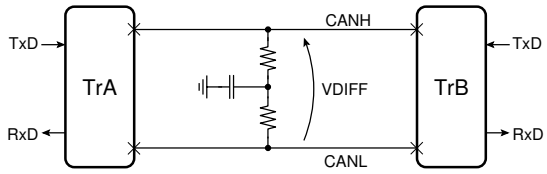

Figure 3: Network setup structure used for the transient analysis

4.2 CAN bus signal integrity analysis

The electrical signal characteristics on CAN bus is probably the most important aspect that the model has to properly represent. It allows signal integrity analyses and it is the basis of the CAN network performance validation. A reliable representation of signals present on the bus line permits the optimization of the entire system considering many variables as, for instance: different operating temperatures for each transceiver, different input impedances in the case of hybrid networks, the devices parameters variation within the specified range, etc.

Figure 4 shows the CANH and CANL signals in a simplified example of signal integrity verification where a recessive-to-dominant and dominant-to-recessive write operations are depicted. The ACCURATE model architecture (see Table 1) was used.

A first signal characteristic that can be seen is the transmission delay from a TxD events to the effective CANH(L) signals change and the delay from a bus line event detection to the RxD change. In general, the signal timing characteristics are strongly influenced by internal delays of the transceivers connected to the bus lines. Setting the related transceiver model parameters to the worst case conditions is useful in order to validate CAN systems operating at high bitrates. Besides, the signal timing analysis is essential for the bitwise arbitration foreseen in the CAN protocol handshake.

Table 1: CAN transceivers model architectures characteristics

	FAST	MODERATE	ACCURATE
Output drivers	Piecewise linear	Taylor series	Transconductor
EME control	NO	NO	YES
Internal Voltage Reference	Piecewise linear	Exponential	Exponential
Power Consumption Estimation	NO	YES	YES
Thermal Shutdown	NO	YES	YES

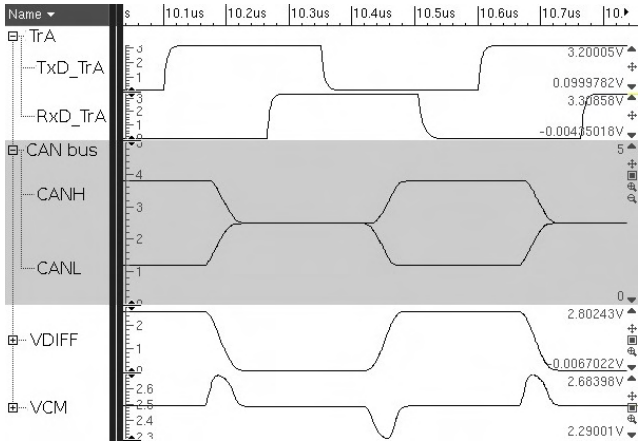

Figure 4: CANH and CANL signal integrity analysis using the ACCURATE model architecture

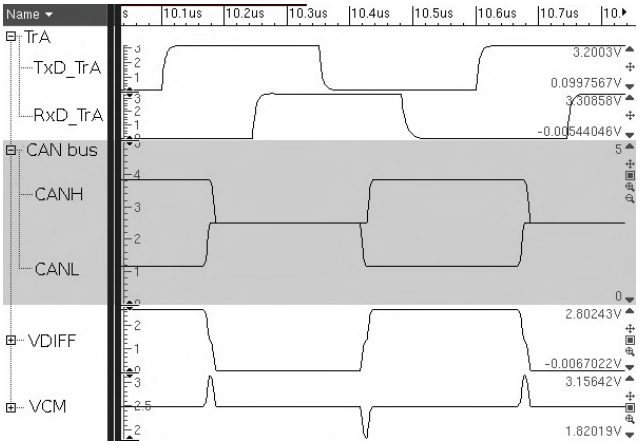

Figure 5: CANH and CANL signal integrity analysis using the FAST model architecture

An important feature of the transceiver device is the voltage slope control of CANH(L) signals. The maximum voltage variation slope of these signals is limited in order to minimize EME effects: the simulations have demonstrated that the model can properly represent the real device operation as can be seen in Figure 4.

At the bottom of the figure, the differential and the common-mode voltages, VDIFF and VCM respectively, are shown. The VCM peaks come from different transmission delays values of TxD-to-CANH and TxD-to-CANL. The possibility of representing such a situations is worth to the electromagnetic performances evaluation.

In order to illustrate the differences between two model architectures (see Table 1), Figure 5 shows the same analysis shown above using the FAST architecture. Please note the differences on CANH(L) signal transitions considering both cases. The VCM voltage peaks increases as well. Considering the accuracy loss, it is clear that this architecture is not indicated to precise signal integrity verification. Its utilization is advised to speed-up CAN networks validation with a high number of devices after a previous detailed signal characteristics study using the MODERATE or the ACCURATE architectures.

4.3 States Hopping

A simulation that illustrates the interactions between the digital and the analog modules of the mixed-mode model is show in Figure 6. The analysis shows a state hopping analysis (power-on, normal, stand-by and sleep) setting EN and STB signals properly. After a first power-on period, TrA is sent to normal state and accesses the CAN bus. Then, the STB and EN signals are set to 0.0V to send TrA to the stand-by state. When entering this state, TrA greatly reduces the bias currents, as it can be seen on signal PWR_TrA that models the instantaneous total power consumption. While TrA is set to the stand-by mode, TrB accesses the bus. TrA, that is monitoring the bus lines by means of its low-power receiver block, understands that a remote wakeup was requested (WAKEUP digital flag). RxD is set to 0.0V in this case. In such state, if STB is set to 3.3V, TrA wakes, as indicated in the Figure 6. Finally, TrA is set to the sleep mode, when EN=0.0V and STB=3.3V.

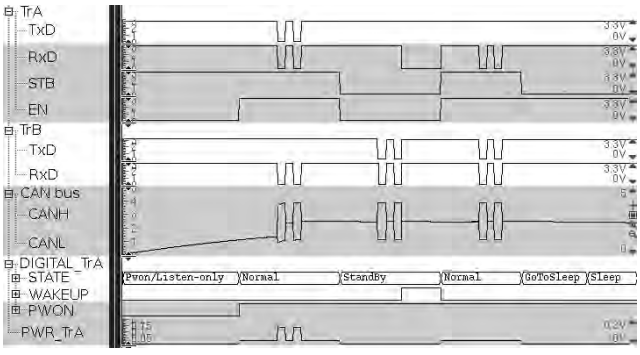

Figure 6: Internal states hopping and remote wake-up analysis

It is worth to note that the signals TxD, RxD, EN and STB are analog signals. Even if they represent digital data that the CAN controller sends/receives to/from a given transceiver, they are set within the range 0.0V∼3.3V as analog signals instead of '0' and '1'.

The signal PWR_TrA depicted in the Figure 6 represents the device instantaneous power consumption. It is used to model the thermal behavior of the transceiver, allowing the implementation of the power-shutdown feature, and it can be used to monitor the power consumption of the entire CAN network system: a very important feature for battery powered systems.

4.4 Short Circuit analysis

An interesting case where the signal integrity analysis is simplified using the proposed model is the study of short-circuits effects in CAN buses.

The Figure 7 shows an example where shorts are arbitrarily applied to both nodes CANH and CANL. In the first case (area A in Figure 7), a short-circuit from the CANL node to ground is applied. Concurrently, the TrA transceiver tries to write dominant states on the bus at a 1.0 Mbps bitrate. Nevertheless, it is not possible and the correct data transmission will be possible only at lower bitrates (200.0 kbps in this case), as it can be seen in the area B.

In the same Figure 7, another short-circuit situation is shown in the area C. A short between CANH and CANL is applied and TrA still tries to write on bus. On a differential bus, a short-circuit between nodes is catastrophic. Indeed, in the example depicted, no data transfer is possible during this short-circuit situation.

Another short-circuit condition applied is between CANL and the battery power supply VBAT (area D in Figure 7). In this case, the data transmission is not possible, following the transceiver device specifications. A important feature that can be highlighted in this situation is the thermal behavior model. If the short-circuit persists for a long time, the operating temperature increases as it can be seen in the Temp variable curve. When it reaches a given temperature threshold (in this example 100°C), the thermal shut-down flag (OverT) is activated and the transceiver goes by itself to a permanent recessive state. The result is that after some time the temperature drops down and, in the real device operation, a permanent damage due to over-temperature can be avoided. The transceiver model warns the user if such an undesired situation occurs.

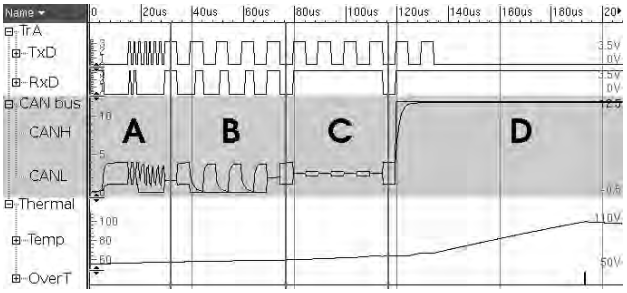

Figure 7: CAN bus short-circuit analysis

4.5 Behavioral model performance

Besides the detailed examples previously introduced, many other validation tests were done. The three available model architectures presented in Table 1 were used. Table 2 gives a brief description of the main performed tests. Test 3, Test 4 and Test 5 are the ones presented in Sections 4.2, 4.3 and 4.4 respectively. Note that for Test 3 (Section 4.2) only a small part of the transient analysis is show in Figures 4 and 5 for convenience. The other test cases are of primary importance for the complete model validation. They are useful to verify the analog interface behavior and the information transfer between analog and digital modules as well.

The third column of Table 2 reports the simulation period set for the transient analyses. Table 3 shows the the CPU usage time in seconds to execute each test. The results show that the proposed approach can be used to manage the speed and accuracy trade-off. One must just realize which of the available features and accuracy levels match the analysis needs to be performed.

Table 2: Test cases description

Test #	Description	Simulation Period
Test 1	TxD dominant clamp timeout	1.1 ms
Test 2	VIO undervoltage timeout	12.3 ms
Test 3	Loop delay TxD-CANBus-RxD	14.0 μs
Test 4	Hoping states	133.1 μs
Test 5	Short-circuits	210.1 μs
Test 6	Local and remote wake-up	670.1 μs
Test 7	Power-On detection	10.5 ms

Table 3: CPU usage time

	FAST	MODERATE	ACCURATE
Test 1	46.9 s	49.7 s	59.3 s
Test 2	392.4 s	450.0 s	534.7 s
Test 3	15.2 s	24.2 s	31.3 s
Test 4	18.8 s	28.3 s	35.0 s
Test 5	30.4 s	52.4 s	90.5 s
Test 6	31.8 s	38.0 s	46.5 s
Test 7	339.1 s	390.0 s	461.0 s

The results shown in Table 2 indicate from -42% to $+73\%$ CPU usage time variation, taking the MODERATE architecture as reference. This factor strongly depends on the given test case characteristics. Test cases where a high number of write operations occurs (Test 2 and Test 5) show the most significant differences. It is worth to note that for real operating conditions, where many devices are supposed to be active at the same time, a huge number of state changes – that means write operations – are expected. Therefore, following the previous results a overall factor of $\pm 30\%$ to $\pm 40\%$ variation on CPU usage time is presumed which can imply many CPU usage hours for a complete system validation!

The benefits are still more evident if one considers the computational effort using SPICE-level simulations. For example, the Test 2 – using just one transceiver – can take about 40 minutes using such a low abstraction level approach.

As a final remark, the robustness related to DC and transient analysis is demonstrated by the amount of test cases taken into account.

5. CONCLUSIONS AND FUTURE WORK

A case study of a Controller Area Network bus transceiver mixed-mode behavioral model has been presented. High and low abstraction level basic blocks models have been mixed together to configure three different transceiver model architectures. As a consequence, the end user may arbitrarily

choose among them according to the application requirements which may differ by speed, accuracy and convergence constraints. Besides, the model structure allows the use of corner parameters analysis methodology. The model was implemented using the VHDL-AMS language.

The model behavior matches all the device datasheet operating description and functionalities. The model was applied in various test cases and the results demonstrate both accuracy and simulation speed efficiency. Moreover, the model behavior was validated comparing the simulation results to the experimental measurements. Nonetheless, the study of a formal model validation method to quantify the model accuracy is still being carried on. Such study will permit a model behavior fine tuning as well.

The mixed-mode modeling structure and the accuracy and simulation performance make the model presented in this work fully compatible with more complex CAN bus systems analysis tools. An example where the model would match all needed requirements is presented in [9].

Further work will also address a more detailed analysis to verify the simulation effort versus the number of transceivers in a CAN bus system. The difficulty of establishing such relationship is that it depends on the operating states and activity level of each transceiver. In a big network a very high number of combinations is possible taking into account the transceivers operating modes diversity. Therefore, setting a significant test case simulation that represents a real situation is a quite complex task. Nonetheless, this analysis is currently being performed in cooperation with automotive systems developers who intend to make use of the transceiver model presented in this work.

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