Efficient Modeling of Single Event Transients Directly in Compact Device Models

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ABSTRACT

With decreasing feature size, analysis of circuits for radiation strike vulnerability is becoming very important in a many applications. Classical modeling methods may be not sufficient to reproduce single event transients observed in deep-submicron, fast ICs. A novel approach for development and efficient inclusion of such effects directly in compact device models is described.

1. INTRODUCTION

AS IC device sizes continue to shrink the impact of ionizing radiation has an ever greater impact upon device performance and reliability. Traditionally only a concern for space-bound electronics, such cosmic radiation is becoming a concern even in terrestrial applications. As the active devices in modern IC processes become diminishingly small the minimal amount of background radiation present on earth affects "bleeding edge" digital and analog circuitry negatively.

There are several broad classifications for radiation effects. These include total ionizing dose, dose rate, and single event effects. Dose-based effects typically manifest themselves as leakage or transistor threshold shift effects, occurring after many hours in a harmful radiation environment; systems may or may not recover without adequate compensation. The study and mitigation of dose-related behaviors is typically left to space-borne systems, although it is still a concern outside that realm as many commercial processes are used for such applications [1]. Single event effects (SEEs), on the other hand, are transitory effects that tend to inject momentary errors into a system. The result of heavy ions passing through a chip, these effects inject very short (nanosecond) current pulses into active devices. These resulting Single Event Transients (SETs) can manifest themselves as errors injected into digital and analog ICs [2, 3].

To adequately understand the effect of radiation on circuit and chip operation, models and simulators must be be available in several different domains. The workhorse of IC design and verification is circuit-level simulation (SPICE). In the device and process development realm, however, two-dimensional (2-D) or three-dimensional (3-D) device-level simulation or Technology CAD (TCAD) is typically used. TCAD is used to provide excellent insight into detailed device operation. However, SPICE simulation is orders of magnitude faster due to the great many assumptions the circuit-level models, aptly named *compact models,* utilize.

A newer analysis approach involves a mixture of TCAD and SPICE level simulation. In so-called *mixed-mode* or *mixed-level* simulators [2], certain user-chosen compact devices in a circuit description may be replaced with TCAD-modeled devices. The TCAD model is then wrapped with a set of boundary conditions and spun into one overall system matrix to be solved using the classic SPICE approach [3]. This is significantly faster than full TCAD-level simulation, but has a drawback; typically only a few TCAD-level devices may realistically be used. Thus, the designer must carefully choose the devices to be simulated at the TCAD level. For a large system, thousands of devices may be involved. Therefore, the designer must have some expertise in single event upset vulnerability to know which devices to investigate.

What is desired is a method to migrate radiation expertise to circuit-level simulation with minimal impact to existing IC design flows. The outlined methodology provides such an instrument by utilizing model compilation technology with a unique tool for analog compact modeling.

2. SINGLE EVENT TRANSIENT EFFECTS

2.1 Transient Upsets: Modeling and Analysis

Many approaches to modeling transient current pulses have been developed over the years [2-5]. A popular approach is to inject a double-exponential current pulse at the hit node, with the time constants and amplitude tailored to achieve a total integrated charge [6]. In an attempt to improve single-event current accuracy, the transient waveforms are sometimes first computed using a stand-alone 3-D or 2-D device model. Those currents are

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then applied at the circuit level using a SPICE-type circuit analysis program where the resulting circuit response is evaluated. Although such decoupled simulations were used successfully earlier for analysis of single event transients in analog circuits, they may give incorrect results in the case of digital SETs in fast deep-submicron CMOS ICs [7]. In the decoupled mixed-level approach, the 2-D or 3-D device physics simulations of an ion strike are done with the node of interest held at a constant bias (voltage boundary condition) during the transient computation. This approach is therefore valid only under the assumption that the circuit response is slow compared to the 100 to 200 ps time evolution of the current waveform. While this was certainly true for older technologies (0.8 µm and larger), it is no longer the case for deep submicron technologies and faster CMOS ICs. This is illustrated in Figure 1 for the TSMC 0.18-µm CMOS technology.

2.2 Effects in Deep Sub-Micron Technologies

Figure 1 was generated from a SPICE simulation using a decoupled mixed-level analysis. The circuit is an 8-stage inverter chain, presented in detail in [6, 7]. The curve of drain current, labeled "Id-3D-PWL", was generated by a separate 3-D device simulation with ion strike at a Linear Energy Transfer (LET) of 20 MeV-cm^2/mg in this case. This current waveform was then described with a piecewise linear (PWL) table. The resulting PWL current pulse was injected during the SPICE simulation into the V(2) node, which was the drain of an off-state NMOS transistor in the first stage of the inverter chain. Two problems are clearly evident. First, the voltage on node 2 immediately responds to the pulse, taking it negative. The negative behavior results from SPICE injecting current through the drain-substrate diode that becomes forward biased. The second inconsistency is that the PWL current does not decrease as the node voltage collapses. To summarize, the voltage on a struck node and the current collected by a struck node do not behave in a self-consistent manner in decoupled analyses for cases where the circuit responds faster than the current pulse width that is modeled by a current source independent of the circuit response. It is therefore necessary to do fully coupled mixed-mode simulations for fast, deep submicron technologies or model the SETs more accurately at the compact device level.

In the fully coupled mixed mode, the SPICE analysis and 3-D device physics modeling are performed simultaneously. In this way, the voltage boundary condition on the struck node dynamically changes with time as the circuit responds to the injected current. As the circuit collects the charge from the strike, the node voltage begins to decrease. This voltage decrease will result in a collapse of the electric fields and subsequently reduce the collection current. As this collection current decreases, a substantial pulse broadening should occur as it will now take a much longer time to clear the deposited charge from the substrate. This is assisted by other carrier removal processes, e.g., Shockley-Reid-Hall (SRH) recombination, which is included in the 3-D physical model of the hit device.

Figure 2 shows results for the same 8-stage inverter chain, again for an LET of 20 MeV-cm^2/mg. The current curve, now labeled "Id (NMOS1)" clearly shows the current decrease as the voltage of the struck node V(2) collapses in response to the initial injected current. Also, V(2) no longer goes negative, but rather remains slightly

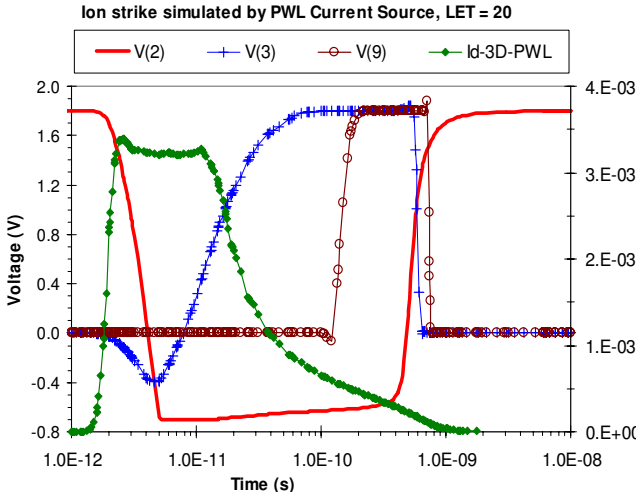

Figure 1. Decoupled simulation results for SET, at LET = 20 MeV-cm2/mg. Calculated V(9) pulse width: 0.59 ns.

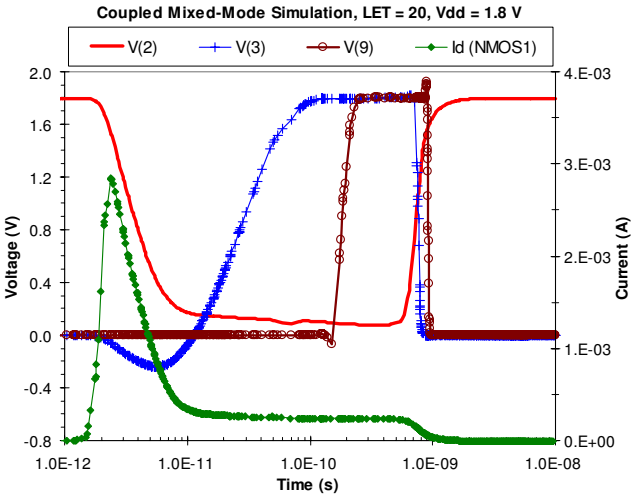

Figure 2. Fully coupled mixed mode results for SET, at LET = 20 MeV-cm2/mg. Calculated V(9) pulse width: 0.74 ns.

positive as the injected current is sunk by the pull-up PMOS of the inverter. The calculated pulse widths at the chain output node, V(9), are compared in the captions of Figs. 1 and 2, respectively. As another example, for LET = 30 MeV-cm^2/mg, the computed pulse widths were: 0.89 ns (decoupled simulation) versus 1.13 ns (coupled mixed mode), which makes over 30% difference.

3. COMPACT MODELING METHOD

3.1 Traditional Modeling Approaches

There are several common approaches to model implementation of single event effects (SEEs) in circuit-level simulators. One approach is to use macromodeling. Using available SPICE primitives, a current source is designed to describe a single event pulse. In more modern simulators, primitives may be implemented directly using a language interface, such as Verilog-A. Unfortunately, this typically incurs a significant penalty in simulation speed. In either case, the SET macromodel is implemented in a somewhat convenient manner as a SPICE subcircuit, wrapping the transistor to be struck with an external SEE model. Several models may be included in one wrapper and parameterized such that the designer may choose which node of the device to strike and with what specific energy.

Both of these approaches have inherent problems. From the point of view of an IC design flow, insertion of such macromodels can be disruptive. Netlists and schematics once considered "golden" or proven must be modified with the new subcircuits. Another negative aspect of this approach is that insertion of the SEE is limited to netlist-level nodes only. Internal nodes of the transistor/device models in the schematic are not available. This may lead to having to zero-out (and re-model externally) certain aspects of the device model or design kit, such as intrinsic resistances or parasitic active devices.

The ideal implementation of many effects is actually inside the device model of interest. However, such models are typically implemented as C-code inside the simulator of choice. This code is non-trivial to edit, if even obtainable, and may be tens of thousands of lines of extremely intricate, simulator-specific, code. More recently, device models are being developed in higher-level hardware description languages (HDLs), such as Verilog-A, and delivered directly to simulators as compiled C-code using model compilation techniques [9]. In fact, the Compact Model Council has recently made Verilog-A the standard format for all new models they accept [10]. This is quite an improvement (Verilog-A may be 2 to 4x smaller than equivalent C-code) but still requires intimate knowledge of Verilog-A programming.

3.2 Efficient Compact Model Augmentation

A new solution to this problem has been developed by Lynguent. The ModLyng software (Figure 3) is a unique integrated development environment (IDE) for analog/mixed-signal modeling. ModLyng allows the user to either start new models from scratch using a library of

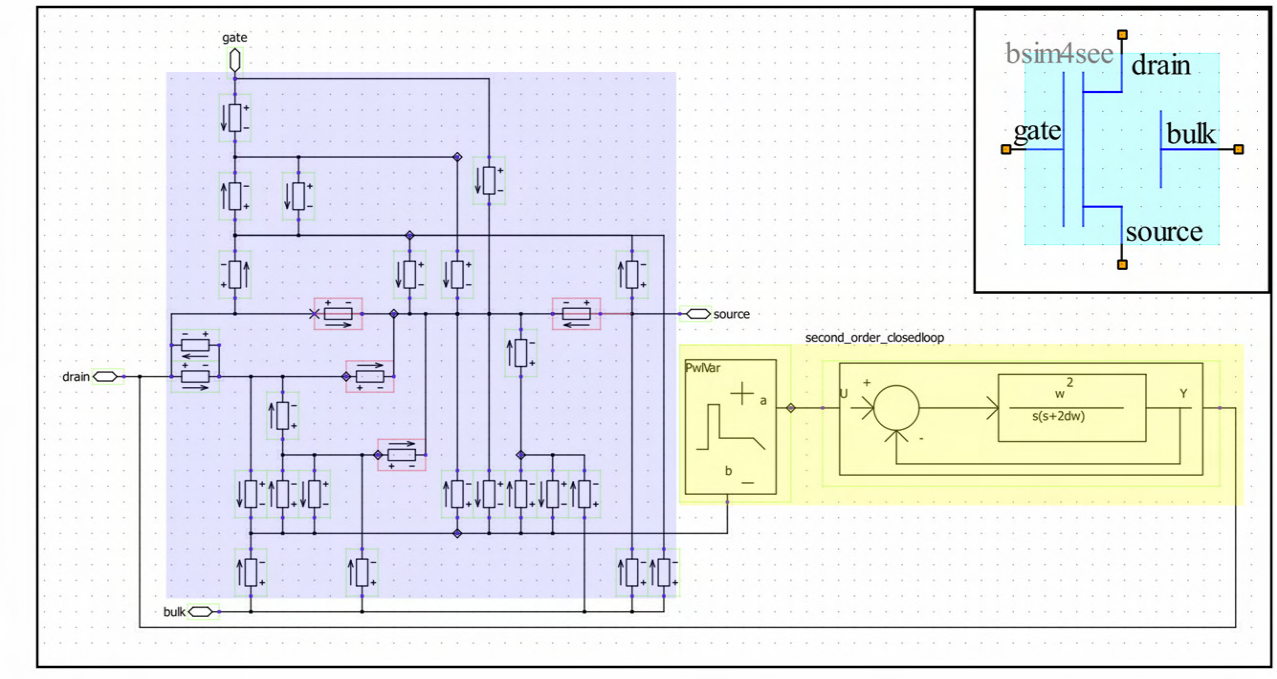

Figure 3. ModLyng with BSIM4 model (SEE effect added).

available effects, or to start from an existing HDL model (Verilog-A/MS, VHDL-AMS, etc). Imported models are mapped to an intermediate format, common model exchange (CMX), which is a superset of the supported languages [9]. This allows models to be migrated between languages and supports integration of models into new simulation tools.

As a case study, the industry standard BSIM4 model has been imported into the ModLyng software as shown in Figure 3. ModLyng separates the model into interface, topology, expression, and symbol data; an editor for each provides an appropriate view. Expressions are displayed in the language of mathematics, not the semantics of an HDL. For this case study, a very simple SEE drain strike model has been implemented directly in BSIM4's large-signal topology using a piecewise-linear source and second-order linear filter to smooth the result. Using this method, an arbitrary result measured from TCAD or physical measurements may be applied by modifying the piecewise source and choosing appropriate filter coefficients. Note that the modeler now has access to internal variables and (physically relevant) nodes of the device model in question. This opportunity has been utilized here to implement the strike model directly between the drain node and an internal bulk node of the device.

With the effect added, a modified BSIM4 model is exported and automatically compiled through the Spectre simulator's compiled model interface (CMI). ModLyng supports exporting both non-optimized Verilog-AMS models for model debug, as well as compact, optimized models via a direct ADMS model compiler output option [11]. Using the later method, augmented models may run as fast or faster than hand-coded models. Results for a drain strike to the "off" NMOS transistor of a standard CMOS inverter configuration are included in Figure 4. The results clearly indicate that by implementing even this simple, linear voltage-invariant strike model directly in the bulk-network model of BSIM4, the desired substrate "tail" effect of Figure 2 becomes prominent. Note that this method may be utilized to easily refine the strike model. The accessibility and understandability provided by the ModLyng interface makes adding ever more advanced effects very possible, such as adding current pulse dependence on terminal or node voltage, or adding charge-based upset models directly in BSIM4's charge model.

4. CONCLUSION

As CMOS technologies continue to shrink, variation in the shape and duration of SEE current pulses arises. Macromodeled independent current sources, especially the classical double-exponential waveforms, are no longer up to the task. In fact, modeling at the circuit/netlist level generally does not provide the fidelity required. The correct place for these effects is *within the compact device models*. The described approach and tools facilitate rapid integration of arbitrary single event effects directly in industry standard semiconductor device models. Further, we propose that model compilation technology allows deployment of these models with minimal impact to design kits and flows; a new model may be deployed directly in the simulator of choice! Clearly this is a method which has the potential to allow researchers and designers to deploy timely single event phenomenon into state of the art IC design flows with minimal disruption.

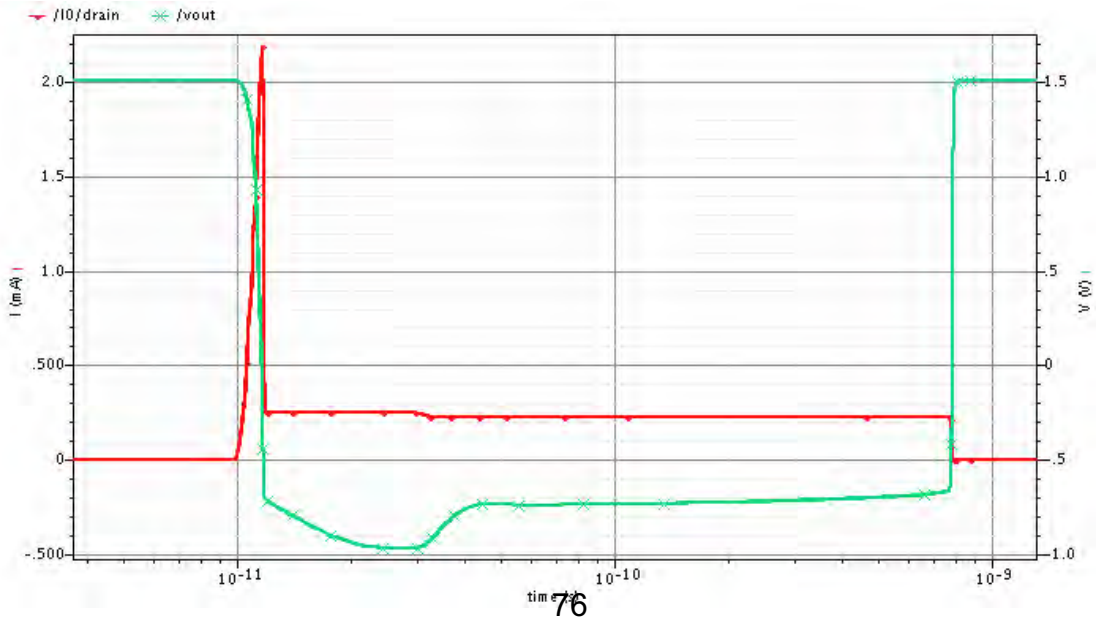

Figure 4. Upset in the output (V_{out}) of CMOS inverter, NMOS drain strike, as observed utilizing augmented BSIM4 model. I_{drain} is the current at the external NMOS drain node.

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