Behavioral Modeling of a Charge Pump Voltage Converter for SoC Functional Verification Purposes

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ABSTRACT

To enable full chip functional verification, critical system building blocks need to be abstracted and simplified using behavioral models. Charge pump voltage converters are highly active circuits and act as bottle necks when integrated in SoC verification simulations. In this paper, a charge pump circuit designed by STMicroelectronics will be modeled using VHDL-AMS. Using this model, the whole SoC can be simulated by ADVance MS^{TM}.

1. INTRODUCTION

The growing competition among chip makers has made first time silicon success a key requirement. To achieve this, SoC designers are always in search for means to minimize risks and to verify their systems at less critical stages within their design cycle. Combining the complexity of digital verification with the increasing integration of more sophisticated analog circuits, the problem is getting exponentially worse. It is no longer wise to divide a design into analog and digital parts and make seperate simulations for each. This is why mixed-signal simulation has become the solution adopted by many design houses to improve their verification methodologies. The complete system is simulated to verify the system functionality with respect to the target system specifications.

To succeed in simulating large and complex systems, some blocks need to be simplified using mixed-signal HDLs. An example of a typical sub-system that needs modeling is the charge pump voltage converter circuit [6]. This circuit is used in many applications that require multiple derived supply voltages, such as LCD drivers [5] and many other portable applications. Its popularity stems from it's low cost, small size and inductorless and fairly simple design [7]. Complex systems such as LCD drivers are almost impossible to simulate at the system level due to their large size and complex functionality. The charge pump is one of the most active blocks in such systems, as it is continuosly alternating between different states throughout the simulation. To make full chip verification feasible, this highly active block must be simplified and abstracted.

To show the impact of this block on simulation time, we will use a real design of a charge pump voltage converter, designed by STMicroelectronics [4]. A corresponding simple behavioral model will be described using VHDL-AMS, and both transistor level circuit and behavioral model will be simulated under the same stimulus and loads using Mentor Graphics mixed-signal simulator, ADVance MS^{TM} [2]. Results will be compared in terms of accuracy and speed. The gain in speed achieved by modeling this block will definitely contribute to enhancing the simulation speed of any application in which this block will be later integrated.

This paper is organized as follows. Section 2 will explain what is meant by functional verification and how it can be achieved using mixed-signal simulation. In this section we will also propose the guidelines for choosing the parts of the system that need to be modeled. In section 3 we will describe the charge pump voltage converter circuit which will be modeled. Next, in section 4, the corresponding VHDL-AMS model will be illustrated. A speed and accuracy comparison will be given in section 5, followed by the conclusion.

2. SYSTEM FUNCTIONAL VERIFICATION

Functional verification attempts to answer the question "Does this proposed design fullfill the intended functionality?". This is a complex and challenging task and consumes the majority of the design and verification process.

SoC's are mostly digital and digital designers have a well defined design and verification flow. Analog designers, on the other hand, rely largely on experience and reuse. Traditionally, both teams were nearly completely isolated, where the digital team followed a mature and automated digital design and verification flow and the analog team used analog spice-like simulations at the transistor level. To avoid fatal integration errors, the complete system must be integrated and verified before tape out.

One important verification aspect is the functionality. In such complex and diverse systems, errors can occur not only in the design of the building blocks, but mostly at block interfaces. This is why it is mandatory to simulate the complete system. The overall system functionality must be verified in addition to the interaction between analog and digital blocks.

At this verification phase, accuracy can be relaxed as a compromise for speed. This is the price to pay to succeed in simulating a large system in a reasonable time.

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Using a fast-spice simulator may be the answer in some cases, but for highly complex systems with very high activity and tightly coupled functionality, this solution may still not be fast enough.

The solution would be to move from a large and complicated analog circuit simulation, that results in a huge simulator matrix and a high probability of running into convergence issues and memory capacity problems, to a more mixed-signal simulation.

A mature mixed-signal simulator is required to cope with these challenging verification demands. The ADVance MS mixed-signal simulator, by Mentor Graphics, offers comprehensive technologies that support multiple modeling languages: VHDL, Verilog, VHDL-AMS, Verilog-AMS, SystemC, SystemVerilog, and SPICE. Blocks that need to be modeled are developed in any of these languages and simulated with other blocks at the transistor level.

The selection of blocks to be modeled must be done wisely. Not everything needs to be modeled. Developing a correct and efficient behavioral model consumes time and resources that should only be invested for a good cause. No matter how accurate, a model is still a simplification and will never cover all regions of operation of the real circuit and will definitely lose some accuracy. Introduction of too many unnecessary models increases the risk of making mistakes and not gaining anything in return.

To determine what needs to be modeled we must locate the blocks that are loading the simulation and slowing it down. Good candidates are large blocks with high transistor count that can be replaced by a simple model that reflects the overall basic functionality. Higher order effects and non-idealities can be ignored at this stage, which is acceptable at this level of verification. Remember, we are not verifying the block itself, instead we are verifying the proper intergration and functionality of the system as a whole.

Another way to increase simulation speed is to minimize the number of converters that are inserted between ports of opposite natures. If the functionality of an analog block is mostly digital in nature or is interfacing with other digital blocks it is better to represent this block by a mixed-signal model that is mostly digital and includes minimal analog effects.

Another culprit is highly active circuits. Examples of those are circuits with high switching activity throughout the simulation. These circuits greatly reduce the simulation timestep and, as a result, cause considerable slow down. Modeling these circuits in a mixed-signal nature, will definitely render a simpler problem for the simulator to solve. The charge pump circuit is a typical example of such circuits which is why replacing it by a very simple model will lead to a considerable reduction in simulation time.

3. CHARGE PUMP CIRCUIT

The charge pump voltage converter, also known as switched-capacitor DC-DC converter, accomplishes energy transfer and voltage conversion using capacitors and semiconductor switches.

In this paper we will focus on a specific charge pump circuit design owned by STMicroelectronics. This circuit is able to generate voltages larger than the circuit supply.

The basic components of the charge pump voltage converter at hand are two pairs of MOS switches, as shown in Figure 1. The two MOS transistors in each pair are turned ON and OFF alternately by an input clock signal.

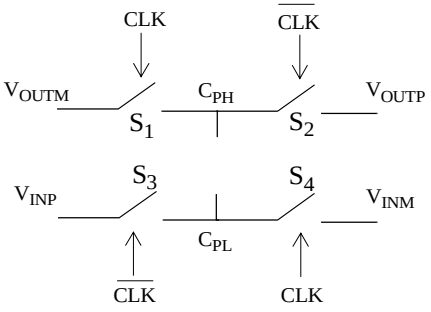

Figure. 1. Charge pump voltage converter basic circuit

The charge pump terminals are connected externally to three voltage supplies, namely V_1, V_2 and V_3, and two capacitors, C_1 and C_0, where C_1 is the pump capacitor and C_0 is the storage capacitor, as shown in Figure 2. The converter output is V_{OUTP}.

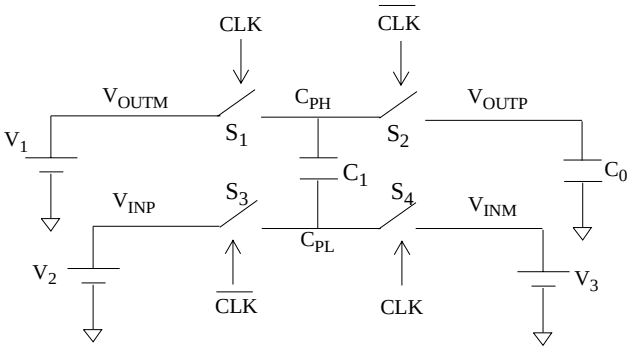

Figure. 2. Charge pump circuit with outer connections

The basic operation can be divided into two phases. In the first phase, when CLK is high, switches S_1 and S_4 are closed and S_2 and S_3 are open, and the pump capacitor is charged by the voltage (V_1-V_3). In the second phase, when CLK is low, switches S_2 and S_3 are closed and S_1 and S_4 are open, and the pump and storage capacitors share charge. The rate of charge and discharge of the capacitors is a function of the switches ON resistances, the capacitance values (C_1 and C_0) and the CLK frequency.

These two phases are repeated periodically until the output voltage at the terminal V_{OUTP} reaches a steady state. The

final steady state voltage reached by this circuit at no load is equal to (V_1+V_2-V_3).

An additional MOS transistor is connected in series between S_4 and V_{INM}. This transistor is normally conducting and acts as a closed switch, unless the voltage conveter is placed in closed loop to regulate the steady state output voltage. Once the output voltage exceeds the desired level, this switch is opened and the output voltage stops increasing. If the output drops below the required voltage level, the transistor is turned back on to allow the output to charge up again, and so on.

The complete circuit schematic is illustrated in the appendix†.

4. CHARGE PUMP MODEL

To model the charge pump circuit for system functional verification purposes, any unnecessary detail needs to be stripped off to have a faster and successful simulation.

The charge pump model needs to capture the two main phases of operation. The MOS transistors are modeled as simple switches and are connected together like the circuit.

The switch model is a simple resistance connected between two analog ports. The value of the resistor can take one of two values representing the switch open (OFF) and closed (ON) states, namely R_{OFF} and R_{ON}, where R_{OFF} is much larger than R_{ON}. The selection of the state is controlled by a digital input control signal. The VHDL-AMS code for the switch model is illustrated in Listing 1.

Listing 1. VHDL-AMS code for the switch model

```
entity switch is
  generic (
    Ron : resistance := 150.0); -- Switch ON resistance
  port (
    signal ctrl : in std_logic; -- Digital control signal
    terminal P1, P2 : electrical); -- Switch analog terminals
end entity;
-------------------------------------------------------------------------
architecture a1 of switch is
  constant Roff : real := 1.0e9;
  signal R : real := Roff;
  quantity VR across IR through P1 to P2;

begin

  R <= Ron when ctrl = '1' else Roff;
  VR == IR * R;

  break on R; -- needed to synchronize between digital and analog solvers

end architecture;
```

The charge pump model is a structural model instantiating five switch models. The two capacitors are connected to the model ports externally from the netlist using Eldo™ primitives [3]. The structural modeling technique is selected since it is more appealing for models with repetitive building blocks. Modifying this model to match any other charge pump configuration will be straight forward. Listing 2 illustrates the complete charge pump model.

Listing 2. VHDL-AMS code for the charge pump model

```
entity cell_pump_X4POS is

  generic (
    Ron_XM2 : resistance := 320.0;
    Ron_XM4 : resistance := 150.0;
    Ron_XM7 : resistance := 320.0;
    Ron_XM1 : resistance := 150.0;
    Ron_XM6 : resistance := 120.0);

  port (
    terminal VDDB, VSSB : electrical;
    signal CK, CNTR : in std_logic;
    terminal CPH, CPL, VINM, VINP, VOUTM, VOUTP : electrical);

end entity;
-------------------------------------------------------------------
architecture a1 of cell_pump_X4POS is

  terminal net0102: electrical;
  signal CKB : std_logic;

begin

  CKB <= not CK;

  XM2: entity switch(a1)
    generic map (
      Ron => Ron_XM2)
    port map (
      ctrl => CK,
      P1 => VOUTP,
      P2 => CPH);

  XM4: entity switch(a1)
    generic map (
      Ron => Ron_XM4)
    port map (
      ctrl => CKB,
      P1 => CPH,
      P2 => VOUTM);

  XM7: entity switch(a1)
    generic map (
      Ron => Ron_XM7)
    port map (
      ctrl => CK,
      P1 => VINP,
      P2 => CPL);
```

† Publication of the schematics authorized by Francesco Pulvirenti, Design Director of Display Division – STMicroelectronics (April 2007)

```
XM1: entity switch(a1)
 generic map (
  Ron => Ron_XM1)
 port map (
  ctrl => CKB,
  P1 => CPL,
  P2 => net0102);

XM6: entity switch(a1)
 generic map (
  Ron => Ron_XM6)
 port map (
  ctrl => CNTR,
  P1 => VINM,
  P2 => net0102);

end architecture;
```

5. SIMULATION RESULTS

Both the transistor level circuit and the behavioral model are simulated using ADVance MS^{TM}, under the same stimulus and loads and the results are compared. The test circuit is illustrated in Figure 3

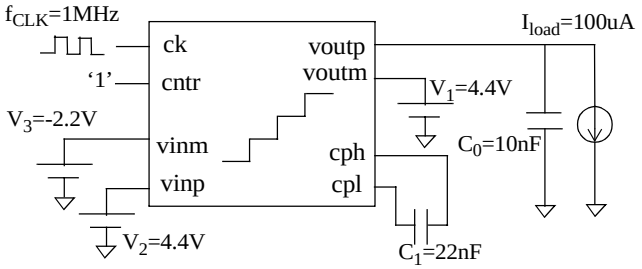

Figure. 3. Test circuit for the charge cump circuit and model

The test circuit was simulated for 5000 clock cycles (5ms). The transistor level simulation took around 3 hours of CPU time, whereas the behavioral model took 12 seconds, which is a speed gain of about 900 times. The design covered in this paper is a fairly simple one. Other more complex charge pump designs with more phases and a larger number of capacitors can simulate in many hours whereas the behavioral model will not increase largely in complexity and will still simulate almost as fast as this one.

The simulation results are illustrated in Figure 4. As seen in the results, the waveforms are not completely overlapping because of the abstraction done in controlling the switches by a digital signal and restricting the switch resistance to one of two distinct values throughout the simulation. The real MOS switch resistance is actually a function of the gate-to-source and drain-to-source voltages. Another level of abstraction is the neglection of the small time delays between the four different clock signals applied to the four switches, as a result of the inverter chains available in the real circuit before the gates of each MOS device. As explained before, such level of detail can safely be dismissed at this level of verification.

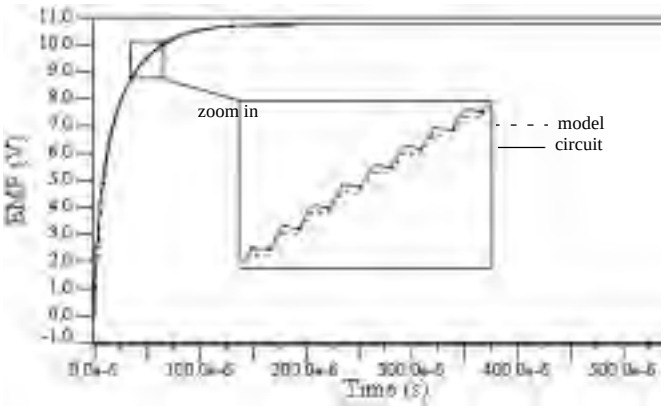

Figure. 4. Simulation results of the charge pump circuit verses behavioral model

The important effects to capture are the transient time needed to reach steady state and the steady state value. The average steady state voltage reached by the circuit is 10.749V and for the behavioral model is 10.788V, which represents an error of 0.36%. This error is very reasonable for a system level functional simulation.

Larger speed gains are possible by using the average behavioral modeling technique described in [1]. The resulting average model is not controlled by a clock signal, therefore the simulator time step is relaxed and the simuation time is greatly reduced. The drawback of using this technique is a larger loss in accuracy compared to the switching model.

6. CONCLUSION

Full chip functional verification is a challenge, but it is becoming mandatory to discover mistakes in the design in earlier, less costly design phases. To integrate and simulate a complete system, some blocks need to be modeled using a mixed-signal HDL (VHDL-AMS or Verilog-AMS) and simulated using a mixed-signal simulator, such as ADVance MS^{TM}. Blocks that need to be modeled are either too complex on the transistor level, can be replaced by a digital model, or have highly active functionality therefore load the simulator heavily. The charge pump circuit is a highly active switching block which when replaced by a simple behavioral model can achieve speed gains in the order of hundreds, with good accuracy. Modeling this block will enable the simulation of complex systems such as LCD drivers, which are otherwise impossible to simulate at the system level.

ACKNOWLEDGEMENTS

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Appendix‡

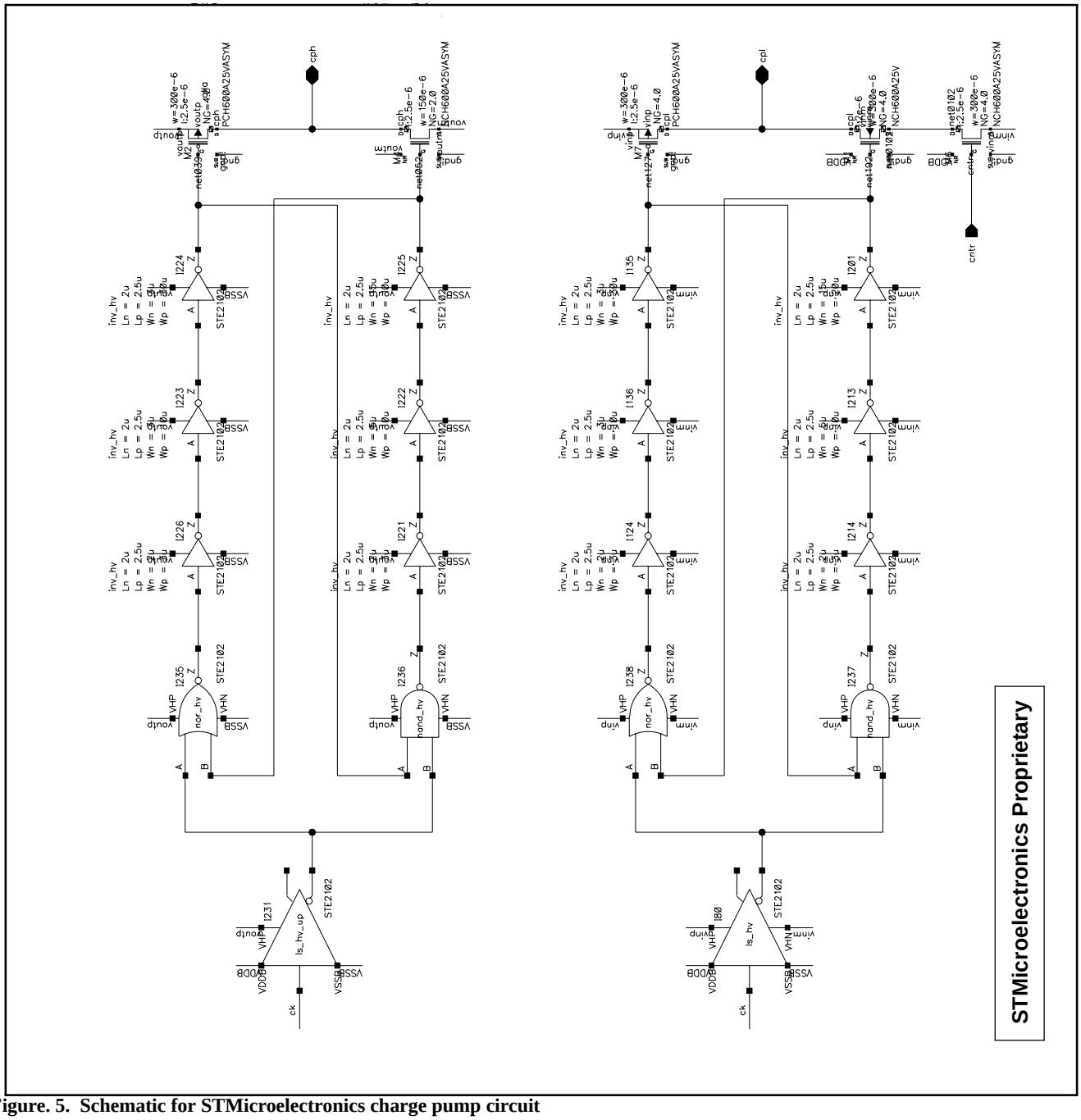

Figure. 5. Schematic for STMicroelectronics charge pump circuit

‡ Publication of the schematics authorized by Francesco Pulvirenti, Design Director of Display Division – STMicroelectronics (April 2007)