A Generic VHDL-AMS Behavioral Model Physically Accounting For Typical Analog Non-Linear Output Behavior

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ABSTRACT

This paper presents a VHDL-AMS behavioral model for a typical non-linear behavior commonly observed at the output of amplifier analog circuits. Based on a circuit-inspired modeling approach, the model offers a parameter-controlled non-linear output while preserving its electrical properties including DC operating point and dynamic output impedance. Connected in a common push-pull topology, hypothetical MOS-like devices were assumed where their behavior was abstracted to directly relate with the model parameters and consequently with the non-linear conduct of the output. The model operation is carefully studied and tested to demonstrate its potential usage as a flexible interfacial candidate for accurate design and verification purposes.

1. INTRODUCTION

The Vogue for mixed-signal verification methodologies has proved essential for debugging the ever-growing complexity of today's integrated SoCs. Given the diverse multiplicity of applications being tightly clustered in the same system, smart accurate test plans are carefully designed to minimize the duration of the design cycle. Most often, these verification plans require top-level simulations to be regularly effectuated during different design phases asserting the integral operation for the entire system [1]. This type of simulations is usually performed beyond the realm of SPICE kernels not only because of the lengthy computational cost involved, but also given the immaturity or even sometimes absence of the design constituent blocks depending on the design stage. In this situation, behavioral modeling is deployed to provide the fit-in pieces inside the composite puzzle, thus rendering verification runs possible at all validation phases.

Depending on the desired verification objective, the level of abstraction utilized during behavioral modeling development is decided. To become valid, an analog mixed-signal model not only should include the associated correct functionality but additionally, must demonstrate a good rapport with the surrounding interfacing blocks. Failure to do so may result in false misleading results, thus not fulfilling the intended verification objectives. This scenario can be strictly avoided by asserting that the model in question accounts for the correct impedance at its peripheral terminals. In other words, the model should be cautiously developed in order to provide the correct loading, thus faithfully undertaking the fidelity of the signal.

The above task comes to be challenging when functionality and loading are interdependent. A relevant example for such an encounter is a typical OPAMP characterized by a specific value for its output impedance. In this case, the latter should be regarded as valid only during the linear gain operation and should yield erroneous signal levels if used when the amplifier is driven into saturation. Such a violation of signal fidelity could become fatal affecting the overall system performance and accordingly restraining the useful role behavioral modeling can play.

Section 2 presents the conventional modeling approach and its limitations, while section 3 presents our circuit-inspired approach and its theory of operation. Model implementation is discussed in section 4, followed in section 5 by simulation results supporting our assumptions. In section 6, we will present a typical application for our model. Finally, our conclusion is provided in section 7.

2. CONVENTIONAL MODELING APPROACH AND LIMITATIONS

Developing a behavioral model for voltage saturation effect becomes straight forward using if-conditional statements. Figure 1 shows a schematic for the direct conventional approach modeling such an effect. A voltage controlled volt-

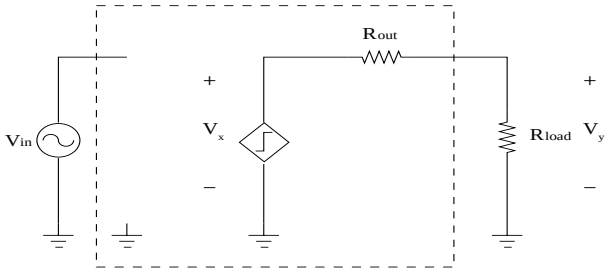

Figure. 1. Schematic for the conventional approach for modeling voltage saturation and output resistance

age source V_x is used to decide on the output voltage depend-

ing on the incoming signal level V_{in}. To model the output impedance, a series output resistance Rout is connected to V_x to result in the block output denoted by V_y. During linear operation, V_{in} is buffered through to V_x. On the other hand, non-linear operation is detected if V_{in} crosses the threshold limiting values V_{lim1} and V_{lim2}. Listing 1 gives a typical pseudocode relating between V_x and V_{in} for different regions of operation.

Listing 1. Pseudocode for voltage limiting in conventional approach model

```
if Vin < Vlim1 then
Vx = Vlim1
else if Vin > Vlim2 then
Vx = Vlim2
else Vx = Vin
```

Given its simplicity, the above approach is conventional when a voltage saturation effect is desired. Nevertheless, this technique should be used with considerable care since it may lead to erroneous results depending on the region of operation. While V_{in} falls within the predetermined limits V_{lim1} and V_{lim2}, V_y will be evaluated by voltage division of V_{in} between R_{load} and R_{out} and thus accurately accounting for the output resistance effect. On the other hand, assuming saturation operation, V_y, still determined by the same voltage division, will result in a signal saturated at levels below the desired output limits.

$$V_y = V_x \frac{R_{load}}{R_{out} + R_{load}} \quad (1)$$

To properly model the saturation behavior, we might argue that it suffices to decrease R_{out} thus driving V_y to approach V_{lim}. Nevertheless, this solution does not become practical since it requires a priori knowledge of R_{load}, needed to calculate the corresponding saturation limits for V_{in}, a condition that highly confines the versatility of the model.

3. A CIRCUIT-INSPIRED APPROACH

Based on a push-pull topology, a circuit inspired approach is used to develop an accurate behavioral model overcoming the above discussed limitations. As depicted in Figure 2, the assumed circuit mainly comprises of two complementary MOS-like devices with their common drain terminal providing an output voltage V_{out} while the input signal V_{in} is applied at their common gate terminal. The source terminal of the P-type device, representing the pull-up node, is tied to the higher voltage supply value V_{lim2}. Similarly, a pull-down to V_{lim1} is achieved by connecting the source of the N-type device to the lower voltage supply value V_{lim1}. With this configuration, the small signal output resistance seen at the output terminal is equivalent to the parallel combination of the output resistance for the complementary devices.

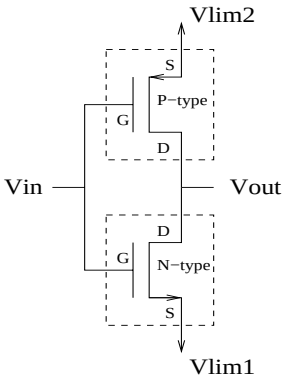

Figure. 2. Schematic diagram for assumed hypothetical circuit

3.1. Simplified Device Model

The transistor action governing our developed model was expressed in its fundamental form. This simplification step comes beneficial not only from a performance point of view but also facilitates devising a direct relation between the behavioral model controlling parameters and the transistor operation eventually determining the output behavior.

Similar to a MOS transistor model [3], three regions of operation were assumed to characterize the I-V relation of the N-type device† as follows:

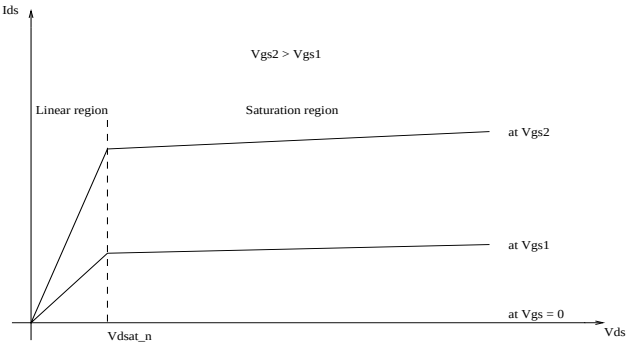

Figure. 3. Device I-V characteristics

For $V_{gs} < 0$

$I_{ds} = 0$, denoting cutoff region (2)

For $V_{gs} > 0$ and $V_{ds} < V_{dsat\_n}$

$I_{ds} = K V_{gs} V_{ds} (V_{dsat} / V_{dsat\_n})$, denoting linear region (3)

For $V_{gs} > 0$ and $V_{ds} > V_{dsat\_n}$

$I_{ds} = V_{gs} \lambda_n (V_{ds} - V_{dsat\_n}) + K V_{gs} V_{dsat}$, denoting saturation region (4)

† Similar equations for the P-type device were assumed by analogy.

The resulting device I-V characteristics is shown in Figure 3 In the above equation, the factor K relates current in the linear region and V_{gs} and is assumed to be 1 Siemens/Volt for simplification purposes. The Parameter V_{dsat_n} is used to define the saturation onset for the N-type device, whereas:

$$V_{dsat} = \frac{(V_{dsat\_n} + V_{dsat\_p})}{2} \quad (5)$$

The factor Lambda$_n$ (λ_n) which is constrained by: $0<(\lambda_n) < 1$ and is used to control the device output resistance in saturation since:

$$R_{sat\_n} = \frac{\partial V_{ds}}{\partial I_{ds}} = (V_{gs}\lambda_n)^{-1}, \quad (6)$$

It is important to note that the above equations as devised result in a transconductance (G_{mn}) independent of V_{gs} since:

$$G_{mn} = \frac{\partial I_{ds}}{\partial V_{gs}} = \lambda_n (V_{ds} - V_{dsat\_n}) + V_{dsat}. \quad (7)$$

In addition the onset saturation current I_{dsat} for both devices is balanced since, for the same $V_{gs/sg}$, the resulting current is made equal to:

$$I_{dsat} = V_{gs/sg} V_{dsat}. \quad (8)$$

3.2. Large Signal Behavior

To analyze the large signal behavior of this topology, consider the case when no load is connected. As the input voltage increases, V_{gs} increases, and V_{sg} decreases, forcing the n-type into the linear region of operation with small V_{ds}, and the p-type deeper into saturation with large V_{ds}. This continues until V_{ds} reaches zero and the output voltage is at the lower voltage limit (V_{lim1}). Similarly as the input voltage decreases, the output voltage reaches the upper voltage limit (V_{lim2}). During normal operation, when the output voltage is within the linear range, both devices are operating in the saturation region. Figure 4 shows the operating point in three cases; when the output was near the upper limit, when the output was near the lower limit, and when the output was at the midpoint between the two rails.

The factors V_{max1} and V_{max2} specify the point at which output voltage compression starts before reaching either limits, which in turn specifies $V_{dsat\_n/p}$ for each device using the relation:

$$V_{dsat\_n} = |V_{lim1} - V_{max1}|. \quad (9)$$

3.3. DC Characteristics

The DC characteristics of the described topology is divided into five regions as shown in Figure 5. The term $V_{dc\text{-}ideal}$ is the average of both limiting voltages V_{lim1} and V_{lim2}. In order to ensure that the output has maximum swing, the input is

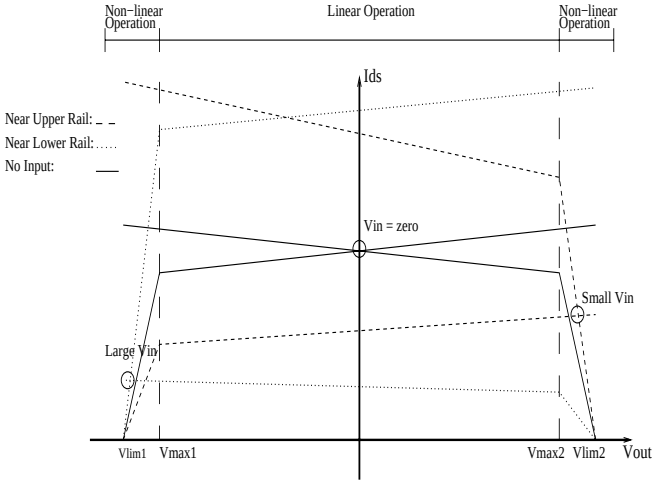

Figure. 4. I-V curves for both devices to demonstrate large signal push-pull behavior

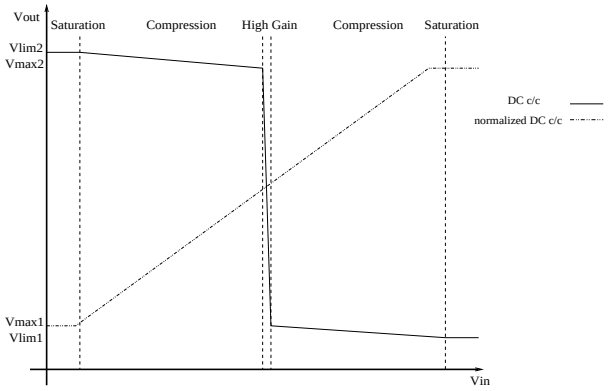

Figure. 5. DC characteristics for model with normalization and without normalization

biased to be in the middle of the high gain region by adding it to $V_{dc\text{-}ideal}$.

The small signal gain of such circuit is found to be equal to:

$$\text{Gain} = -(G_{mn} + G_{mp}) r_{out}. \quad (10)$$

Gain is calculated and is used to normalize the input voltage to maintain unity gain of the model. Having our model with unity gain is essential so as not to influence functionality of the output.

By dividing the input by the linear operation gain, which is larger than non-linear operation gain, we are further adding to the compression of the output voltage in non-linear operation and thus we have V_{max_n} and V_{max_p} as the effective voltage limits. Figure 5 shows the DC characteristics before and after normalization.

3.4. Output DC Level

The model's output DC level (Vdc_out) and output resistance (r_{out}), are used to determine the saturation output resistance of each device (R_{sat_n}, d R_{sat_p}). By adjusting the value of R_{sat_n} and R_{sat_p}, the DC voltage drop across each device is varied and an offset DC voltage is created.

4. MODEL IMPLEMENTATION

The model is implemented using VHDL-AMS hardware description language. The model has an input and an output port both of type electrical. Model parameters include limiting voltages (V_{lim1}, V_{lim2}), Output resistance (r_{out}), Output DC Level (V_{dc_out}) and start of non-linear operation voltages (V_{max1},V_{max2}). The code for the model is given in Listing 2. We made use of the mixed signal nature of the language by determining the device's region of operation with 'above statements, this way we can utilize the simulator's‡ mixed signal engine for better computational efficiency [2].

5. SIMULATION RESULTS

In this section we will present simulation results for tests performed on our model.

5.1. Output Impedance Test

Our first test verifies that the output resistance is equivalent to the user defined parameter r_{out} and that V_{dc_out} controls the DC level of the output. A Sinusoidal input is applied to the model, a load resistance of value equal to r_{out} is connected to the output and a transient analysis is performed. We observe that the output, as shown in Figure 6, has amplitude exactly half the amplitude of the input but shifted by a DC value equal to half of V_{dc_out} which indicates that the output resistance is equivalent to R_{load} and r_{out}.

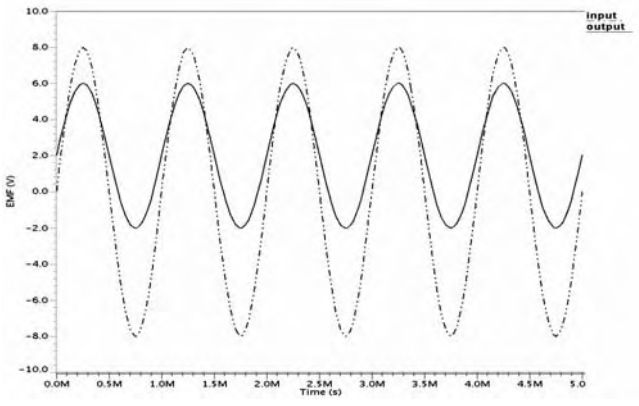

Figure. 6. Transient simulation result when R_{load} equals r_{out}

‡ All Simulations were performed using Mentor Graphics mixed signal simulator, ADVance MS™

Listing 2. VHDL_AMS code for output stage model

```
library IEEE ;
  use IEEE.electrical_systems.all;

entity output_stage is
generic ( Vlim2 : voltage :=  10.0 ; -- Upper limiting voltage
        Vlim1 : voltage := -10.0 ; -- Lower limiting voltage
         rout : resistance :=  1.0e3; -- Output resistance
         Vdc_out: voltage :=  0.0; -- DC out voltage
         Vmax1:real :=  -9.9; -- Lower saturation start Voltage
         Vmax2:real :=  9.9); -- Upper saturation start Voltage
port ( terminal ain : electrical; -- input terminal
       terminal aout : electrical); -- output terminal
end entity output_stage;

architecture A1 of output_stage is
  terminal aVdd , aVss , a_in : electrical ;
  quantity Vps across Ips through aVdd;
  quantity Vns across Ins through aVss;
  quantity Vin   across ain ;
  quantity V_in  across Iin through a_in ;
  quantity Vgs  across a_in to aVss ;
  quantity Vsg  across aVdd to a_in ;
  quantity Vds across Ids through aout to aVss ;
  quantity Vsd across Isd through aVdd to aout ;
  constant Vdc_ideal: real :=  0.5*(Vlim2+Vlim1);
  constant Vdsat_n  : real := abs(Vlim1-Vmax1);
  constant Vdsat_p  : real := abs(Vlim2-Vmax2);
  constant Vdsat    : real := 0.5*(Vdsat_n+Vdsat_p);
  constant VSD_DC : real := Vlim2 - Vdc_out - Vdsat_p;
  constant VDS_DC : real := Vdc_out - Vlim1 - Vdsat_n;
  constant rN : real := rout*(1.0 + (VDS_DC)/(VSD_DC));
  constant rP : real := rN*(VSD_DC)/(VDS_DC);
  constant lambdaP : real := 1.0/(((Vlim2-Vdc_ideal)*rP));
  constant lambdaN : real := 1.0/(((Vdc_ideal-Vlim1)*rN));
  constant GmP : real := lambdaP*(VSD_DC) + Vdsat;
  constant GmN : real := lambdaN*(VDS_DC) + Vdsat;
  constant gain: real := - (GmP + GmN)*rout;
begin

  V_in == Vin/gain + Vdc_ideal;
  Vps == Vlim2;
  Vns == Vlim1;

  if not Vgs'above(0.0) use Ids == 0.0;
  elsif not vds'above(Vdsat_n) use Ids*Vdsat_n == Vgs*Vds*Vdsat;
  else Ids == Vgs*lambdaN*(Vds-Vdsat_n) + Vgs*(Vdsat);
  end use;

  if not Vsg'above(0.0) use Isd == 0.0;
  elsif not vsd'above(Vdsat_p) use Isd*Vdsat_p == Vsg*Vsd*Vdsat;
  else Isd == Vsg*lambdaP*(Vsd-Vdsat_p) + Vsg*(Vdsat);
  end use;

  break on  Vgs'above(0.0),Vsg'above(0.0);
  break on  Vds'above(Vdsat_n),Vsd'above(Vdsat_p);
end architecture A1;
```

5.2. Loading Effect Test

Our second test compares between the implemented model and the conventional approach model discussed in section 2.1 in terms of their reaction to loading and how this affects their DC characteristics. A DC analysis is performed while sweeping the value of the input voltage showing the DC characteristics when no load is connected and when R_{load} is connected to the output with equal value to r_{out}. By examining the case where $R_{load} = r_{out}$ we find the following: For the simple model, the output is not limited at the value V_{max1} and V_{max2}, but scaled by the voltage division factor between r_{out} and R_{load} while our model did not reach the limiting voltages due to loading. Figure 7 shows the simulation results for the conventional approach model, while Figure 8 shows the results for our circuit-inspired model.

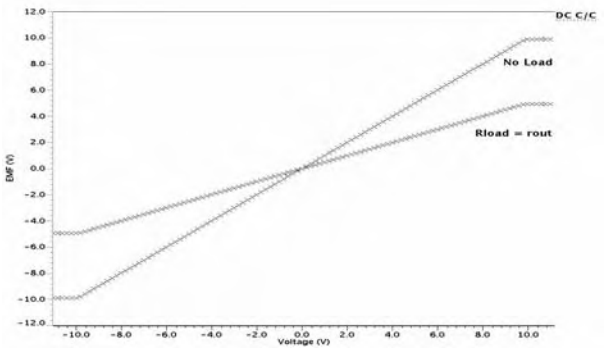

Figure. 7. Results from simulation showing the effect of loading on the conventional approach model

6. APPLICATION

A typical application for our model is its usage as an amplifier output stage. The model could be connected to the amplifier output, thereby modeling amplifier functionality within the main model leaving output saturation, output DC level, and output resistance for the output stage model. Our model was tested with an operational amplifier model, and it showed ease of convergence in different feedback configurations.

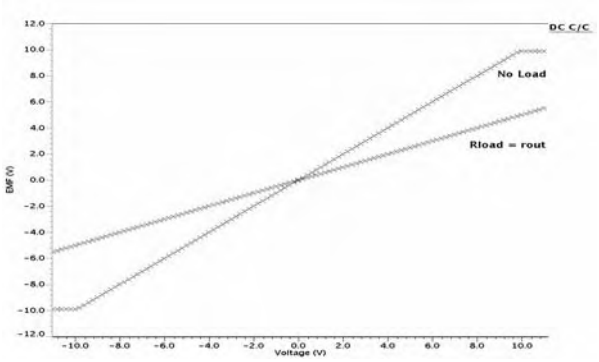

Figure. 8. Results from simulation showing the effect of loading on our circuit-inspired model

7. CONCLUSION

We have presented a model that accurately models output voltage saturation and output resistance in a way that preserves their interaction. Our model is derived by abstracting circuit physics. We have shown through simulations that our modeling approach successfully captures these inter-related effects. We have shown a typical application for our model and how it provides a solution for modeling amplifier output characteristics.

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