A Generic VHDL-AMS Behavioral Model Physically Accounting For Analog Non-Linear Output Behavior

Kamal Sabet

Tamer Riad

Mentor Graphics®

Outline

- Introduction
  - Modeling AMS Systems
- Analog Output Behavior
  - Conventional Modeling Approach
  - Circuit Inspired Approach
- Model Implementation
- Experimental Results
- Application
- Conclusion

Introduction

- Mixed-signal verification has proved essential for debugging today's integrated SOCs.
- To assert the integral operation of the entire system, several top-level simulations have to be performed.
- Extensive computational cost and design immaturity require top-level simulation to be performed beyond the realm of SPICE kernels.

Modeling AMS Systems

- A valid AMS system's models must capture the correct functionality of their corresponding blocks.
- In addition, accurate interfacing must correctly account for the correct impedance at the peripheral terminals.
- This becomes a challenge when functionality and loading are interdependent.

Analog Output Behavior

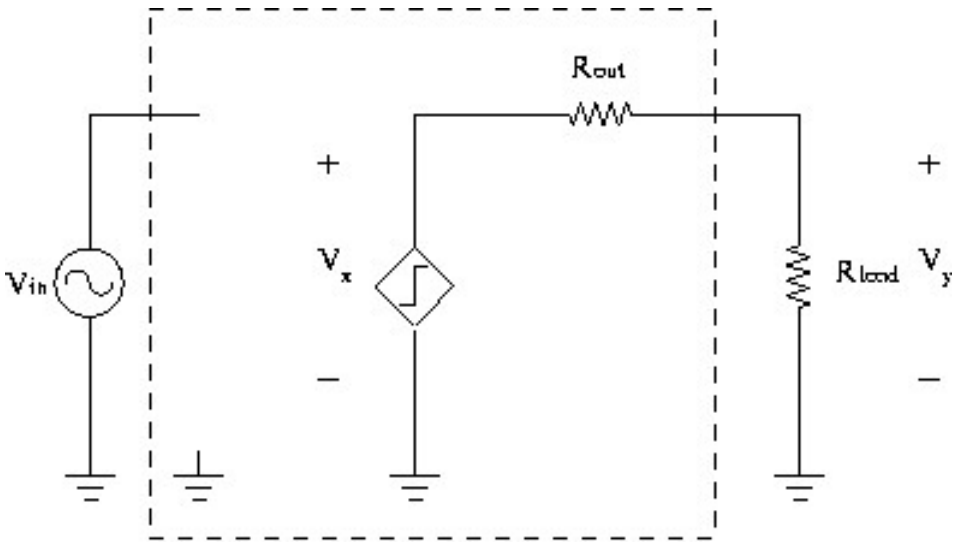
- Common output characteristics
  - Output voltage saturation
  - Output resistance
  - Output DC level
  - Output capacitance
  - Output current limiting

Modeling Voltage Saturation & Output Resistance

- Has to be valid in both linear and non-linear operation.
- The value of output resistance should change from one mode of operation to the other.
- Assuming it to be the same, will yield erroneous results, which would restrains the use of this model.

Conventional Modeling Approach

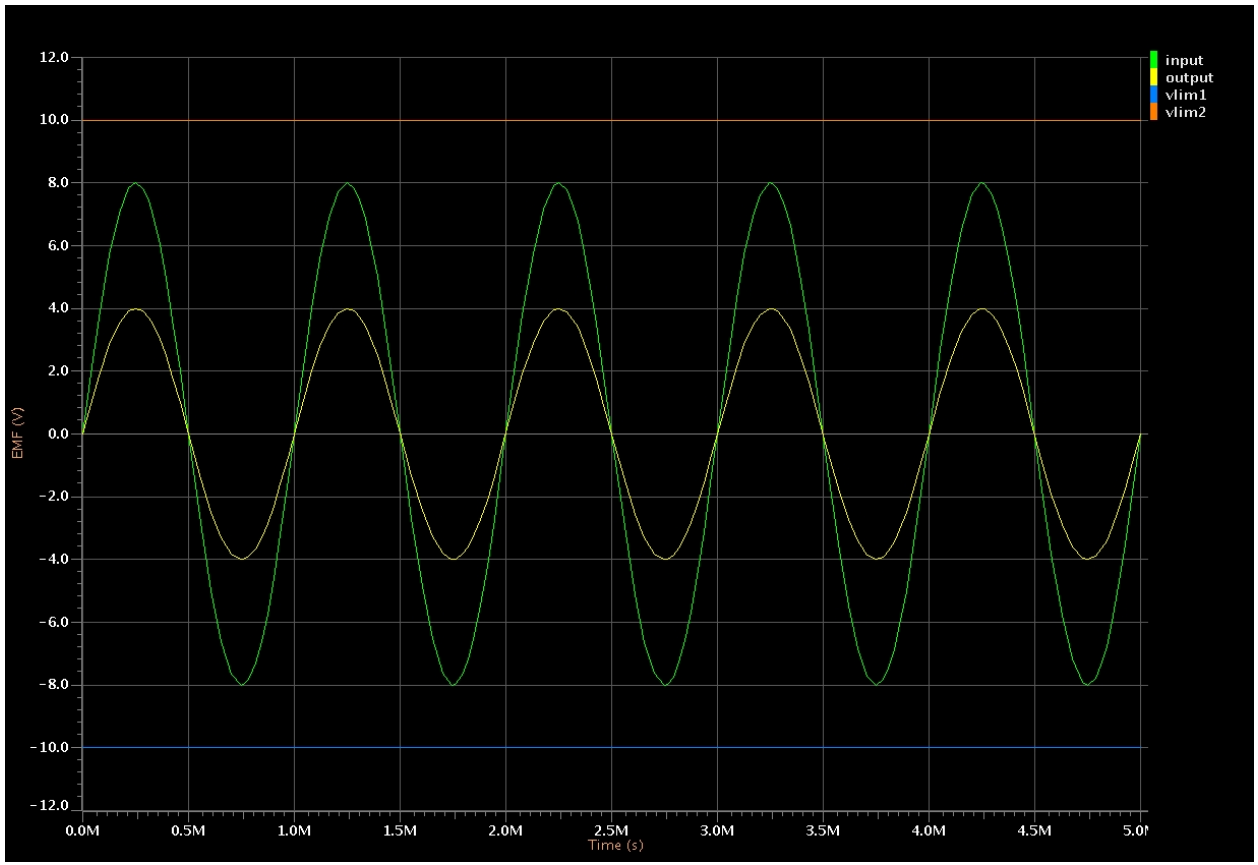
The controlled source V_x is used to decide on the output voltage V_y depending on V_{in}.



If Vin < Vlim1
Vx = Vlim1
else if Vin > Vlim2
Vx = Vlim2
else
Vx = Vin

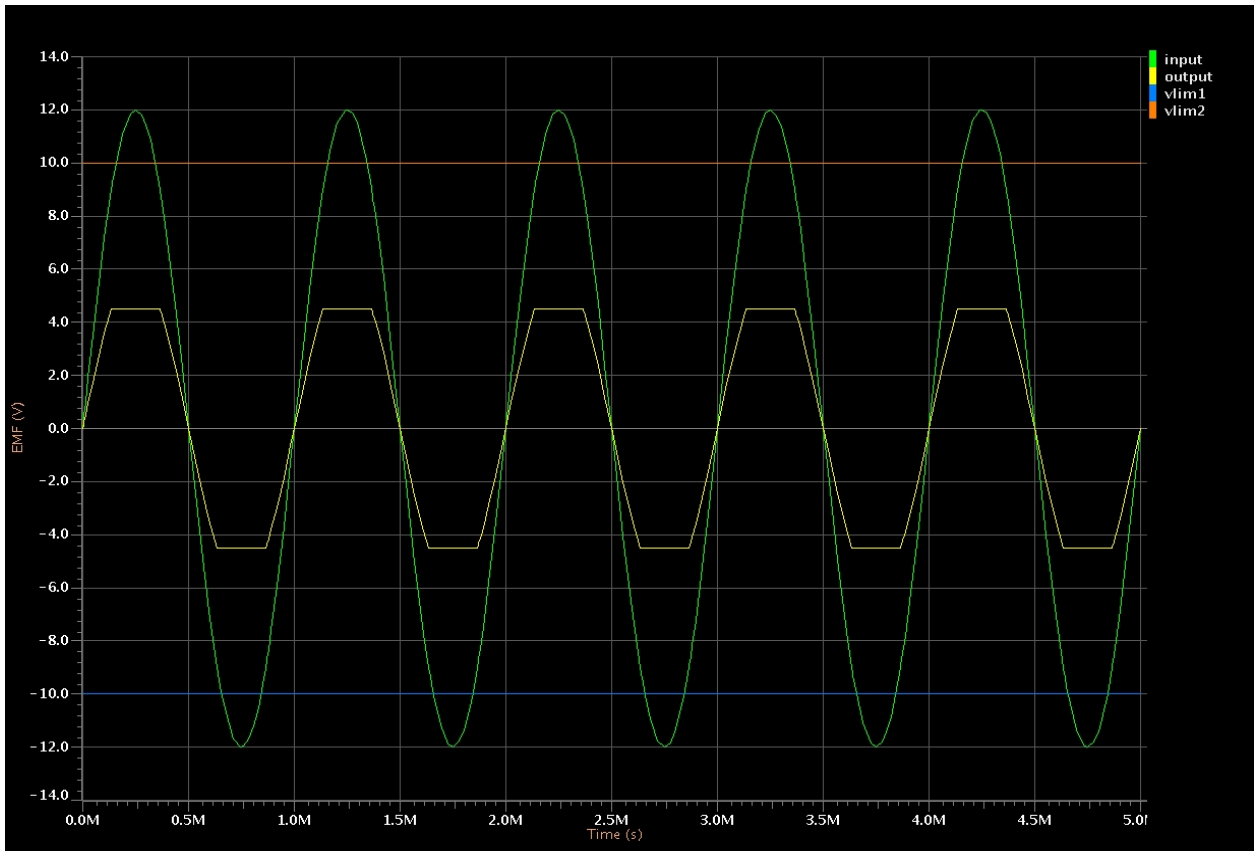
Conventional Modeling Approach (cont'd)

During linear operation, V_y will be evaluated by voltage division of V_{in} between R_{load} and R_{out}.



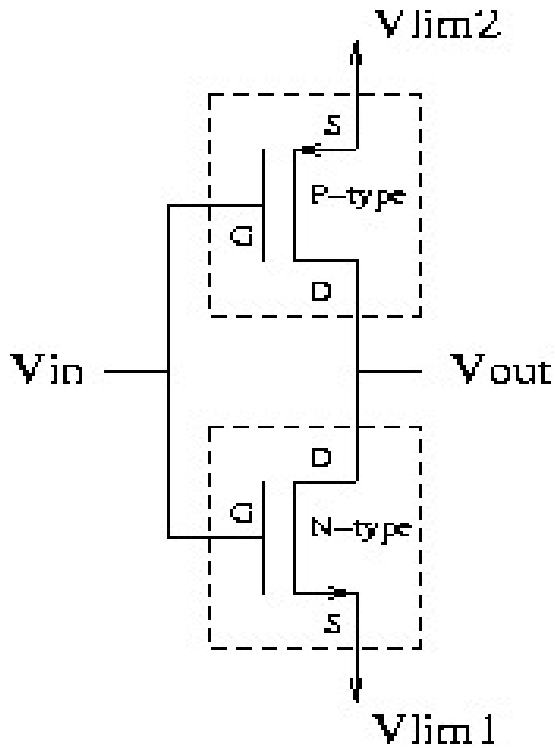
Conventional Modeling Approach (cont'd)

During non-linear operation, voltage division will result in a signal saturated at levels below the desired output limits.



Circuit Inspired Approach

- Assumed circuit comprises of 2 hypothetical MOS-like devices connected in a push-pull topology.
- Input common to both gates, output at their drains.
- Power supplies are the limiting voltages.

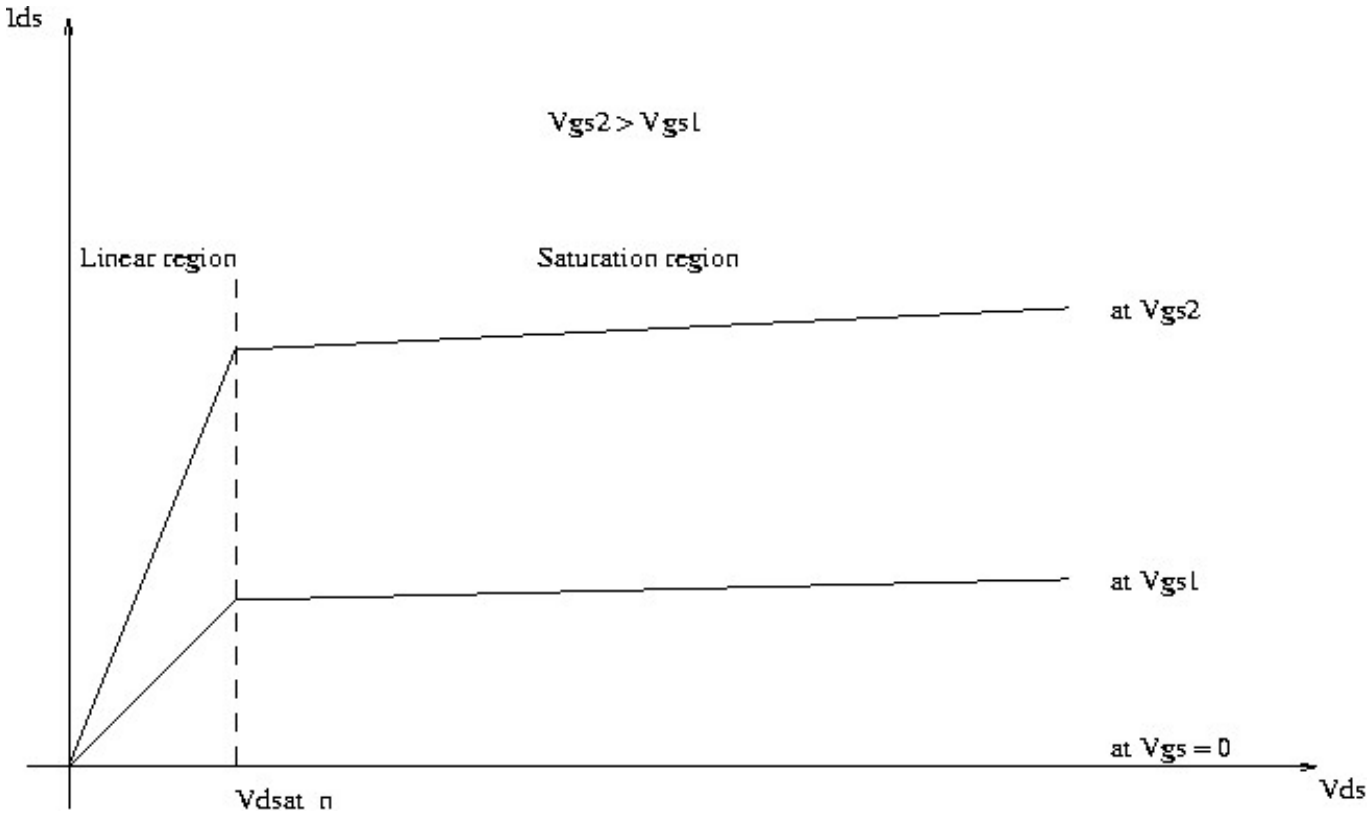


Simplified Device Models

- Circuit inspired approach uses Abstracted transistors.
- Expresses Basic transistor action.
- Preserves relations between model parameters and device parameters.
- Starting point is MOS level 1 equations.

Device I-V Characteristics

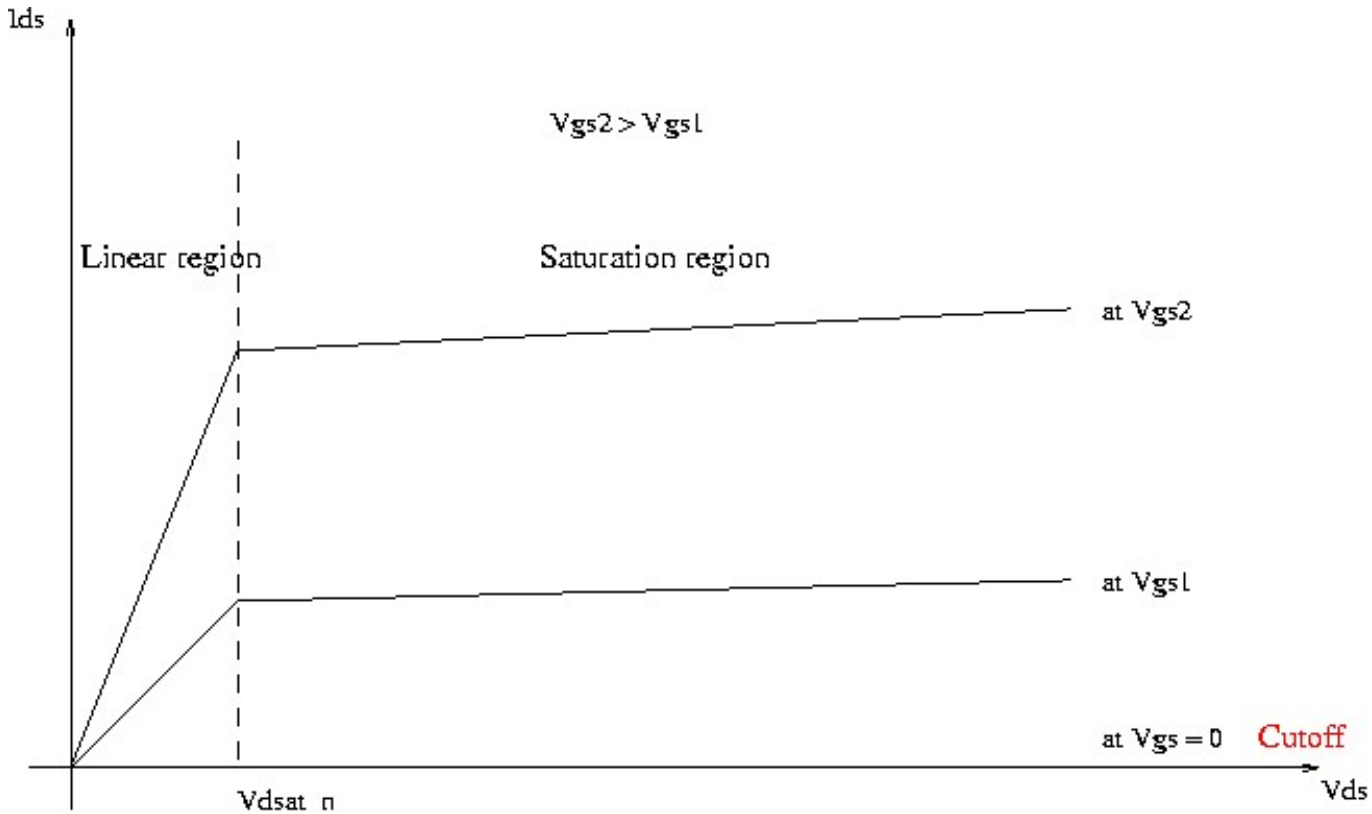
- 3 Regions of operation
- 2 Linear Equations



Device I-V Characteristics (cont'd)

- **Cutoff operation** $V_{gs} < 0$

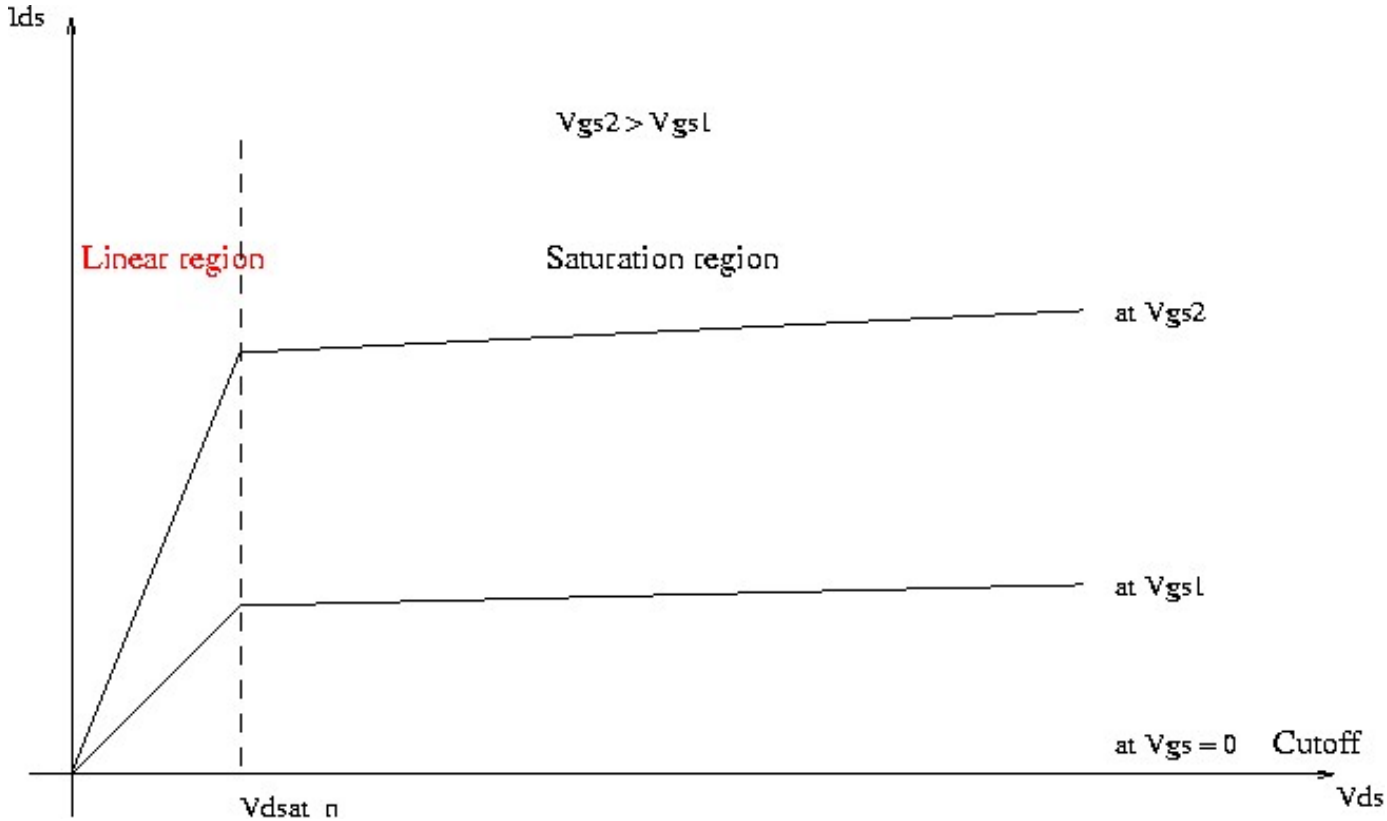
  $I_{ds} = 0$



Device I-V Characteristics (cont'd)

- Linear operation $V_{gs} > 0$ & $V_{ds} < V_{dsat\_n}$

  $I_{ds} = K V_{gs} Vds (V_{dsat} / V_{dsat\_n})$



Device I-V Characteristics (cont'd)

- Linear operation $V_{gs} > 0$ & $V_{ds} < V_{dsat\_n}$

  $I_{ds} = K\, V_{gs}\, V_{ds}\, (V_{dsat} / V_{dsat\_n})$

  Where;

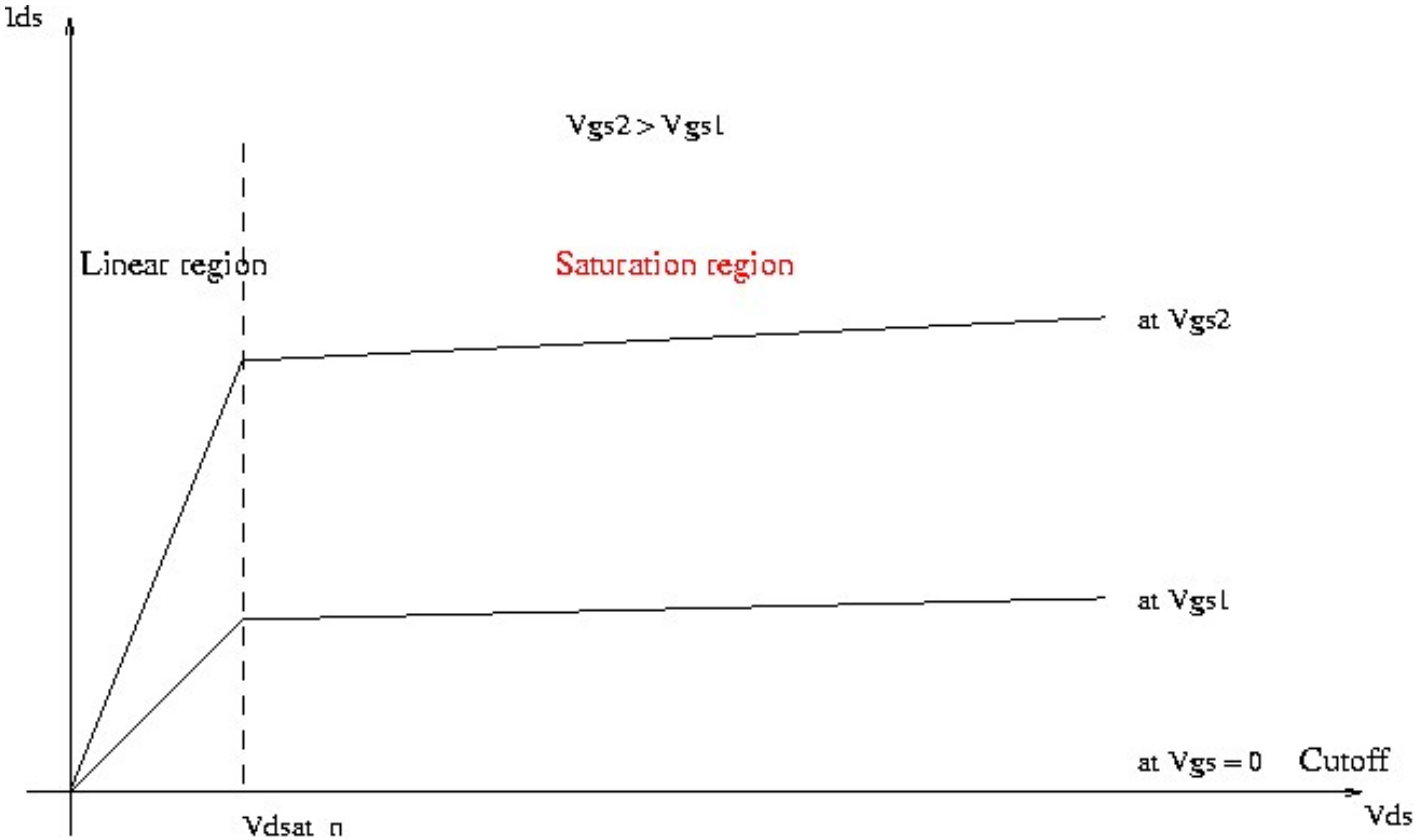
  - K : relates I_{ds} to V_{gs} = 1 S/V for simplicity
  - V_{dsat_n} : Defines onset of saturation
  - $V_{dsat} = (V_{dsat\_n} + V_{dsat\_p})/2$: Used to balance Idsat for both devices.

    For the same $V_{gs}\backslash V_{sg}$: $I_{dsat} = V_{gs}\backslash V_{gs}\, V_{dsat}$

Device I-V Characteristics (cont'd)

- **Saturation operation** $V_{gs} > 0$ & $V_{ds} > V_{dsat\_n}$

$$I_{ds} = V_{gs}\,\lambda_n\,(V_{ds} - V_{dsat\_n}) + K\,V_{gs}\,V_{dsat}$$



Device I-V Characteristics (cont'd)

- Saturation operation for $V_{gs} > 0$ & $V_{ds} > V_{dsat\_n}$

  $I_{ds} = V_{gs}\,\lambda_n\,(V_{ds} - V_{dsat\_n}) + K\,V_{gs}\,V_{dsat}$

  Where;

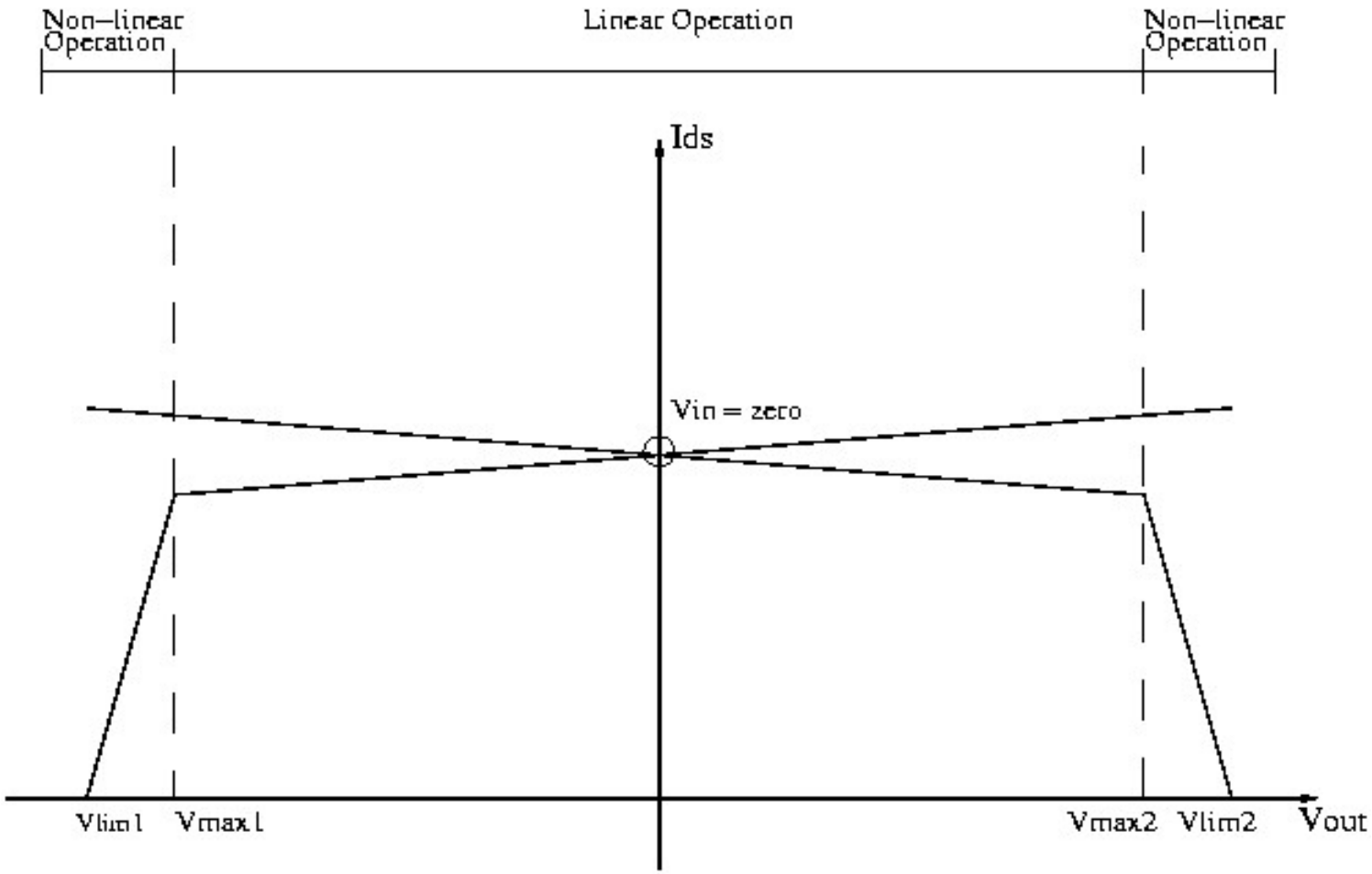
  - λ_n: Controls device output resistance in saturation

    $R_{sat\_n} = \delta V_{ds}/\delta I_{ds} = 1/(V_{gs}\lambda_n)$

  - Device transconductance $G_{mn} = \lambda_n(V_{ds} - V_{dsat\_n}) + KV_{dsat}$

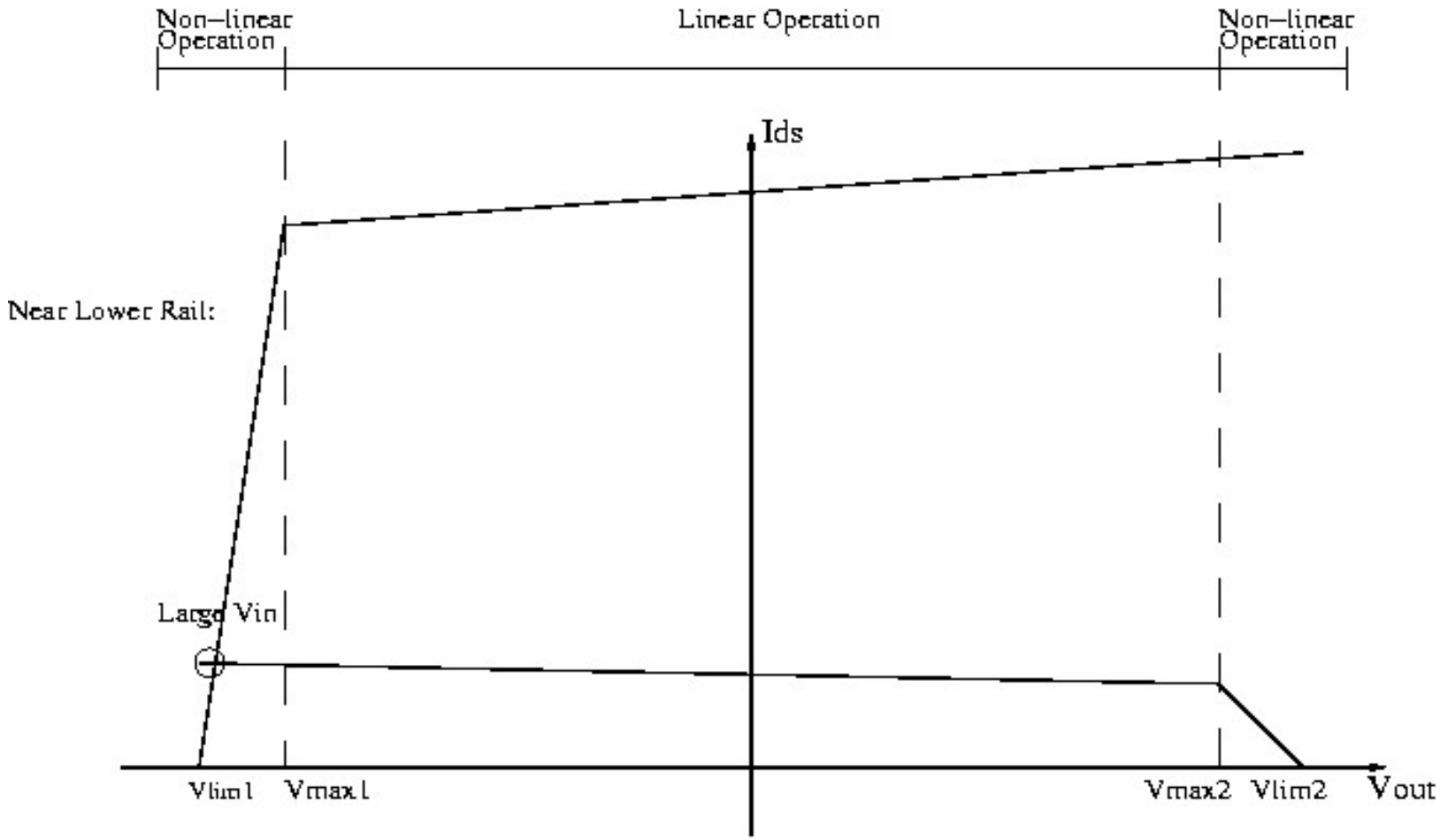
    * G_{mn} independent of V_{gs}

Large Signal Behavior



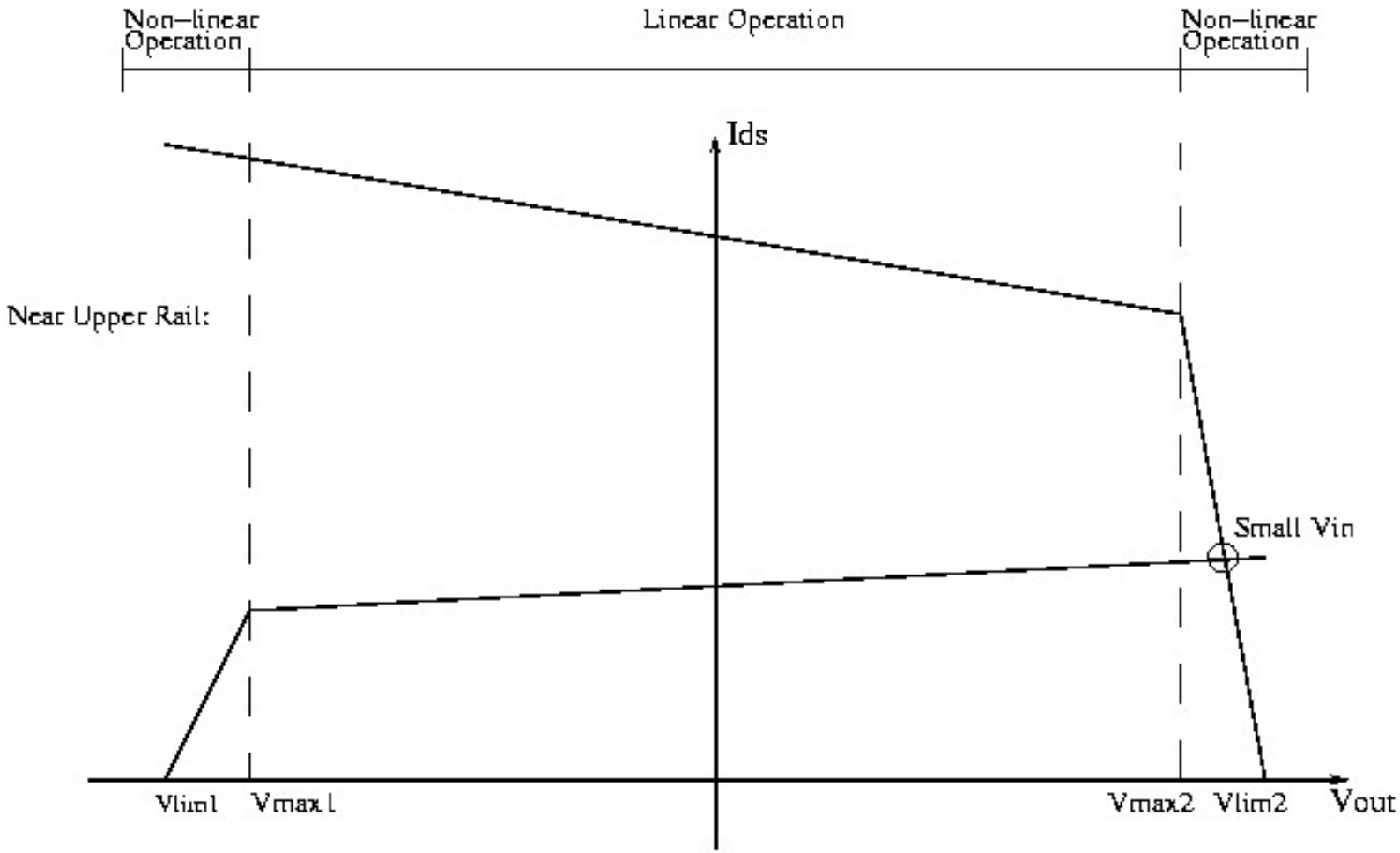
$V_{in}=0,\ V_{gs}=V_{sg}$

Large Signal Behavior (cont'd)



V_{in} Increases, V_{gs} Increases, V_{sg} Decreases, V_{out} goes nearer to the lower rail

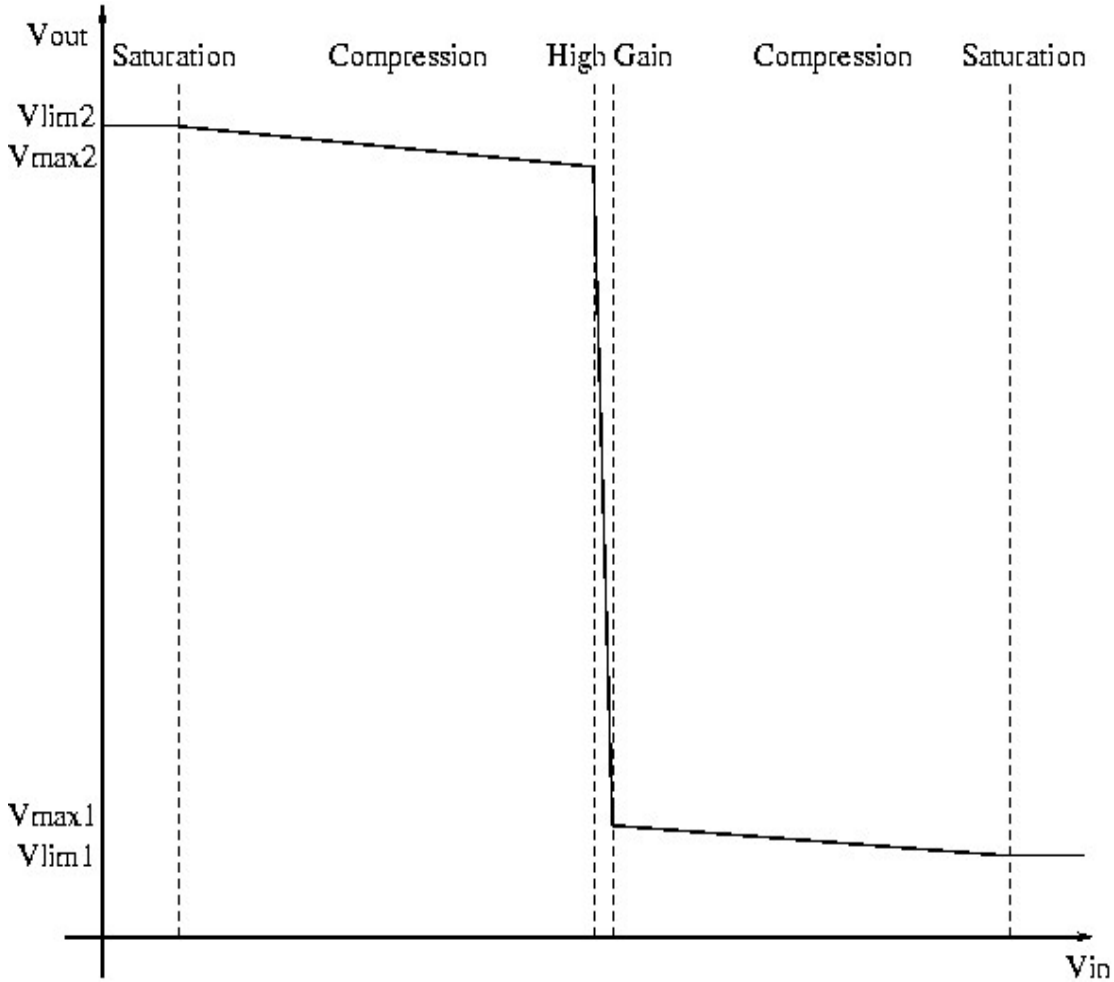
Large Signal Behavior (cont'd)



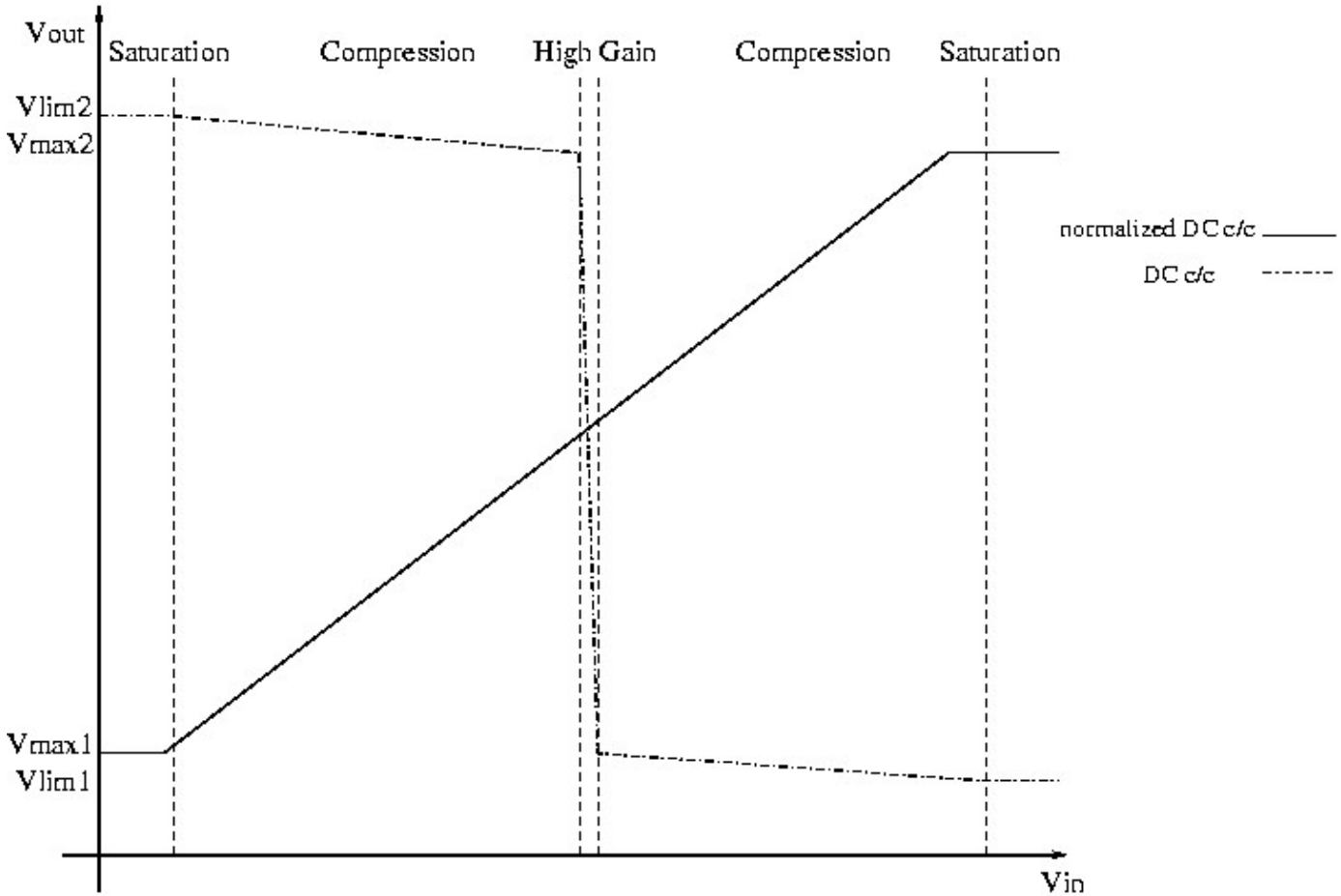
V_{in} Decreases, V_{gs}Decreases, V_{sg} Increases, V_{out} goes nearer to the upper rail

DC Characteristics

- Divided into 5 Regions.
- Gain = -(Gmn + Gmp)Rout
- Required model has to have unity gain, normalization is needed.
- To insure maximum swing for o/p, biasing is needed.



DC Characteristics (cont'd)



$V = V_{in}/Gain + V_{dc\_ideal}$

$V_{dc\_ideal} = (V_{lim1} + V_{lim}2)/2$

Output DC Level

- **An Output DC level is created by adjusting the values of each device's resistance in saturation.**

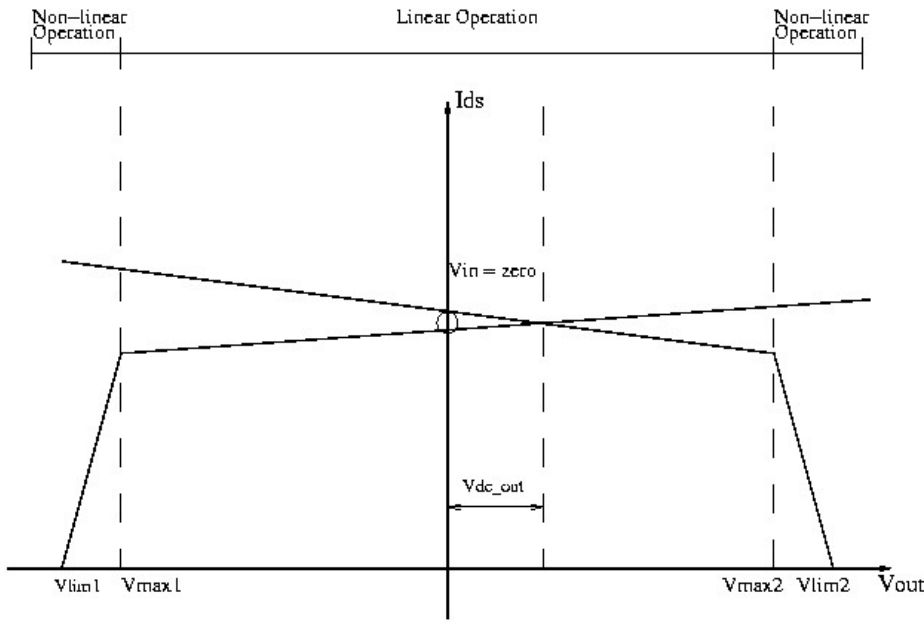
To calculate each device resistance using the user-defined output resistance and output DC level, we use the following equations :

VSD_DC = Vlim2 - Vdc_out - Vdsat_p

VDS_DC = Vdc_out - Vlim1 - Vdsat_n

Rsat_n= rout*(1.0 + (VDS_DC)/(VSD_DC));

Rsat_p= Rsat_n*(VSD_DC)/(VDS_DC);



Model Implementation

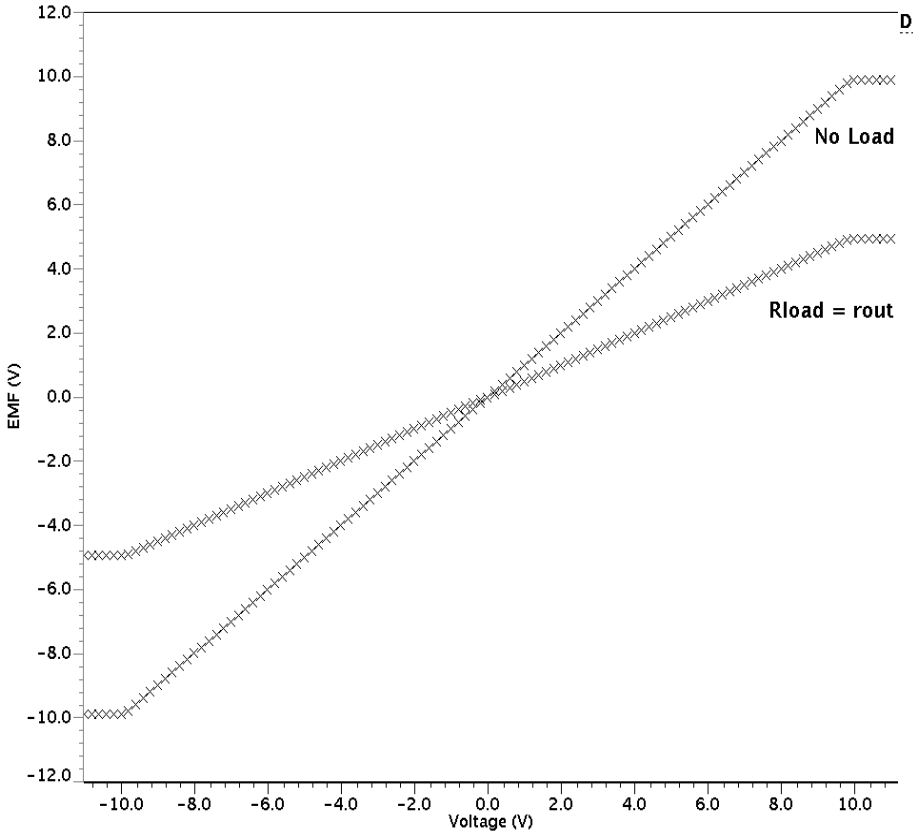
- Implemented using VHDL-AMS
- Electrical input and output ports
- Parameters:
  - Limiting voltage
  - Output resistance
  - Output DC level
- Coding makes use of the language's mixed-signal nature utilizing simulator's mixed-signal kernel for better computational efficiency

```
entity output_stage is
generic ( Vlim2 : voltage := 10.0 ; -- Upper limiting voltage
Vlim1 : voltage := -10.0 ; -- Lower limiting voltage
rout : resistance := 1.0e3; -- Output resistance
Vdc_out: voltage := 0.0; -- DC out voltage
Vmax1:real := -9.9; -- Lower saturation start Voltage
Vmax2:real := 9.9); -- Upper saturation start Voltage
port ( terminal ain : electrical; -- input terminal
terminal aout : electrical); -- output terminal
end entity output_stage;
architecture A1 of output_stage is
.....
V_in == Vin/gain + Vdc_ideal;
Vps == Vlim2;
Vns == Vlim1;
if not Vgs'above(0.0) use Ids == 0.0;
elsif not vds'above(Vdsat_n) use Ids*Vdsat_n ==
Vgs*Vds*Vdsat;
else Ids == Vgs*lambdaN*(Vds-Vdsat_n) + Vgs*(Vdsat);
end use;
if not Vsg'above(0.0) use Isd == 0.0;
elsif not vsd'above(Vdsat_p) use Isd*Vdsat_p ==
Vsg*Vsd*Vdsat;
else Isd == Vsg*lambdaP*(Vsd-Vdsat_p) + Vsg*(Vdsat);
end use;
break on Vgs'above(0.0),Vsg'above(0.0);
break on Vds'above(Vdsat_n),Vsd'above(Vdsat_p);
end architecture A1;
```

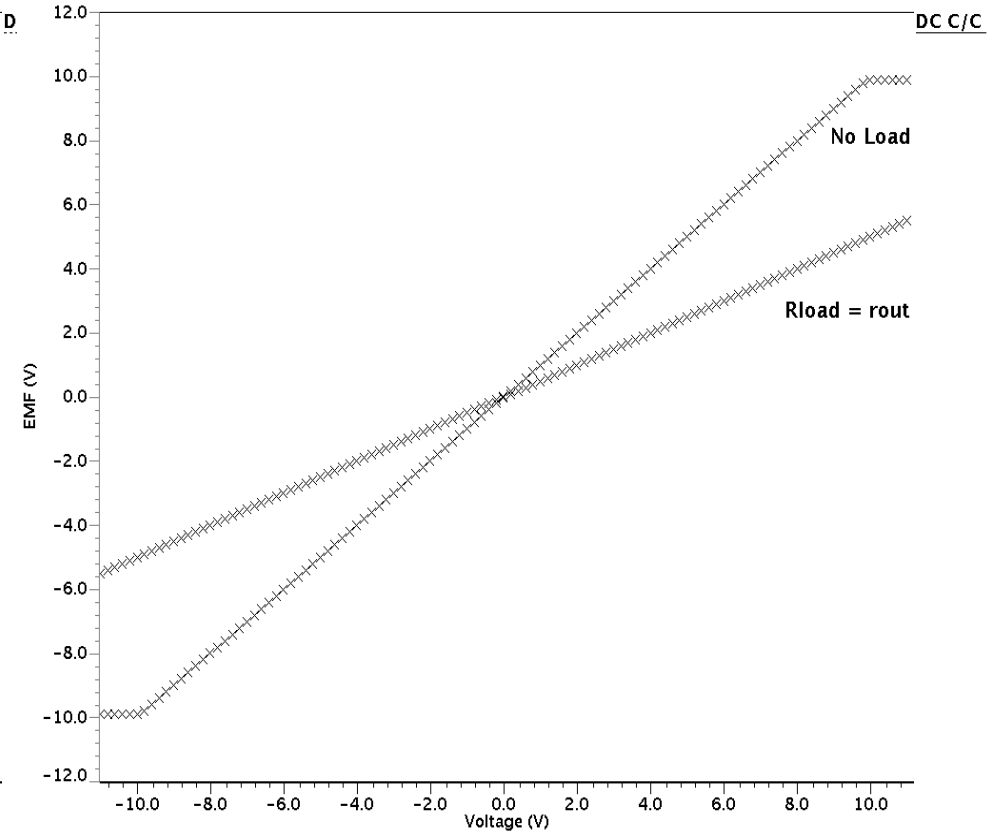
Experimental Setup

- Simulations performed using Mentor Graphics, ADVance MS™ mixed signal simulator.
- Loading effect test performed on both the conventional approach model and our proposed model.
  - A DC analysis is performed while sweeping input Voltage both with and without load.

Experimental Results



Conventional Approach



Circuit inspired Approach

Application

- Typical application for model would be as an amplifier output stage.
- Simplifies amplifier modeling to input characteristics and core functionality(gain, frequency response).
- In case of balanced differential output, model could be instantiated twice with parameters adjusted to account for differential characteristics.
- Model was used as an opamp output stage and it showed ease of convergence in different feedback configurations.

Conclusion

- Modeling analog output behavior should preserve interaction between voltage saturation and output resistance.
- Disregarding such interaction will lead to erroneous results restraining the use of the behavioral model.
- Using abstracted circuit physics successfully captures these inter-related effects.
- Our model provides a solution for modeling output characteristics of an amplifier .

Thank You