An Accurate PLL Behavioral Model for Fast Monte Carlo Analysis under Process Variation

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Abstract

Hierarchical statistical analysis using the regression-based approach is often used to improve the extremely expensive HSPICE Monte Carlo (MC) analysis. However, accurately fitting the regression equations requires many simulation samples. In this paper, an accurate Behavioral Monte Carlo Simulation (BMCS) approach to analyze PLL designs under process variation is developed by building a bottom-up behavioral modeling approach with an efficient extraction process. Using the accurate model, we also develop a modified sensitivity analysis for process variation effects to provide accurate enough results with less regression cost. As shown in the experimental results, we reduce the simulation time of HSPICE MC analysis from several weeks to several hours and still retain similar statistical results as in HSPICE MC simulation.

1. INTRODUCTION

Traditional HSPICE Monte Carlo (MC) analysis is often used to analyze the statistical results under process variation by performing many expensive transistor-level simulations. Hierarchical statistical analysis [1]-[6] is a popular approach to solve the speed issue of HSPICE MC analysis. Because system-level performance of analog circuits is hard to be directly modeled as a function of device variations, the regression process is often divided into two level modeling. The device-level variation models can be obtained from IC foundries and used to form the regression equations for the variation models of some intermediate-level circuit properties, such as timing, current, and frequency information. Other equations are then regressed to model the system-level circuit performance under process variation. The lock voltage and lock time of a Phase Lock Loop (PLL), for example, can be modeled as some equations according to the variation of intermediate-level circuit properties.

A popular approach to build those regression equations is the response surface methodology (RSM) technique [1, 4-6]. Although some techniques [5] can reduce the regression complexity, the number of training samples is still about 4 times greater than the number of unknown coefficients, which still requires too many transistor-level simulations. The other issue of regression-based approaches is the poor observability of the analysis results. Since the circuit performance is modeled as a function of the parameter variation, only some statistical numbers can be calculated in the analysis. The detailed information of circuit responses, such as the locking waveform of a PLL under process variation, cannot be provided for designers to improve their circuits if necessary.

Therefore, in some approaches [1]-[4], intermediate-level parameters are used to build a corresponding behavioral model of the circuit. Using suitable behavioral models, Behavioral Monte Carlo Simulation (BMCS) can be performed to generate the corresponding output waveforms and estimate the performance shift under process variation. Because behavioral simulation is often very fast, the MC analysis results can be obtained in a short time with detailed circuit behavior. However, the accuracy of behavioral models is the most critical issue in BMCS-based approaches. If the behavioral model is not accurate enough, accurate MC analysis results are hard to be obtained even if high-order regression equations are used to reflect the process variation effects.

In this paper, an efficient BMCS approach to analyze PLL designs under process variation is developed by this modeling approach. We first use an efficient bottom-up approach to generate accurate behavioral models for IP-based designs. The key concept is using a special "characterization mode" to acquire required circuit parameters. Only one input pattern in this extraction mode is sufficient to obtain all actual circuit properties with parasitic and loading effects. Using our modeling approach, simple relationships to reflect the process variation effects are accurate enough without high-order regression equations as shown in the experimental results. Therefore, we adopt sensitivity analysis (S_E) to find out the relationship between our behavioral parameter variation and the device variation with less regression efforts.

However, traditional sensitivity method may induce too many errors on the analog blocks, such as modeling the variations of charge pump (CP) and voltage-controlled oscillator (VCO). Therefore, we also develop the modified S_E strategies for these two blocks without extra simulation cost. For each considered device variation parameter, using two-run extractions in our efficient characterization mode is enough to find out the relative modified sensitivity values for all behavioral parameters in our model. Then these parameters can be adjusted when every device variation values are randomly generated in the MC analysis. Using the adjusted behavioral model, we can perform a fast behavioral simulation and obtain accurate responses under process variation, as illustrated in Figure 1.

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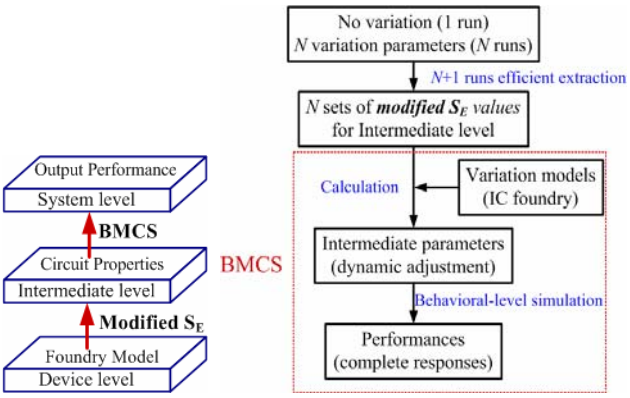

Figure 1. Our hierarchical statistical analysis and BMCS flow

The remainder of this paper is organized as follows. The methods to apply sensitivity analysis in our developed efficient behavioral modeling approach are introduced in Section 2. Modeling strategies using our developed modified sensitivity analysis for CP and VCO block is explained in Section 3. The experimental results are provided in Section 4 to demonstrate that our approach deals with process variation accurately by using a simple behavioral model. Conclusions are finally drawn in Section 5.

2. PROCESS-VARIATION-AWARE MODEL

In this section, we will introduce the bottom-up extraction flow to generate accurate behavioral models for existing PLL designs. The key concept is using a special "characterization mode" to acquire required circuit parameters. The PLL design in the characterization process does not have to operate as in a real system. In this way, the required parameters can be obtained faster and time-consuming correlation analysis can be avoided for building accurate models. We will also explain how to extend this extraction flow to build a variation-aware behavioral model for a given PLL design.

According to previous researches [7], we choose four transistor parameters, ΔW, ΔL, ΔV_t and ΔT_{ox}, which are considered to have more contributions on performance shift, as the random variables of the MC analysis in this work. To be more realistic, we use the same variation models as in the SPICE MC model provided by TSMC during our experiments. In the provided MC model, these four parameters are independently described by different random generators. Therefore, we model our behavioral parameters as a function of process parameters and find out their sensitivities independently. Taking the delay time (T_d) as an example, the timing change (ΔT_d) under process variation can be simply modeled by the sensitivity analysis, as shown in (1),

$$\Delta T_d = T_d(\Delta x_i) - T_{d0} \approx \frac{\partial T_d}{\partial x_i} \times \Delta x_i \qquad (1)$$

where T_{d0} is the nominal delay without process variation, $\partial T_d / \partial x_i$ is the delay sensitivity to the process parameter x_i.

2.1. Characterization Mode

In our developed characterization mode, we break the PLL loop without separating it into independent blocks as shown in Figure 2. The broken connection helps us to send special patterns and quickly trigger the PLL into different situations. Moreover, simulating every PLL blocks together allows automatic parasitic and loading effect consideration. This methodology is more suitable for existing IPs, avoiding tedious layout-tracing steps. Only one pattern in this mode can trigger the design and extract all required characteristic parameters from simulation results. Major factors affecting PLL performance include the timing information of phase frequency detector (PFD) and frequency divider, the current information of CP and loop filter (LF) block, and the frequency information of VCO. These factors can be obtained by using this approach without detailed circuit structure and device size information.

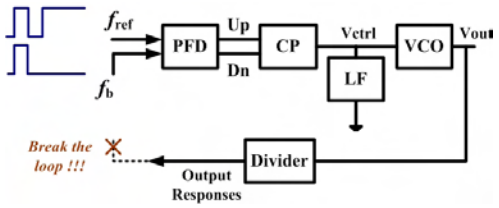

Figure 2. Developed characterization mode of PLL

Since the behavioral model parameters are directly obtained from voltage-domain measurement, it is convenient for us to use simple sensitivity analysis to find out the relationship between those parameters and process variation. In our approach, besides the original extraction process to build the behavioral model without process variation, we only need another four runs of the extraction process. By comparing each parameter value under device variation to the value without device variation, four different sets of S_E values can be obtained for the four different device-level variations. Taking the delay change under width variation ($T_{d,\Delta W}$) as an example, we can model the relationship using a sensitivity value ($S_{E,Td\_\Delta W}$) as shown in (2). Because the developed extraction process is very efficient, five runs of such extraction process will require much less simulation time than fitting the complicated regression equations in traditional approaches, as demonstrated in the experimental results.

$$S_{E,Td\_\Delta W} = \frac{\partial T_d}{\partial W} \approx \frac{\Delta T_d}{\Delta W} = constant \qquad (2)$$

While performing MC analysis using our behavioral models, the changes of behavioral model parameters can be calculated according to their sensitivity when every device variation values are randomly generated. Since the contribution of each device variation is treated as independent in foundry model, we use linear function to obtain the final value of each behavioral model parameter, as demonstrated by the delay time (T_d) in (3). Our approach does not assume any specific distribution of the device parameters. Therefore, any kind of probability distribution can be used in our BMCS approach to obtain accurate statistical results.

$$T_d = T_{d0} + \Delta W \times S_{E,T_{d\_\Delta W}} + \Delta L \times S_{E,T_{d\_\Delta L}} + \Delta V_t \times S_{E,T_{d\_\Delta V_t}} + \Delta T_{ox} \times S_{E,T_{d\_\Delta T_{ox}}} \quad (3)$$

In our approach, possible non-ideal effects at each block are considered, not the VCO block only. However, constant sensitivity values may not sufficiently model the CP and VCO behavior under process variation. Therefore, the modified sensitivity analysis method considering the actual circuit characteristics is developed to model their variation responses with acceptable accuracy, as explained in Section 3.

2.2. PFD & Frequency Divider

These two circuits are often treated as digital blocks. Timing information, such as delay and transition time, is the major concern of PLL designers. Those characteristic parameters are also the primary sources of non-ideal effects, such as PFD dead zone, and contribute to PLL performance. In our approach, timing parameters and their process variation sensitivities can be easily measured from the simulation results in the characterization mode. Then, flexible adjustments like (3) can be easily made without extra efforts to build accurate behavioral models.

3. MODIFIED S_E ANALYSIS FOR CP&VCO

3.1. CP & LF

In our behavioral model, the transfer function of these two blocks are modeled together such that the information of current mismatch (I_{up}-I_{dn}) and charge/discharge current (I_{up}/ I_{dn}) of CP can be observed by the extracting pattern in Figure 2. The equivalent switch on/off time is also extracted in our work due to its effects in locking phase.

$$ratio(\Delta V_t) = \frac{I_D'}{I_D} \cong \frac{[V_{GS} - (V_t + \Delta V_t)]^2}{(V_{GS} - V_t)^2} = \left(1 - \frac{\Delta V_t}{(V_{GS} - V_t)}\right)^2 = \left(1 - \frac{\Delta V_t}{k}\right)^2 \cong \frac{I_{CP}'}{I_{CP}} \quad (4)$$

In order to reflect the process variation effects, a variable ***ratio*** is defined as the changed current (I_{CP}') ratio to the nominal current (I_{CP}). Using the traditional S_E analysis, ***ratio*** can be expressed as a pure linear function like (3). However, actual current variation ratio may not have a linear relationship with threshold voltage variation. A single MOS saturation current (I_D) is used as an example to observe the relationship between current variation ratio and ΔV_t, as shown in (4). Since ***k*** is a constant value, the ***ratio*** is a 2nd order function of ΔV_t. Therefore, considering the threshold voltage variation, this 2nd order form can be used as the modified sensitivity function instead of a linear function, which also requires only two simulation samples. Figure 3 shows the variation ratio of charge current under different ΔV_t. We compare the calculated results of traditional S_E and our modified S_E with HSPICE simulation. It shows that the results of our model are more similar to HSPICE simulations.

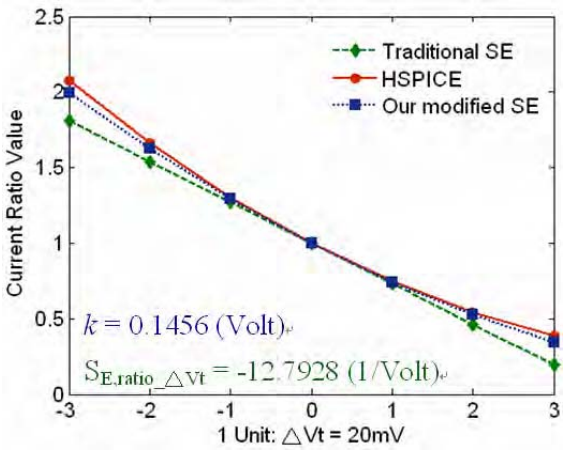

Figure 3. Current variation ratio under different ΔV_t

As to the other three device-level parameters (ΔW, ΔL, and ΔT_{ox}), linear sensitivity models are still accurate enough for modeling the information of current variation ratio. Therefore, the ***ratio*** under such four device parameter variations can be expressed as (5). The 2nd order term indeed makes our model more accurate than traditional sensitivity analysis without extra regression cost, as shown in the experimental results.

$$\frac{I_{CP}'}{I_{CP}} \cong ratio(\Delta W, \Delta L, \Delta T_{ox}, \Delta V_t) = \frac{\Delta W \times S_{E,I_{CP\_\Delta W}} + \Delta L \times S_{E,I_{CP\_\Delta L}} + \Delta T_{ox} \times S_{E,I_{CP\_\Delta T_{ox}}}}{I_{CP}} + \left(1 - \frac{\Delta V_t}{0.1456}\right)^2 \quad (5)$$

3.2. VCO

We adopt the linear VCO model to simplify modeling complexity because the linear VCO model predicts more than 90% of real VCO characteristics, especially in the operating range, according to a related study [8]. Then, we use actual simulation results of a ring oscillator to explain the process variation effects. Considering different ΔL for an example, the relationship between oscillator input voltage (V_{ctrl}) and output frequency (f_{out}) obtained from HSPICE simulation, is shown in Figure 4. The unused part is truncated in order to focus on VCO responses in the normal operating region (0.8V ~ 1.2V). Curves are quite linear in Figure 4 except for the transition positions. Therefore, using linear VCO model will not incur too many errors.

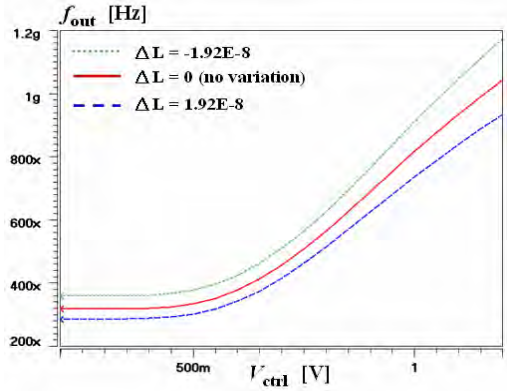

Figure 4. f_{out} -V_{ctrl} vs. ΔL

Traditional sensitivity analysis for such a linear VCO model uses a constant value to represent frequency sensitivity to ΔL. In other words, frequency change should be the same when ΔL value is the same. However, the distance between any two curves is not a unique value as shown in Figure 4, implying that the frequency change under a given fixed channel length variation is not a constant.

Another experiment is conducted to observe this problem and to understand the effects of V_{ctrl} values. Three different V_{ctrl} values, 0V, 0.8V and 1.2V, are arbitrarily chosen and frequency sensitivity $S_{E,f\_\Delta L}$ is measured under different V_{ctrl} values. The experimental results displayed in Figure 5 show that the frequency sensitivity (slope) are quite different in different V_{ctrl} values. Therefore, our modified frequency sensitivity is modeled as a function of both process variation and V_{ctrl} value in our approach. Waveforms in Figure 4 can be translated into piece-wise linear curves shown in Figure 6 when we adopt linear VCO modeling approach. Then, we model the frequency sensitivity as a function of three variables instead, which are V_{ctrl}, $S_{E,f\min\_\Delta L}$ and $S_{E,f\max\_\Delta L}$ defined in (6). As illustrated in Figure 6, we can see that different sensitivity for f_{min} and f_{max} can give different frequency sensitivity at different V_{ctrl} value according to (7) and (8). Then, the other sensitivity values ($S_{E,f\_\Delta W}$, $S_{E,f\_\Delta Vt}$, $S_{E,f\_\Delta Tox}$) can be obtained by the same way. Our modified S_E analysis including the V_{ctrl} effects still uses simple linear models, which allow us to flexibly adjust the frequency sensitivity in a simple way. In the following experiments, we will demonstrate that our VCO model can still have accurate responses under process variation using the modified sensitivity analysis.

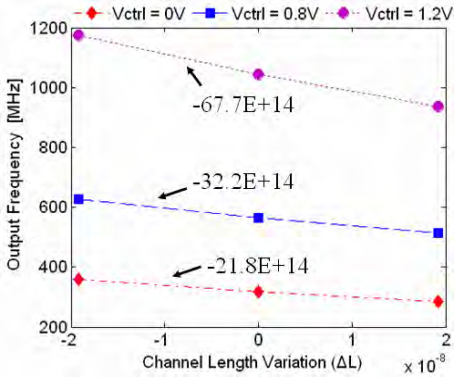

Figure 5. $S_{E,f\_\Delta L}$ values vs. V_{ctrl}

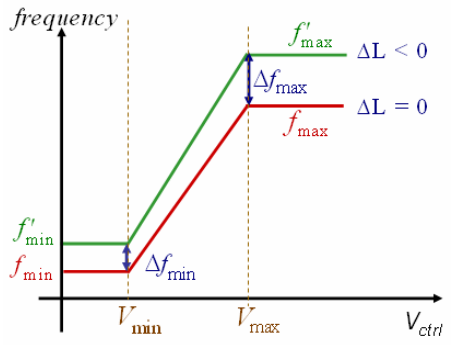

Figure 6. Developed linear VCO model with V_{ctrl} effects

$$S_{E,f_{\min}\_\Delta L} = \frac{\Delta f_{\min}}{\Delta L} \qquad S_{E,f_{\max}\_\Delta L} = \frac{\Delta f_{\max}}{\Delta L} \tag{6}$$

$$slope_{\Delta L} = \frac{\Delta L \times (S_{E,f_{\max}\_\Delta L} - S_{E,f_{\min}\_\Delta L})}{V_{\max} - V_{\min}} \tag{7}$$

$$S_{E,f\_\Delta L}(\Delta L, V_{ctrl}) = \begin{cases} S_{E,f_{\min}\_\Delta L} & ,if\ V_{ctrl}(t) \le V_{\min} \\ S_{E,f_{\min}\_\Delta L} + [V_{ctrl}(t) - V_{\min}] \times slope_{\Delta L} & ,if\ V_{\min} < V_{ctrl}(t) < V_{\max} \\ S_{E,f_{\max}\_\Delta L} & ,if\ V_{ctrl}(t) \ge V_{\max} \end{cases} \tag{8}$$

4. EXPERIMENTAL RESULTS

We use a charge-pump PLL circuit implemented in TSMC 0.18μm process to perform some experiments. The PLL behavioral model is built up by Verilog-A language and simulated in Cadence's Virtuoso environment (Analog Artist). Referring to the statistical models of transistor parameters in TSMC, we perform 4+1 runs parameter extraction developed in Section 2 to find out our modified sensitivity values for these 4 process parameters, which are W, L, V_t, and T_{ox}. Then we can adjust the behavioral parameters according to the modified S_E values when every device variation values are randomly generated in the MC analysis.

For comparisons, we perform the traditional sensitivity analysis and 1st order RSM to model the behavioral parameters under process variation. The required extraction samples of traditional S_E method is the same as in our approach, but the number of training samples of 1st order RSM is at least 4 times to keep the fitting accuracy according to the conclusions in [5]. Then, the estimated circuit parameters from these three approaches are used in a 100-run BMCS analysis using our accurate behavioral model to analyze the statistical results under process variation.

We also perform 100-run traditional HSPICE MC analysis for this PLL circuit. The same device variation values are used in HSPICE and our BMCS approach to compare the analysis accuracy in TABLE I. The lock voltage (V_{lock}) and the lock time (T_{lock}) are selected as the system characteristics of PLL circuits for comparisons. In our experiments, T_{lock} is defined as the time when V_{ctrl} is within 3% of V_{lock}. As to the most concern of PLL designers, peak-to-peak jitter ($Jitter_{p\text{-}p}$), the worst value under MC analysis is also shown in TABLE I. The scatter plots in Figure 7 and Figure 8 also demonstrate that our simple models can still retain good accuracy to estimate the performance shift under process variation.

Referring to the previous work [4] using 2nd order RSM for their behavioral parameters under process variation, we can improve the correlation coefficient value of T_{lock} from 0.888 [4] to 0.991 using our accurate PLL model. The results are also much better than the pure RSM-based approach (0.858) in [4]. It shows that a behavioral model with accurate responses to process variation is very important. If the behavioral model is not accurate enough, the statistical results would not be accurate even if use the high-order regression equations for device variations.

In the TABLE I, our accurate behavioral model has similar statistical results to HSPICE simulation, but significantly reduces the simulation time of Monte Carlo analysis from several weeks to several hours. Using our BMCS approach, the correlation coefficient (corr. coe.) values of these two system performance, V_{lock} and T_{lock}, are very close to 1 (>0.99), which can demonstrate the identical variation direction with HSPICE MC simulations. The standard deviation (St. Dev.), which is expressed as the percentage of nominal value, shows the statistical dispersion of system performance under such device variation. Our modified S_E method considering actual circuit properties also has more accurate results than tradition S_E approach with same extraction time. Compared to the results of RSM-based models shown in the last column of TABLE I, our approach has similar accuracy but reduce the regression cost significantly. It shows that such a simple model for behavioral parameters under process variation is accurate enough to perform BMCS analysis.

TABLE 1
COMPARISON RESULTS OF MONTE CARLO ANALYSIS

		HSPICE MCS	**Modified S_E +BMCS**	Trad. S_E +BMCS	1st RSM +BMCS
V_{lock} (V)	Nominal	0.9935	**0.9930**	0.9930	0.9920
	St. Dev.	3.45%	**3.62%**	1.56%	3.67%
	corr. coe.	1	**0.999**	0.998	0.999
T_{lock} (μs)	Nominal	3.342	**3.341**	3.341	3.361
	St. Dev.	17.25%	**17.21%**	15.25%	17.03%
	corr. coe.	1	**0.991**	0.984	0.990
$Jitter_{p-p}$ (ps)	Nominal	13.2	**13.4**	13.4	13.5
	Worst	17.0	**17.4**	15.4	19.6
$T_{extraction}$ (hours)		N/A	**(4+1)×1.71 = 8.55**		34.20
$T_{simulation}$ (hours)		598.54	**3.50**	2.93	2.95

5. CONCLUSIONS

In this paper, a Behavioral Monte Carlo Simulation (BMCS) approach to analyze PLL designs under process variation is developed by using a bottom-up modeling approach with efficient extraction process. We also develop the modified strategies for traditional sensitivity analysis to improve the accuracy with same extraction cost. Such simple methods can reflect the process variation effects with acceptable accuracy and save considerable simulation time for complicated curve fitting. Then, we can use this accurate behavioral model to perform fast MC analysis and provide similar variation trend (correlation coefficient > 0.99) and statistical distributions (according to standard deviation values) to the results of transistor-level simulation. As shown in the experimental results, we can reduce the simulation time of HSPICE MC analysis from several weeks to several hours and still retain high accuracy.

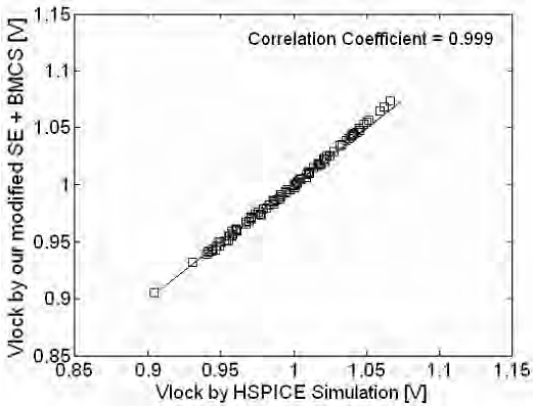

Figure 7. Scatter plot of V_{lock}

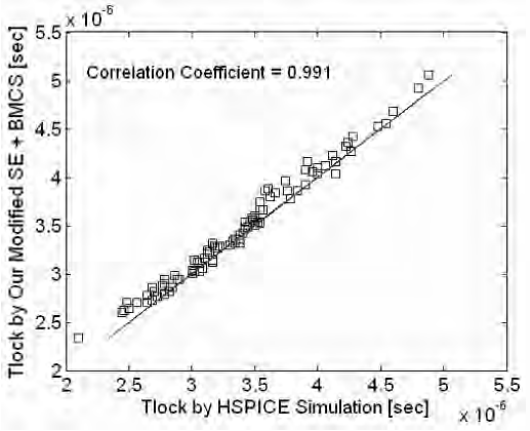

Figure 8. Scatter plot of T_{lock}

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