Model to Hardware Matching for nm Scale Technologies

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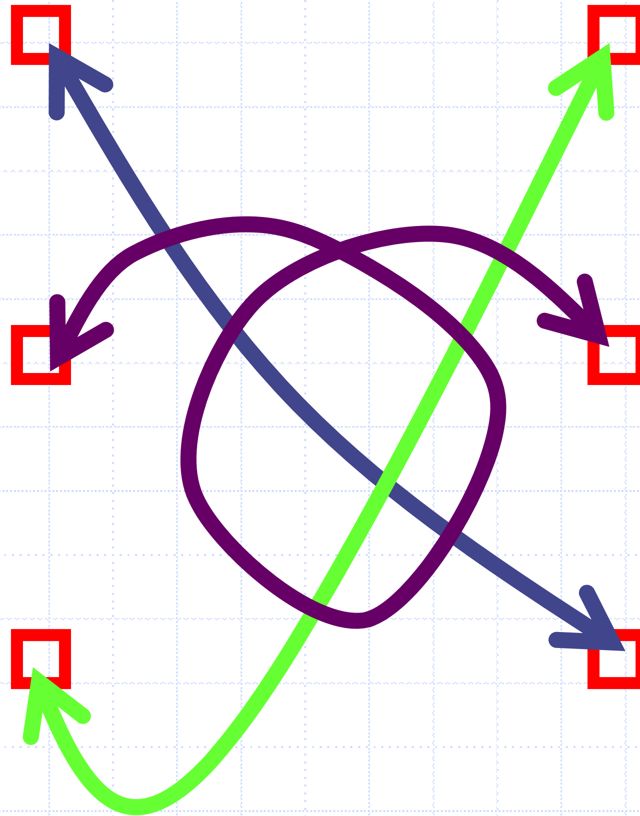
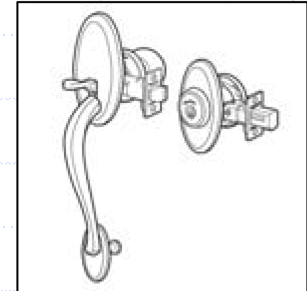
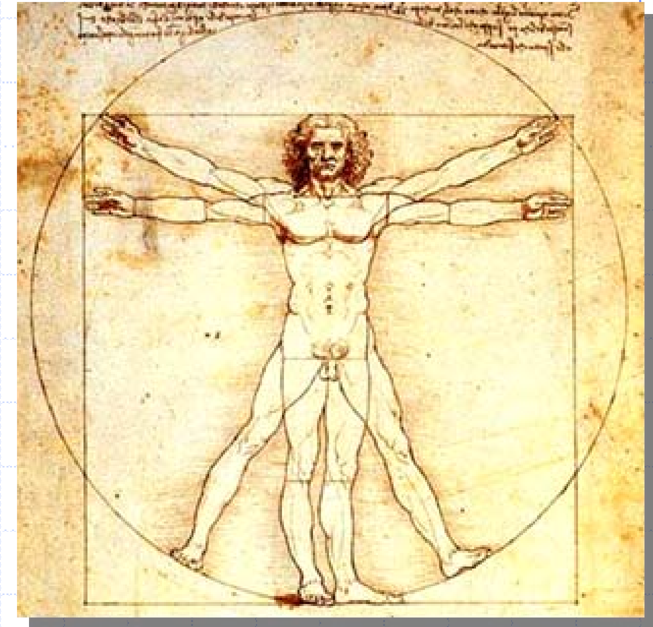
Model to Hardware Matching?





DFM Job Description

- What is the real problem?
- Imagine 10^9 people being asked to form a human chain.
  - Maybe the population of Europe.
  - With height and width of each person varying by ~50%.
  - Maybe after some beer…
- This is what we ask 1B highly variable MOSFETs to do!
  - And we want to predict how long the chain is going to be, and how much food and beer is required etc…
- And… we cannot prototype! We use predictive models, and need them to match reality.

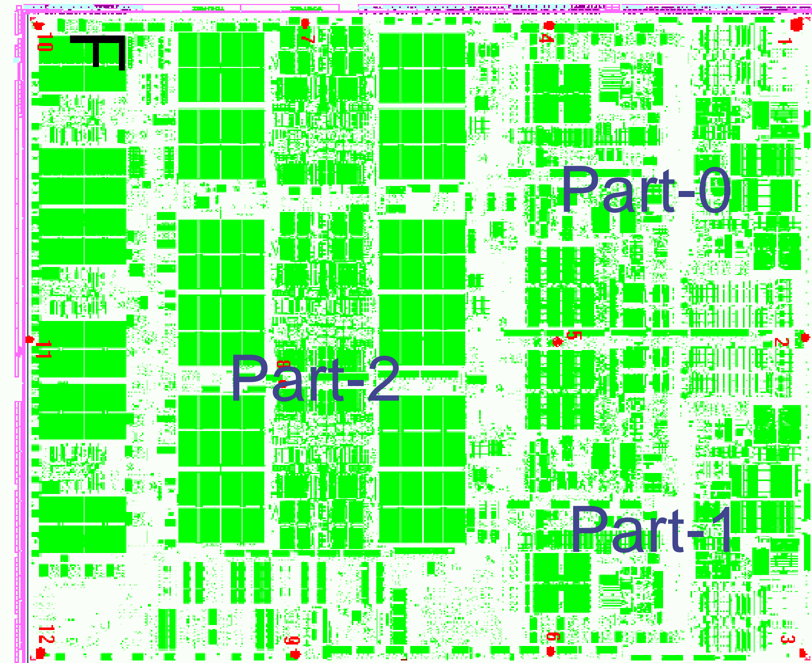


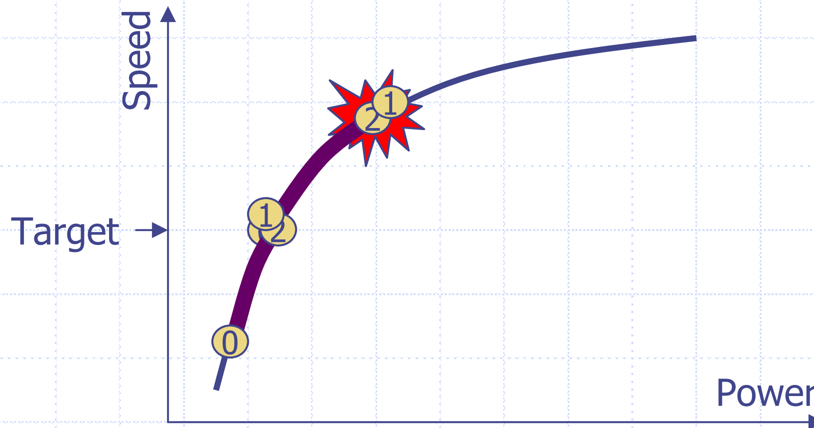
Realities and Motivation

- The IC industry is built on a foundation of models for performance, power, yield, cost…
- When models do not predict the correct outcome, we lose money.
- Technology complexity near the end of scaling is exacerbating this “prediction gap”.
- Investments in technology modeling and understanding are needed!

An Example from IBM

- One part of a design was found to be ~15% slower than other parts.
- Models predict all parts of design are identical.
- Model/hardware mismatch!
  - Slower block limits F_{MAX}.
  - Faster block wastes power.

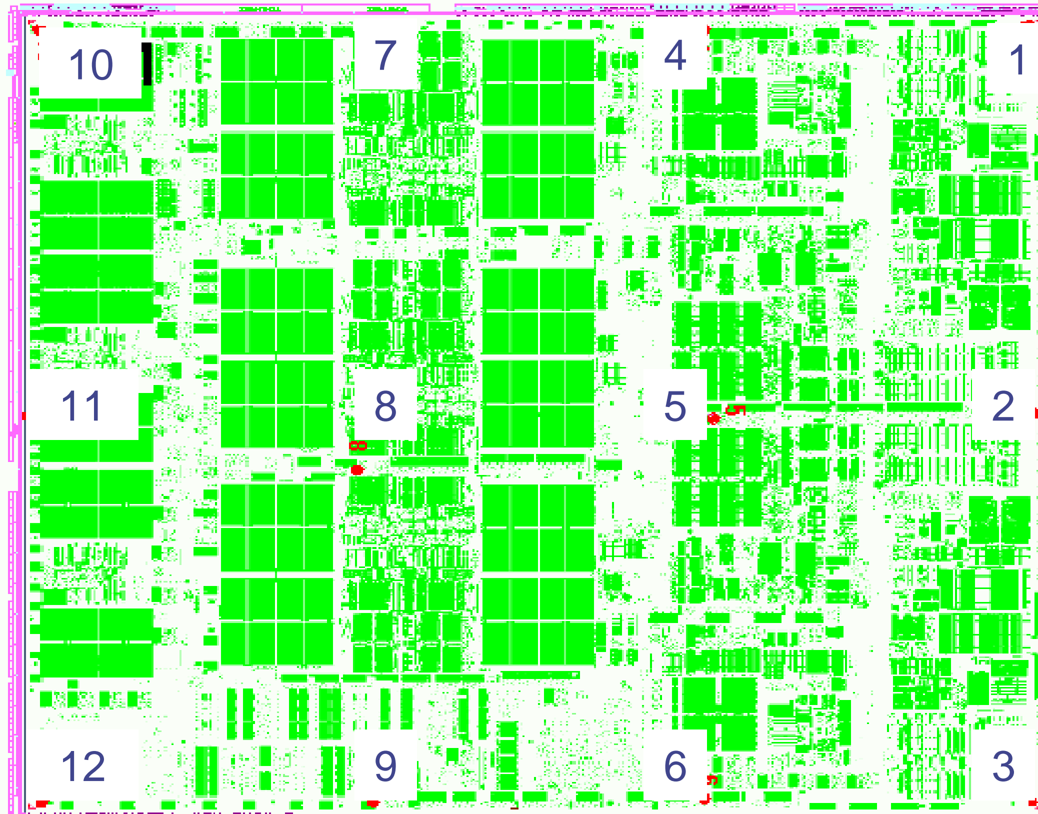




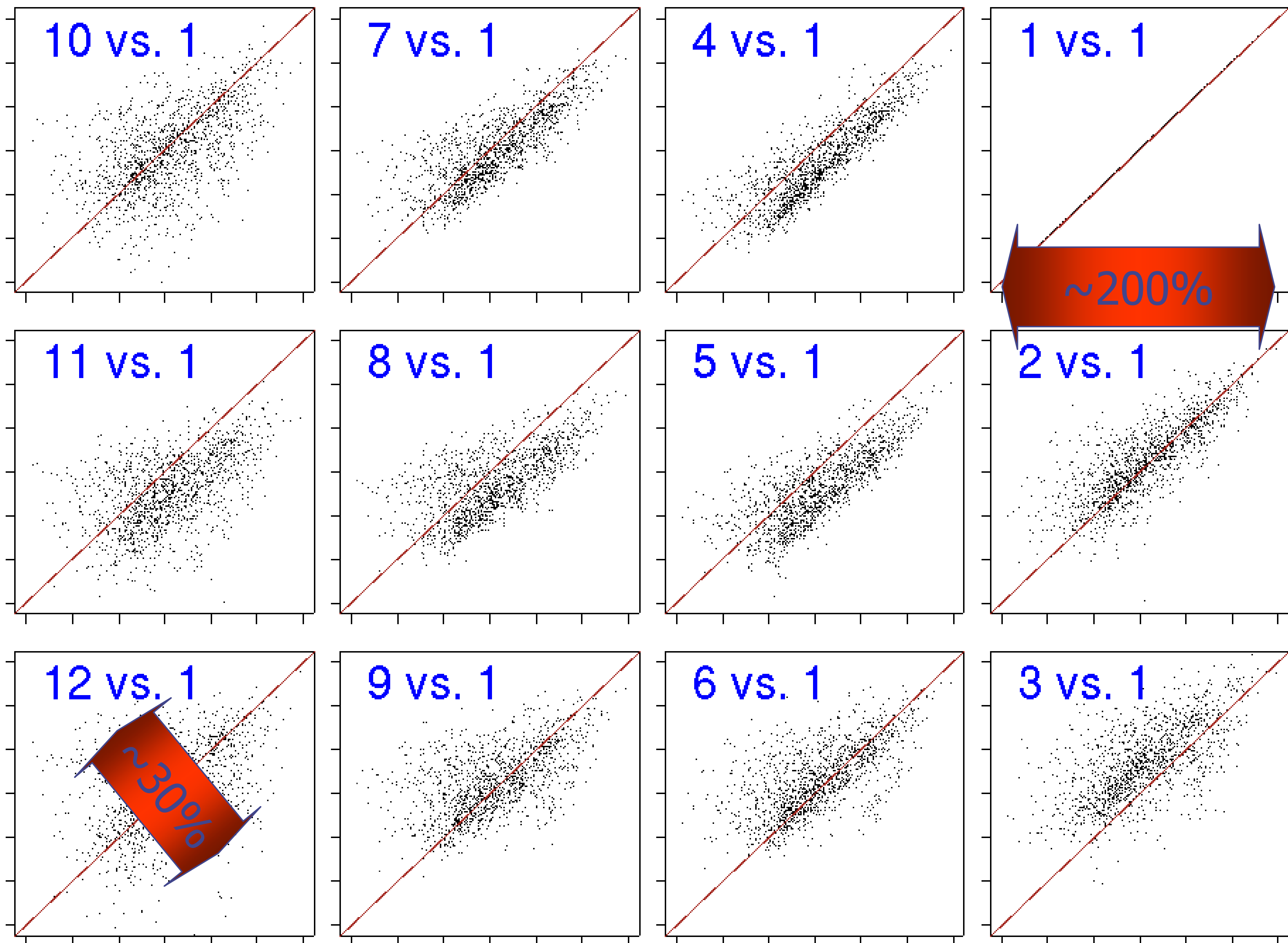
Case study performed by Anne E. Gattiker

Model to Hardware Support

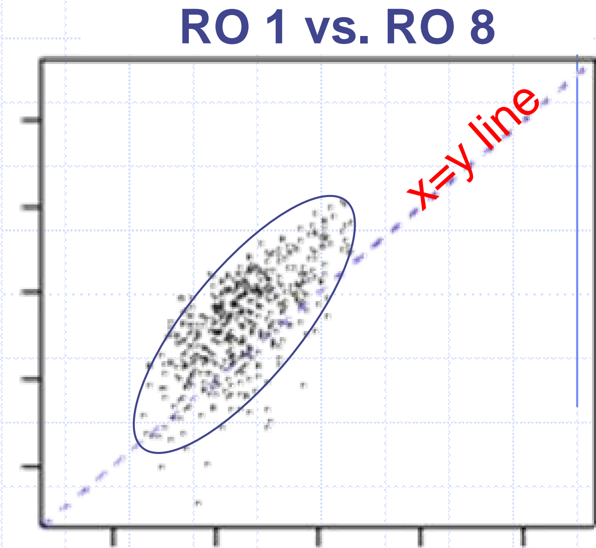
- Chip has 12 ring oscillators distributed across the die, and individually measurable.



Chip map with Ring Oscillator locations


10 vs. 1
7 vs. 1
4 vs. 1
1 vs. 1
~200%
11 vs. 1
8 vs. 1
5 vs. 1
2 vs. 1
12 vs. 1
~30%
9 vs. 1
6 vs. 1
3 vs. 1

Systematic Offsets



- Strong correlations between:
  - Part-0 and RO 1.
  - Part-2 and RO 8.
- Systematic offset between the ROs.
  - Even though the two ROs are identical!

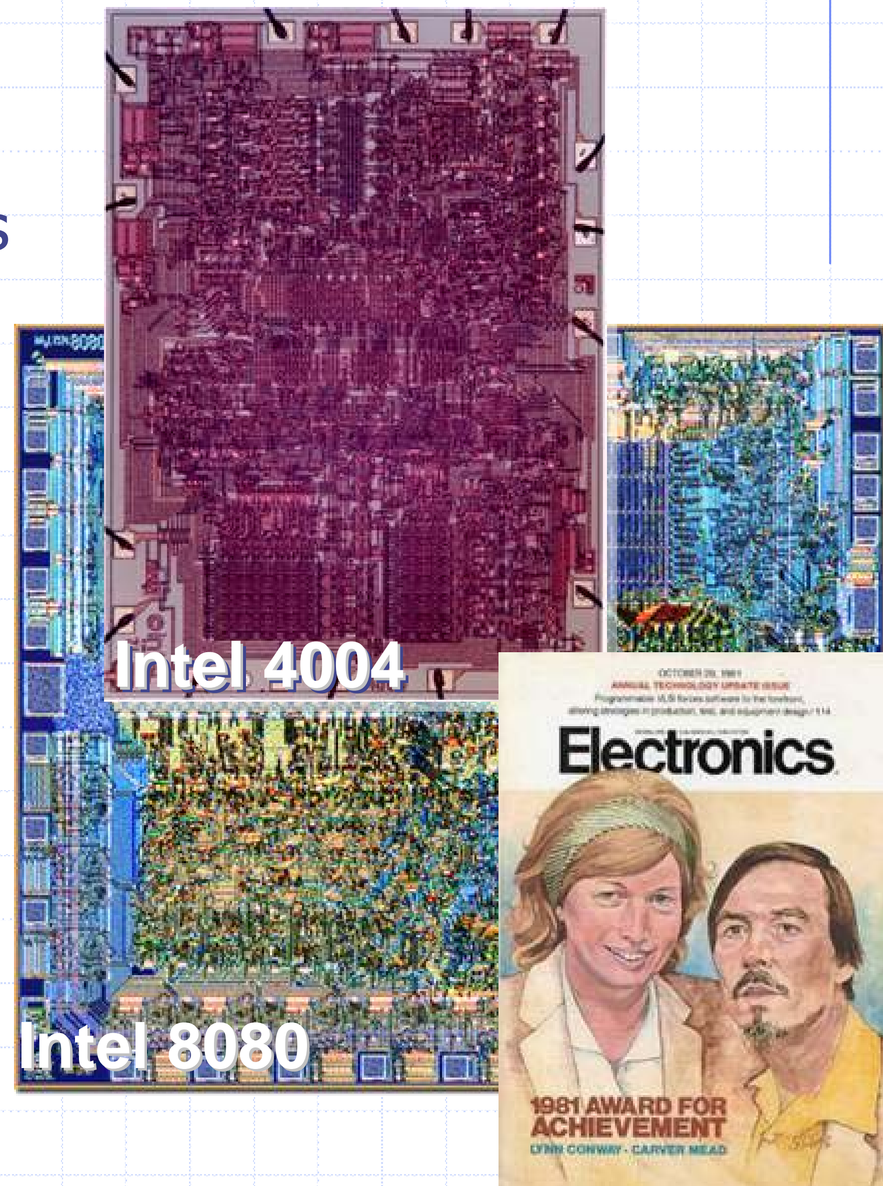
Conclusion:

- Within-die variability caused systematic spatial mismatch (mean shift + rotation).
- Magnitude of mismatch large and has –ve impact on design.

Why? (Historical Perspective)

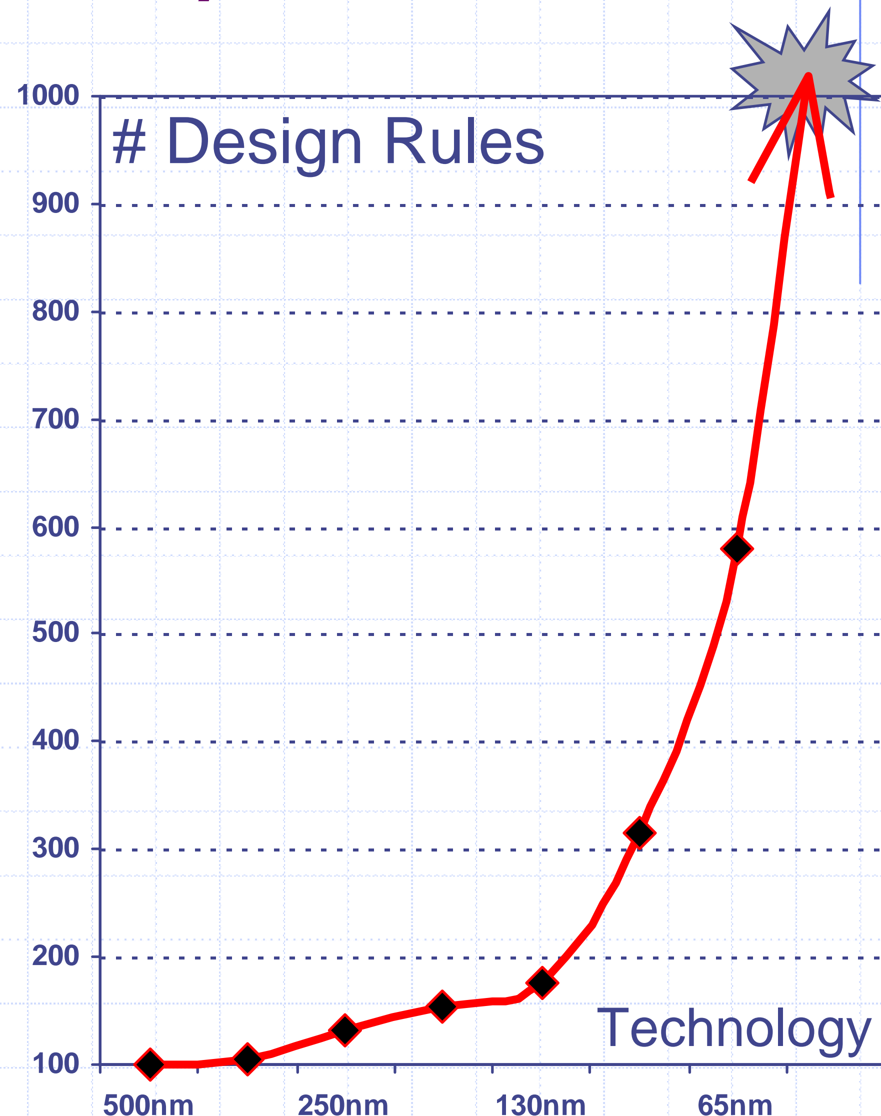
- In the beginning, design was hard and only few were able to do it well. This was the age of "chip engineering".

- But with scaling-driven performance, it became possible to abstract design to a few simple rules. This was the age of "chip computer science"!



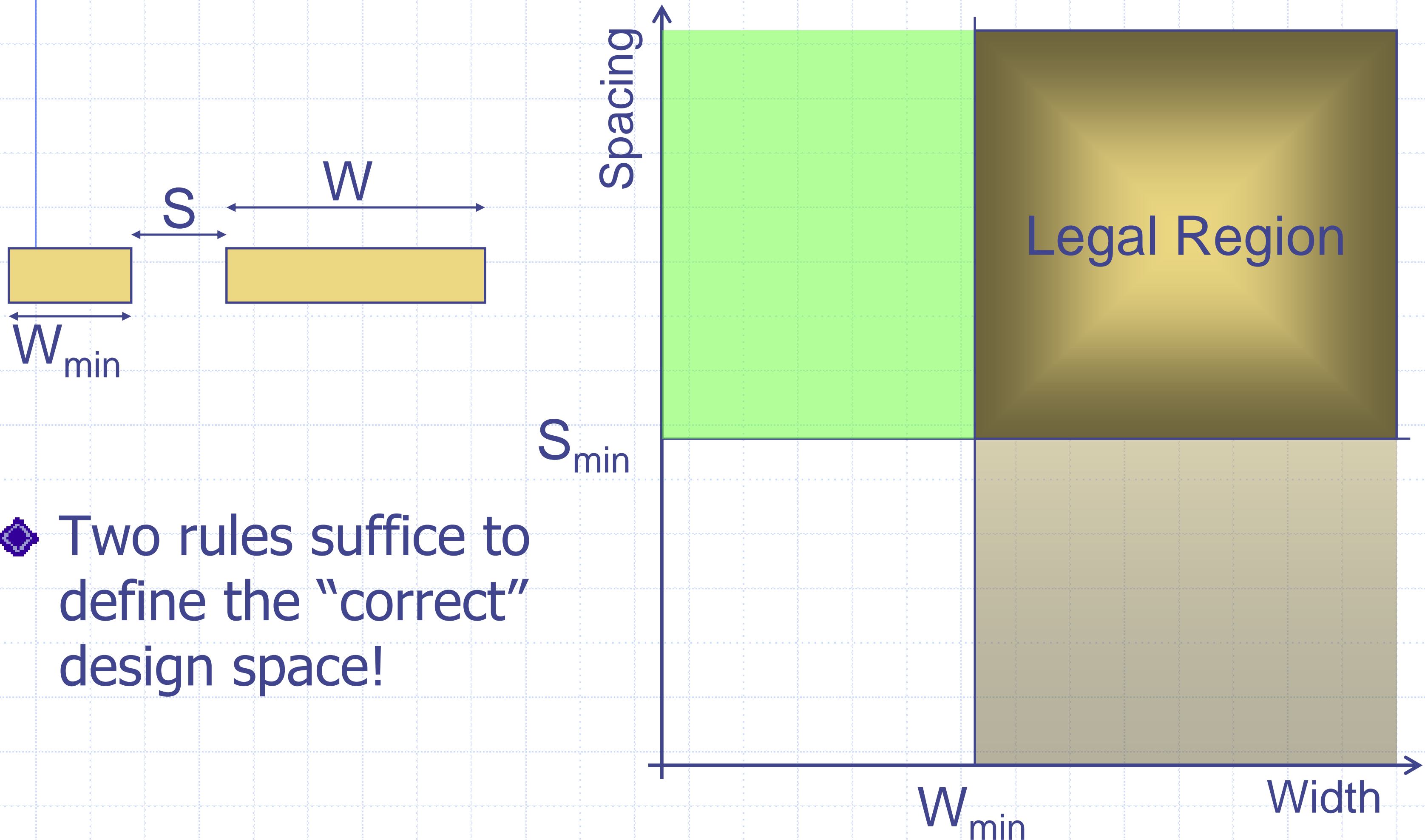
Technology Complexity

- Technology has become so complex that it is not well represented by "rules".
- Design / Technology interface information bandwidth needs are skyrocketing!
- Expressing complex non-linear realities via rules is becoming difficult.



Technology Rules (History)

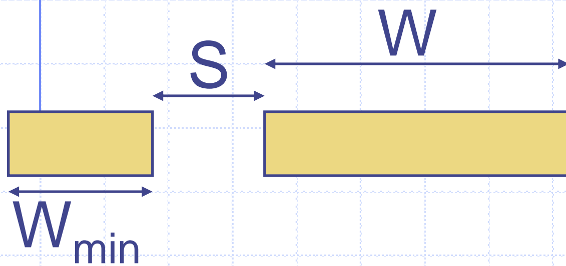
- Example: wire spacing…



- Two rules suffice to define the “correct” design space!

Technology Rule Explosion

- Impact of CMP, Dishing, Erosion as well as lithography...



- Four (or more) rules for the same situation in order to accommodate technology complexity!

What Does This Change?

- Transistor performance is being determined by new physics and complex interactions.
  - Large variety in behaviors.
  - Systematic & Random variability increasing.
- Devices used for technology characterization becoming less typical…
  - Number of variants is exploding.
  - Ability to bound all behaviors is compromised.

- Result: model / hardware mismatch.
  - Gap in our understanding of technology is relatively large and getting larger!

Where Does This Put Us?

- Our lack of understanding of technology is endangering the way we do design.
- The “contract” between manufacturing and design can no longer be just BSIM+DRC.
- These changes will have a dramatic impact on CAD and on the Foundry business.
  - More than just more OPC.
- Much of what we observe is being driven by variability…

Variability vs. Uncertainty

- Variability: known quantitative relationship to a source (readily modeled and simulated) – **systematic**!
  - Designer has option to *null* out impact.
  - Example: power delivery (package + grid) noise.
- Uncertainty: sources unknown, or model too difficult/costly to generate or simulate – **random**!
  - Usually treated by some type of worst-case analysis.
  - Example: ΔV_{TH} within die variation.

- Lack of modeling infrastructure and/or resources often transforms variability to uncertainty.
  - Example: power grid noise when not assessed!

Taxonomy

- In addition to systematic and random, we also differentiate variability according to source and distribution.

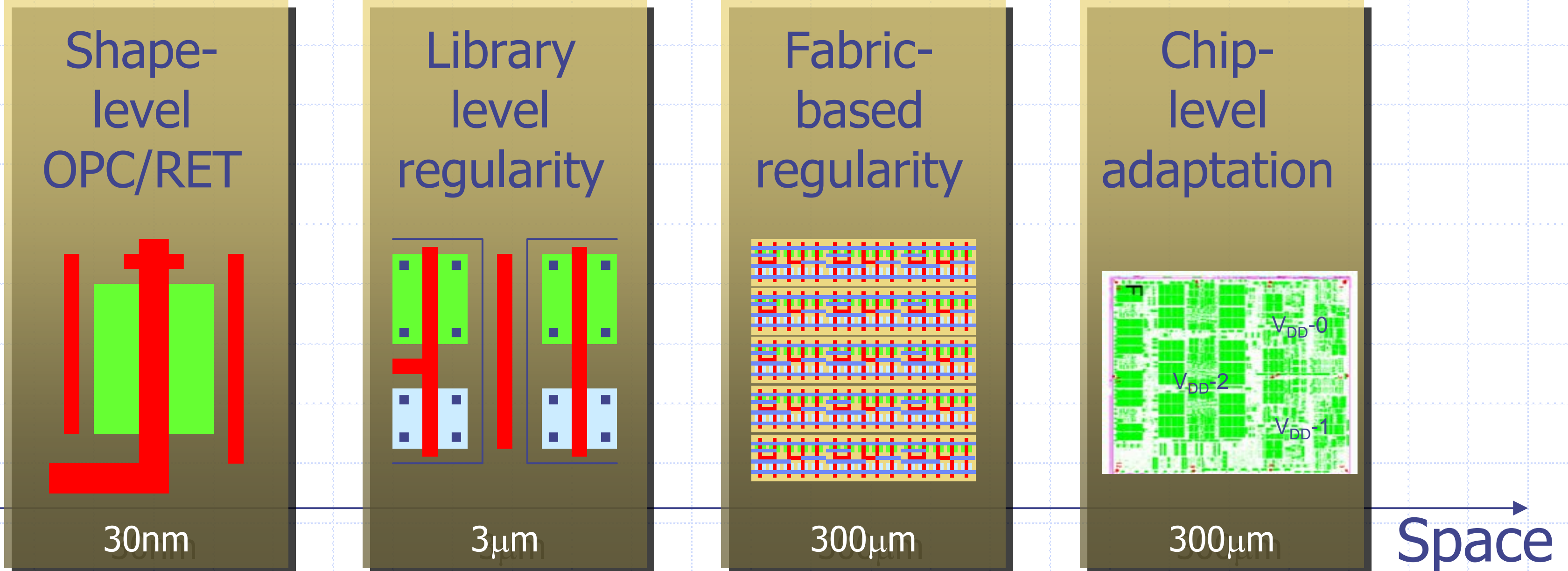
	Physical (time scale 10^{9} sec)	Environmental (time scale 10^{-9} sec)
Spatial	ΔL, $\Delta\mu$, ΔV_T	Noise coupling
Temporal	NBTI, Hot-ē, electro-migration	V_{DD}, T

Variability Interaction with Design

- Old view: Die to die variation dominant
  - Imposed upon design (constant regardless of design).
  - Predominantly random (e.g. wafer location effect).
  - Well modeled via worst-case files.
- New view: Within-die variation dominant
  - Co-generated between design & process (depend on details of the design).
  - Predominantly systematic.
  - Example: CMP-driven RC variation.

Response to Variability

- Responses to variability target different "spatial frequencies".
  - No one response is sufficient to tackle the full impact, but all responses require accurate estimates of magnitude and impact.



Variability Characterization

- A hard problem.
- Requires a large investment in test and characterization in order to understand all aspects of physical, environmental, systematic, random, etc…
- Also, many factors are design dependent.
  - So often generic test structures are not useful predictors (e.g. analog circuits)!
  - Number of variants exploding with “transistor weight” problem.

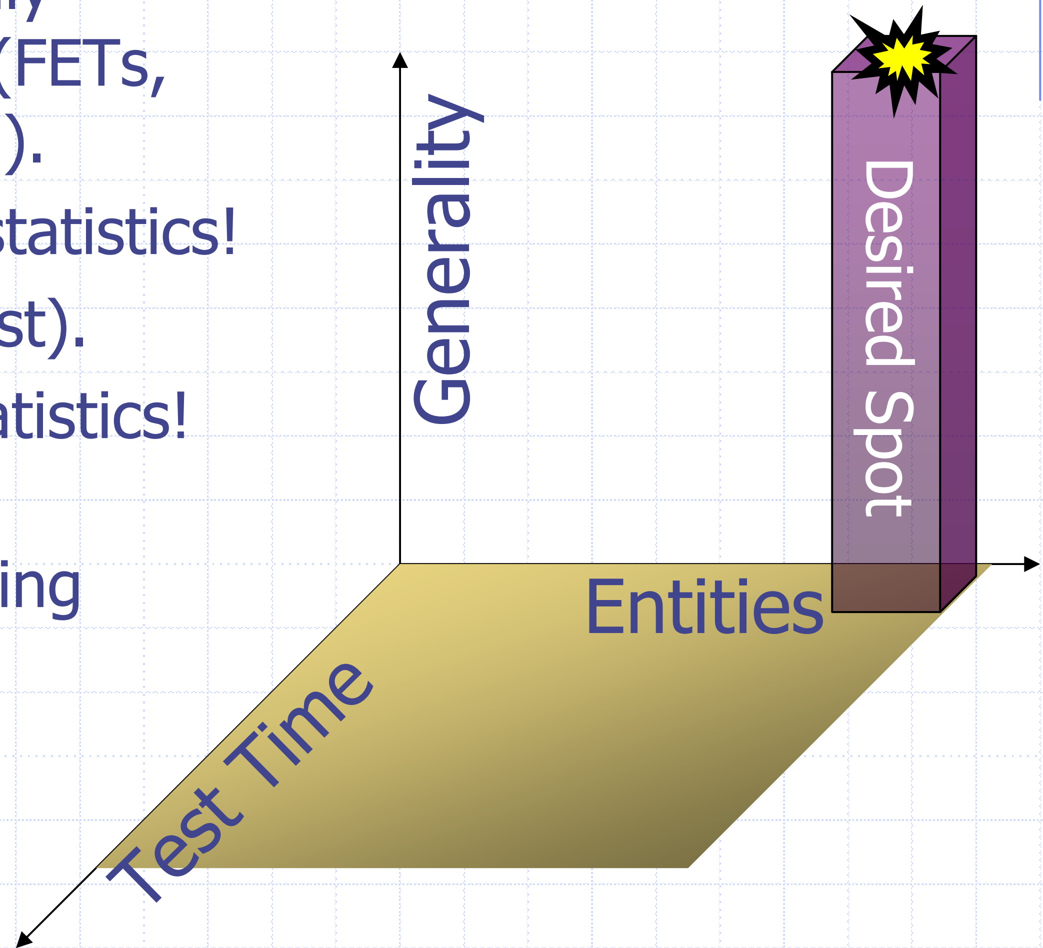
Silicon Information Density

- The efficiency with which we can perform precise variability characterization is going to become important.
  - No longer sufficient to do it once (technology bring up). Need to continually model and re-evaluate.
  - As EDA tools ramp up on understanding process, they will enable new methods of design optimization (e.g. during re-spins).
- Need vastly more information from scarce Si & test resources (i.e. more density)!

Test Structure Quality?

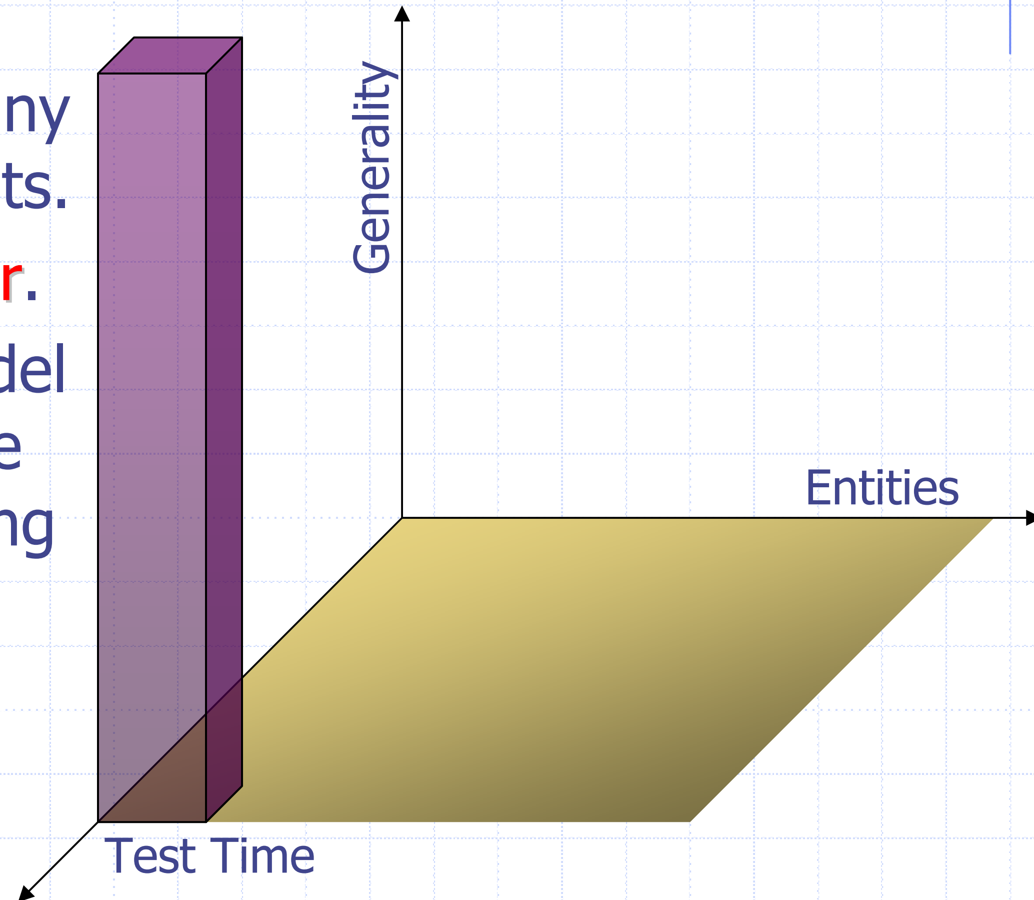
Three relative measures:

- Number of individually measurable entities (FETs, ring oscillators, etc…).
  - Many entities ⇒ statistics!
- Test time (or test cost).
  - Lower cost ⇒ statistics!
- Generality of result: suitability for predicting design outcome.
  - Modeling & EDA.



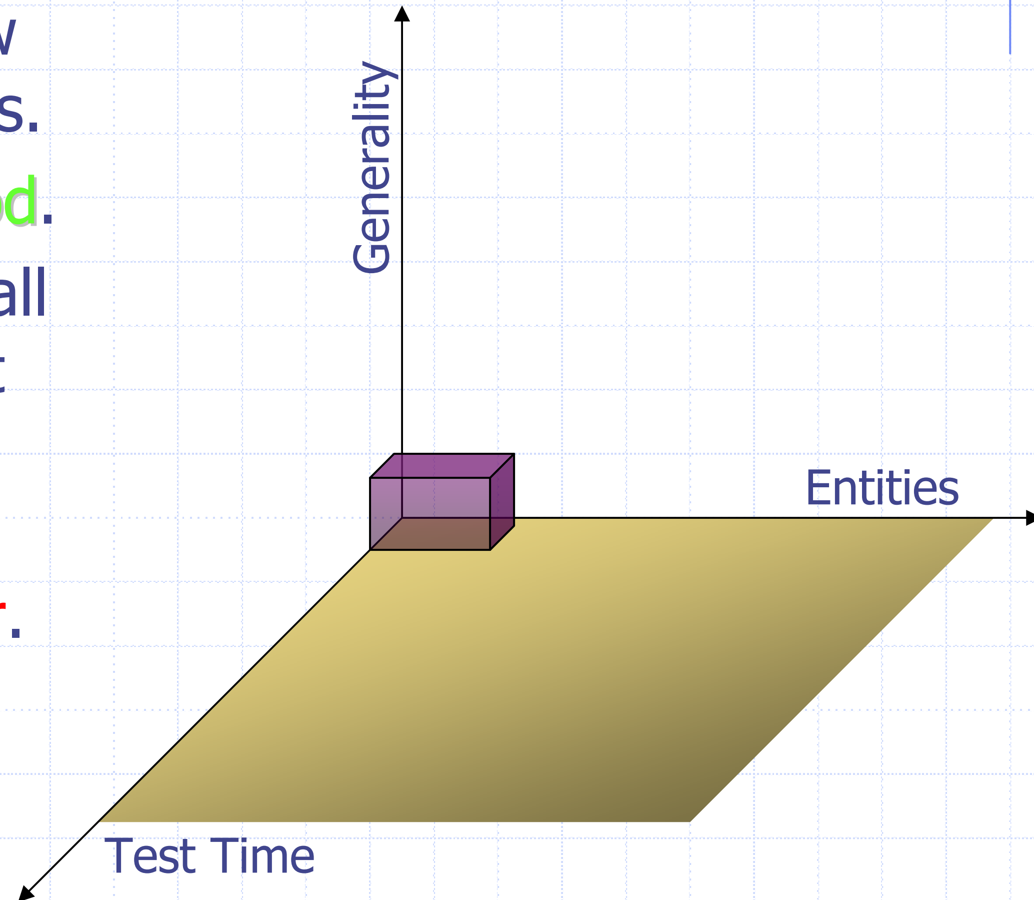
Example: Device Characterization

- Small number of devices with various dimensions.
  - Entities poor.
- Typically measure many current / voltage points.
  - Slow test time poor.
- Used to generate model parameters, which are the basis for everything else… (e.g. BSIM)
  - i.e. generality excellent.



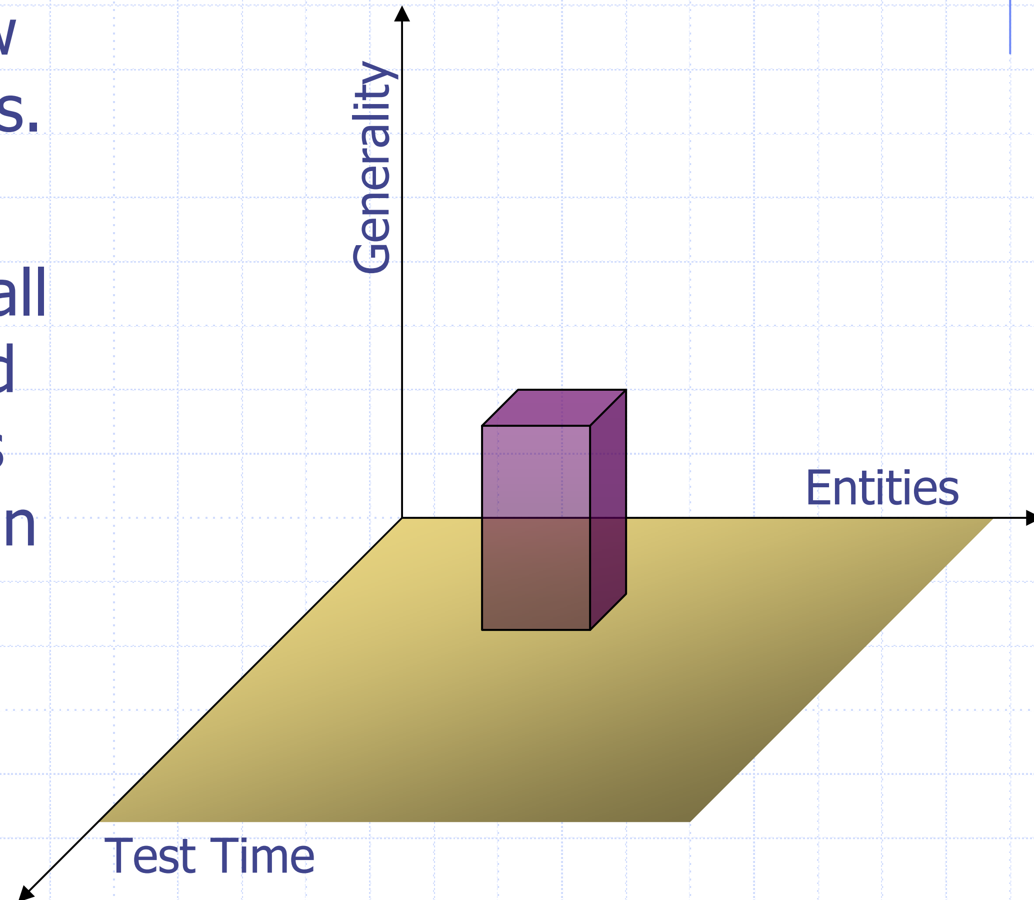
Example: Ring Oscillators (ROs)

- Few ROs per unit.
  - Entities poor.
- Typically measure few frequency & I_{DD} points.
  - Fast test time, good.
- Useful to assess overall health of process, but result is unique to RO structure.
  - i.e. generality poor.

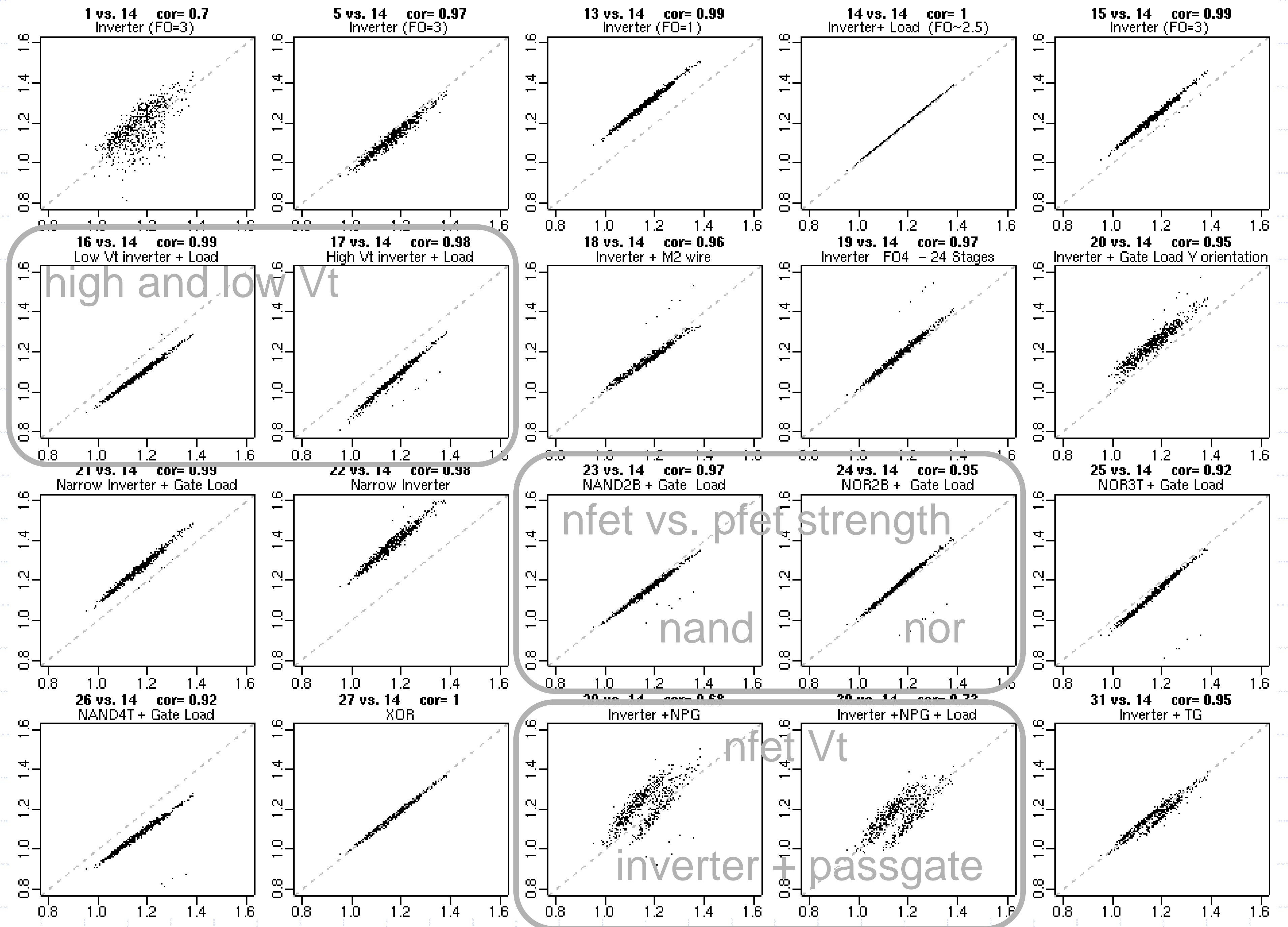


Example: RO Collections

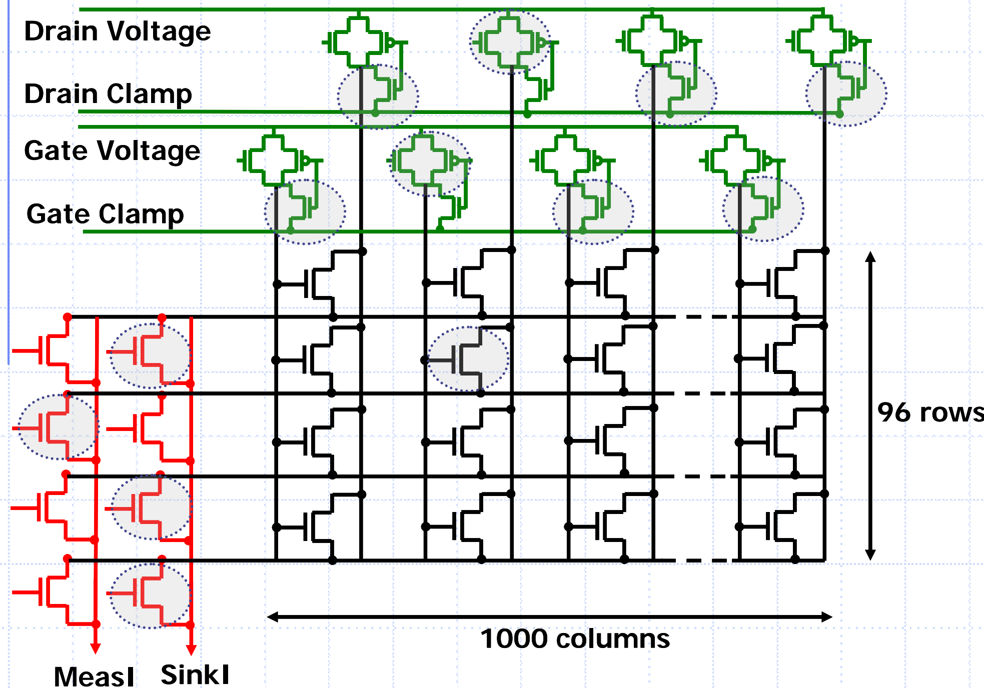
- Variety of ROs per unit.
  - Entities OK.
- Typically measure few frequency & I_{DD} points.
  - Test good.
- Useful to assess overall health of process, and since a variety of ROs are included, more can be learned.
  - i.e. generality OK.



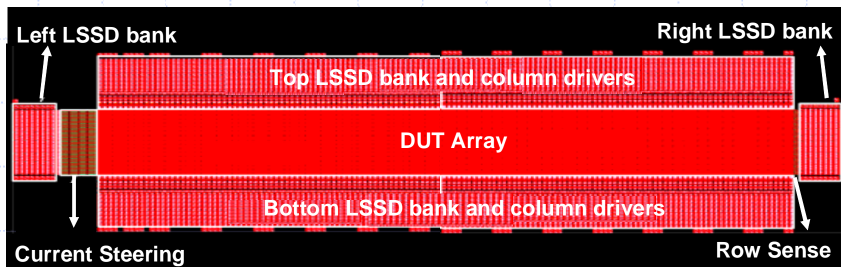
Canonical view: Varied ring types versus basic inverter ring

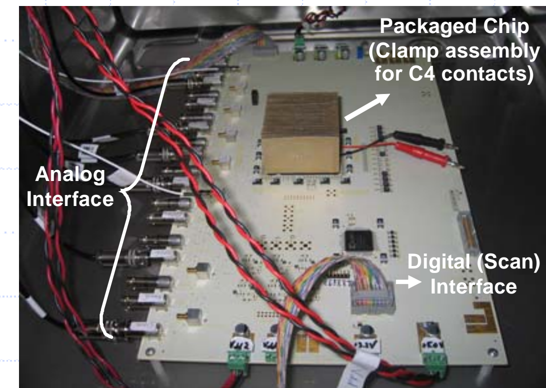


Advanced Modeling Structure

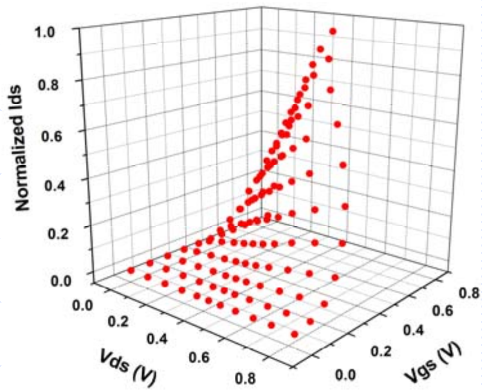


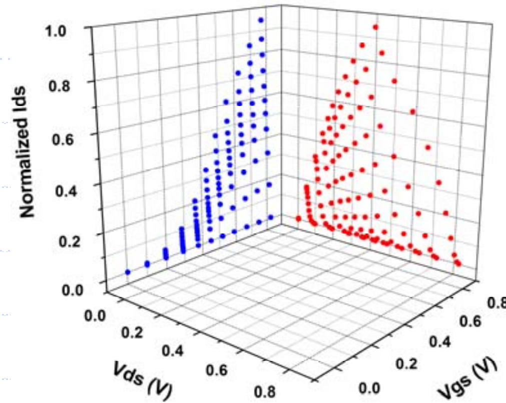
- SRAM sized devices arranged in an addressable manner.
- 96 rows, 1000 columns – 96,000 total devices.
- Complete I/V possible.

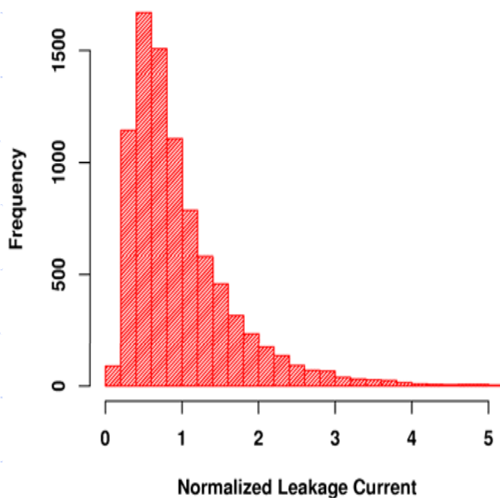


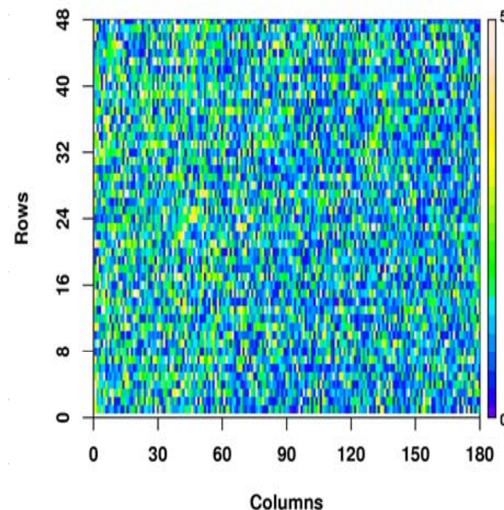


Experimental Results









- Measure full I/V range.
  - Extract parameter statistics through least-squares based parameter extraction.
- Leakage statistics.
  - Lognormal distribution.
  - No spatial correlation.
  - Systematic effects do not appear due to regular layout.
  - Random dopant effect is the dominant source of variation.

Siren Call: Variational Modeling

- Device models caught between the need to provide nominal and statistical accuracy.
- Nominal accuracy: ever more complex models with many fitting parameters and difficult-to-extract inter-dependencies.
  - Can you spell BSIM?
- Statistical accuracy: simple models that exhibit a physically significant and predictive correlation structure.
  - What is the right solution for this?

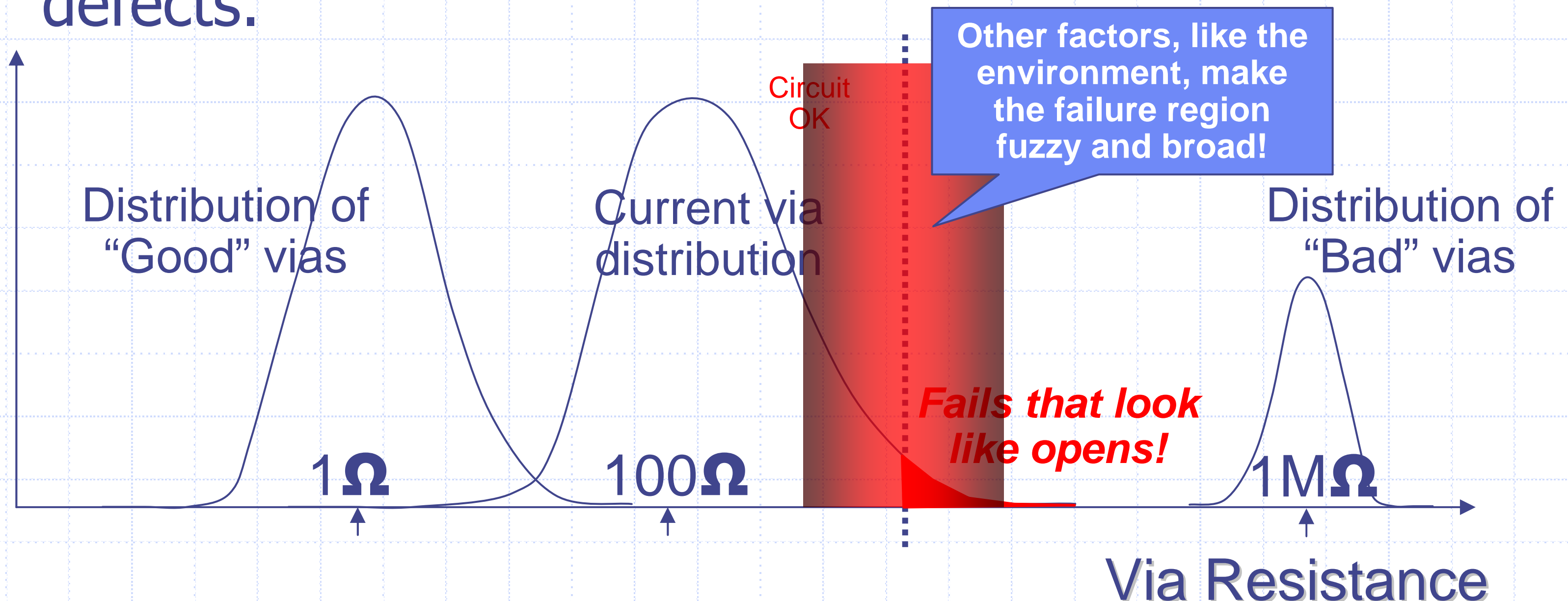
Linking Variability & Resilience

- Much current work is focused on the immediate and short term impact of variability.
  - Examples: statistical timing analysis, CMP-aware routing, new approaches for function-based OPC etc…

- But increasing variability will change the **character** of the impact it has on circuits.

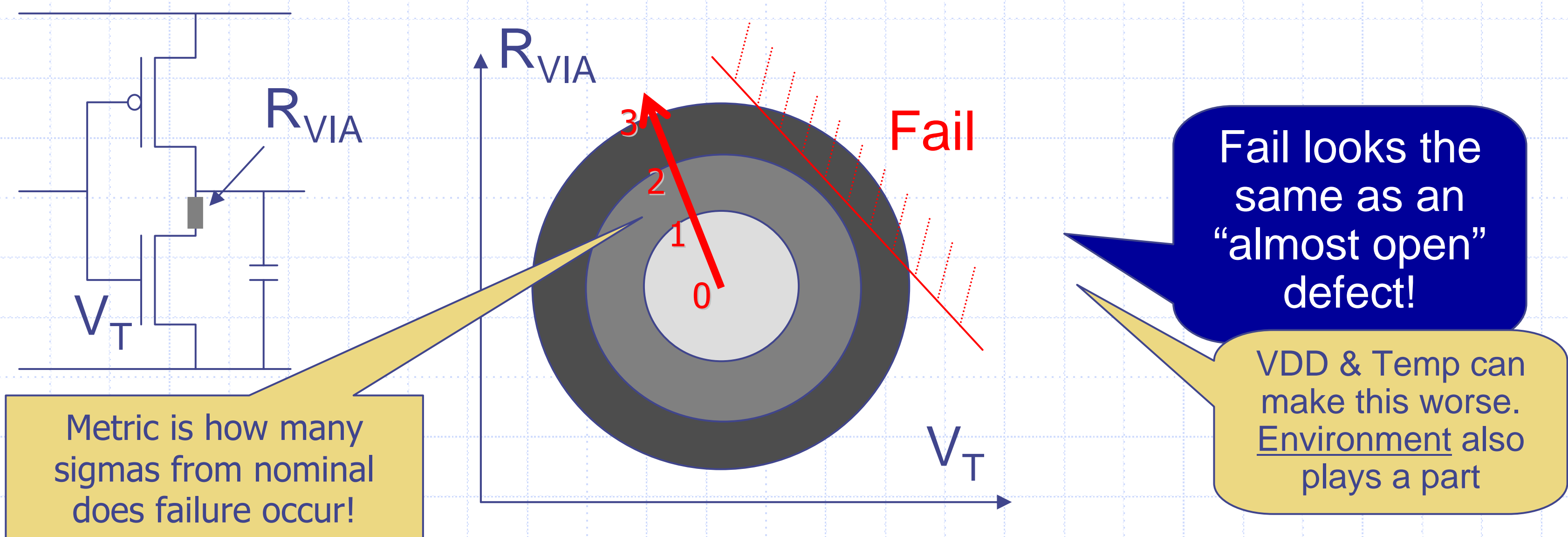
What changes with increased variability?

- Circuits can become permanently or intermittently defective.
- Failure dependence on operating environment makes test coverage very difficult to achieve.
- This can be viewed as the merger of failure modes due to structural (topological), and parametric (variability) defects.

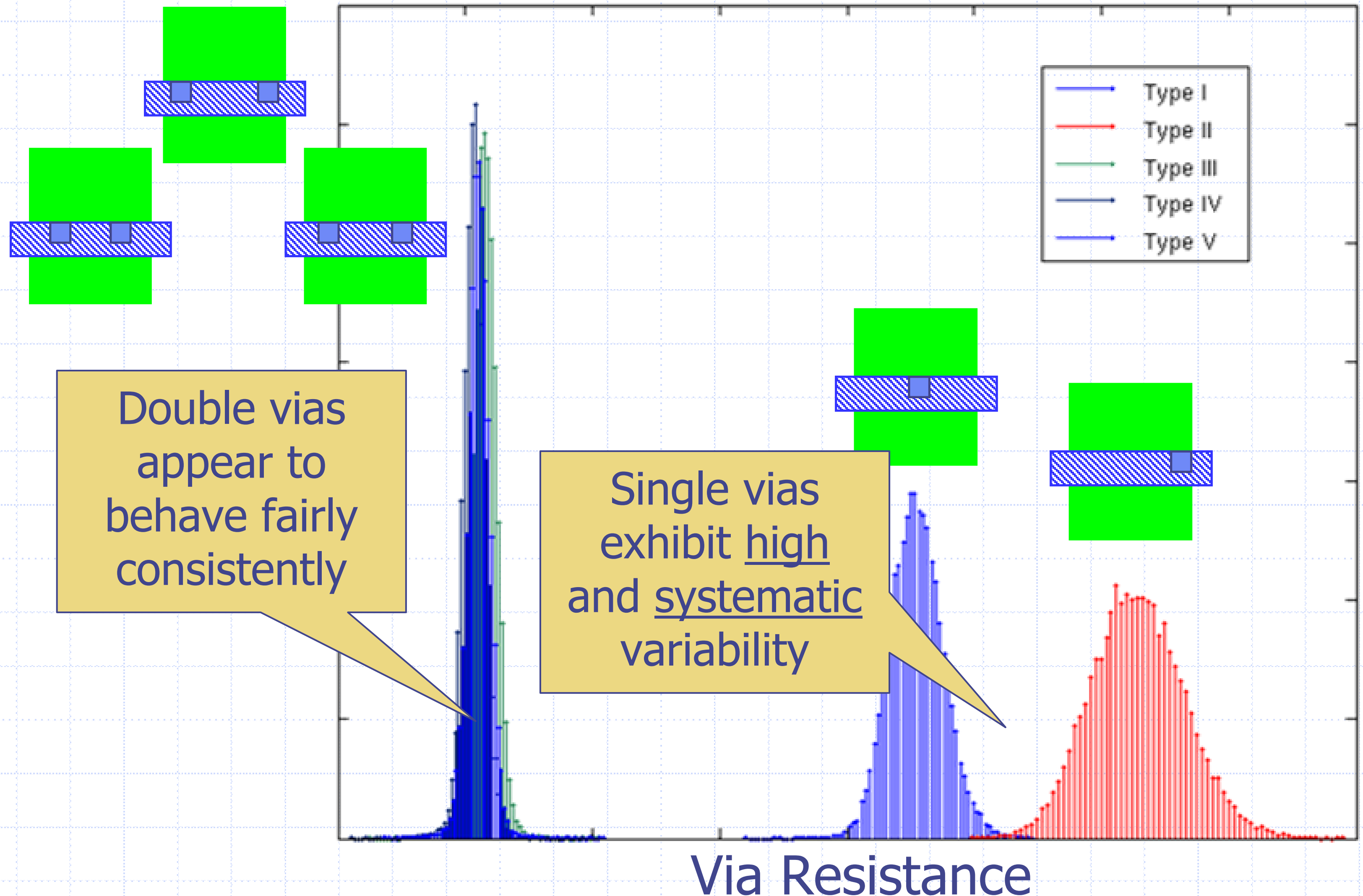


How Is This Happening?

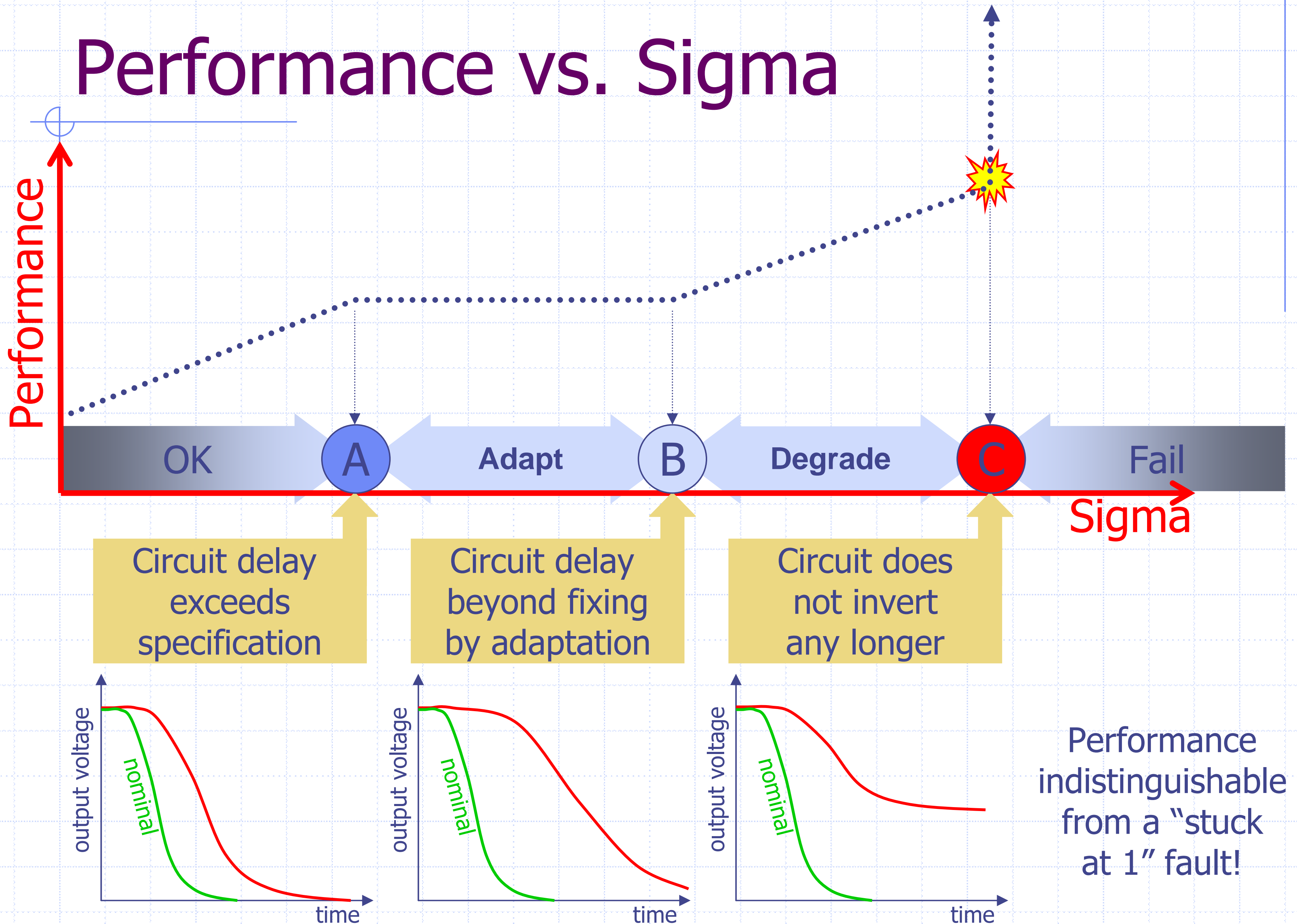
- Increased process complexity and systematic variability.
  - Example: a V_T of 0.25±0.1, a via of 20…200Ω.
  - Multidimensional: combination of multiple sources of variations.
- As variability increases, circuit performance passes from a degraded phase to a regime where failure becomes indistinguishable from hard (short/open) faults.



Random/Systematic Via Variability

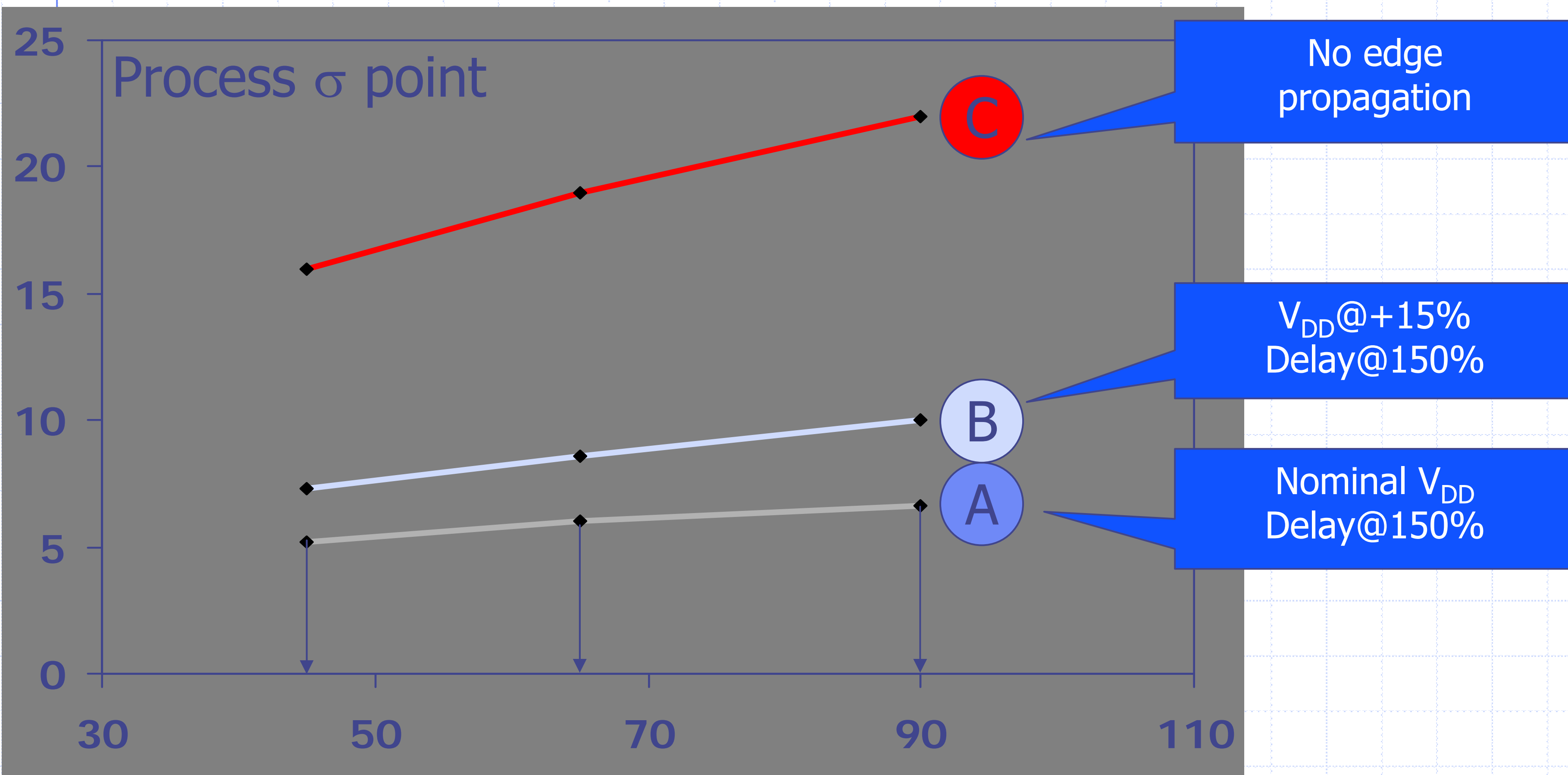


Performance vs. Sigma



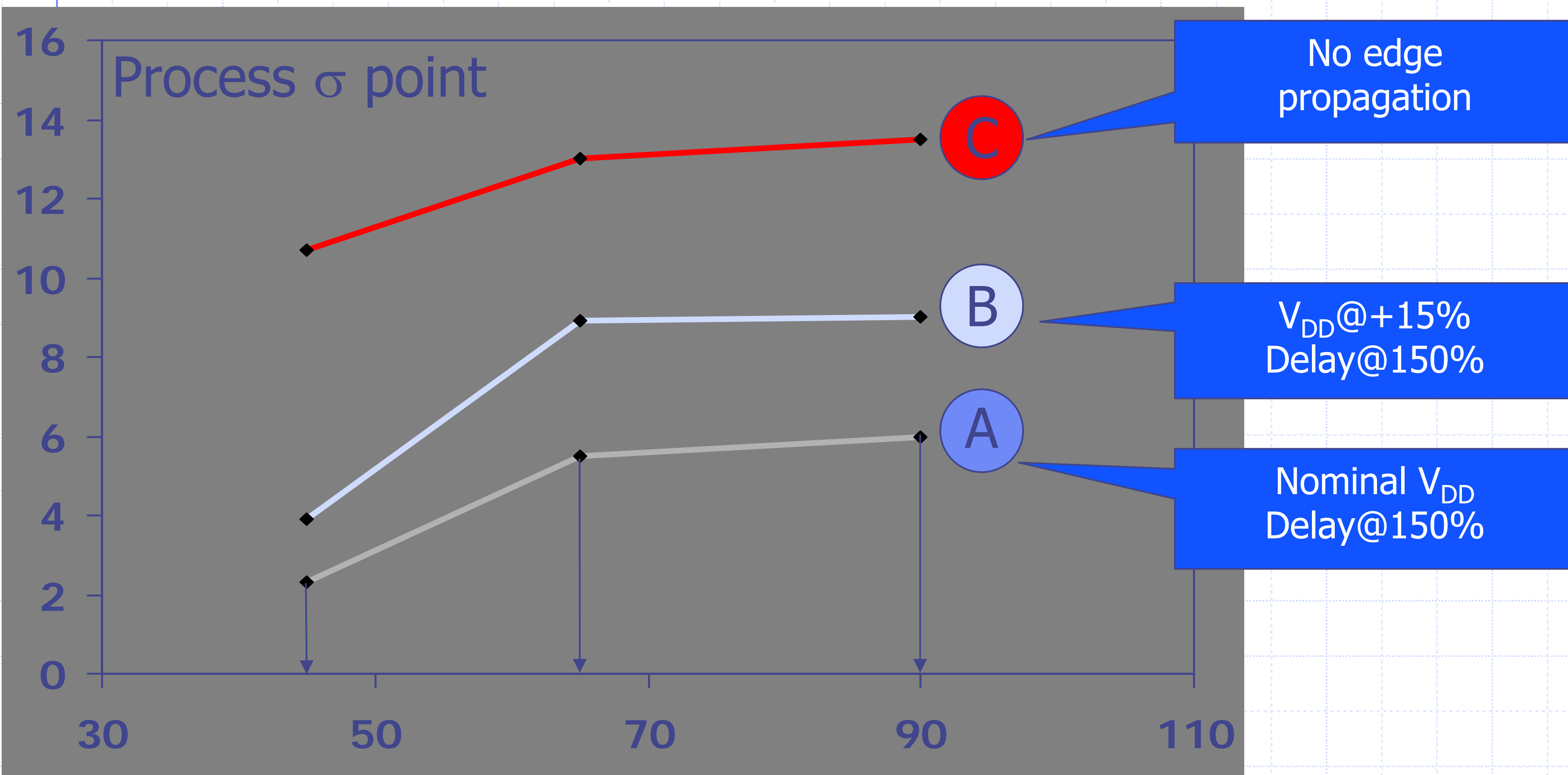
Trend For a Simple Buffer

- Simplest possible circuit (if this fails, everything else will).
- Performed analysis for 90nm, 65nm and 45nm.
- Clear trend in sigma!



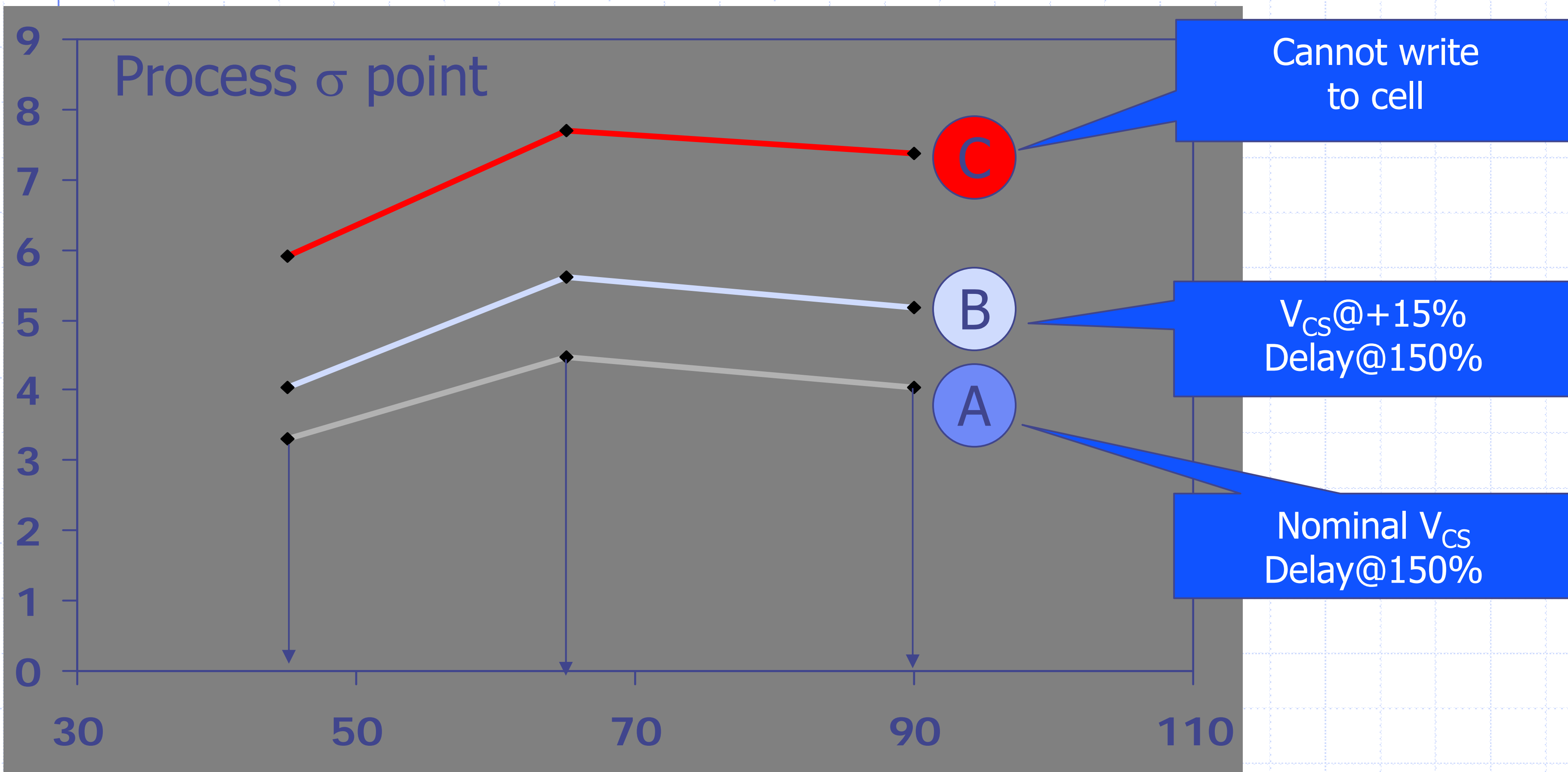
Technology Trend For a Simple Latch

- Pervasive circuit crucial for correct logic operation.
- Performed analysis for 90nm, 65nm and 45nm.
- Clear trend in sigma!



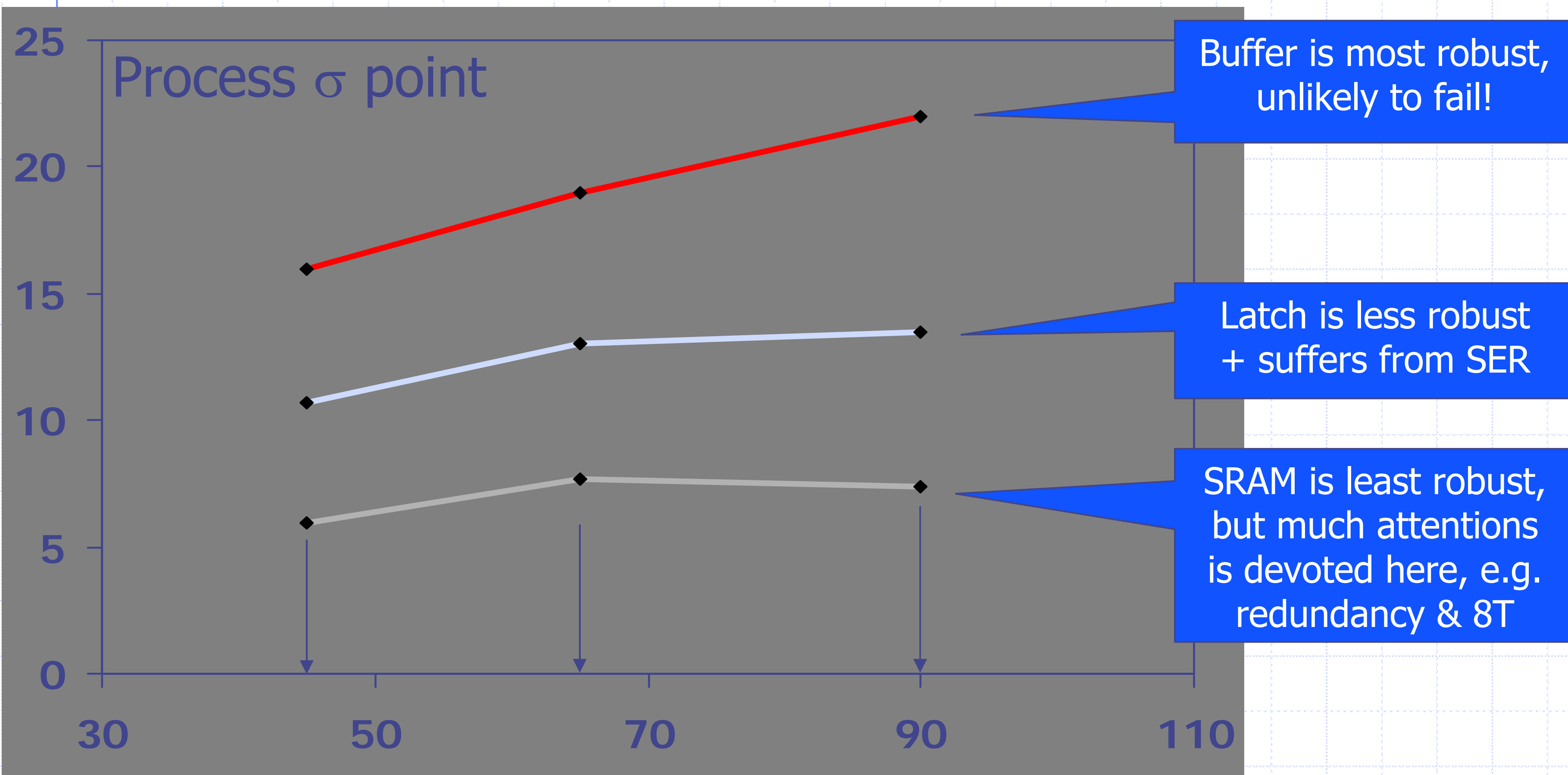
Technology Trend for an SRAM

- SRAM is known to be a more sensitive circuit… (lower σ).
- But, circuit heavily optimized for each technology.
- Much lower σ values + similar trend in sigma!



Comparison of Circuits (@Point C)

- Technology trend is modulated by circuit innovation and investment in analysis and optimization tools.
- Global trend remains clear!



Variability and Resilience

- We will likely need wide-spread resilience at and beyond the 32nm technology node.
- How much resilience and/or adaptation will be determined by how well we understand the fabrication process.
  - Firm understanding of the sources and impact of systematic variation is needed.
  - Magnitude of random or un-modeled variation will determine design margins (and design profit).
  - Models are critical to both!

Role of Modeling

- Modeling needs to become more aware of systematic and random variability.
  - As do other parts of the analysis flow, e.g. layout extraction.
- We need the ability to mix empirical and physical capabilities in a clean manner…
  - As we learn to make better characterization structures, the opportunity for early semi-empirical modeling will expand!

Ultimate Vision

Enable accurate model to hardware correlation and sophisticated design adaptation.