Behavioural Simulation and Synthesis of Biological Neuron Systems using VHDL

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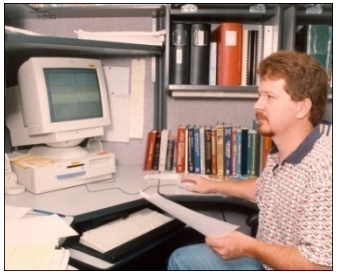
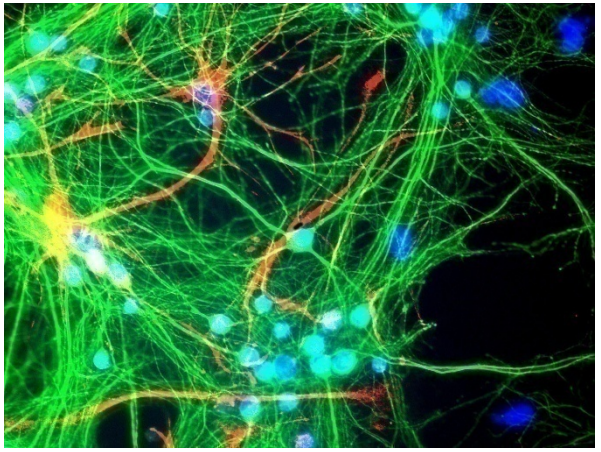
Presentation Outline

- Introduction
- The Nervous System
- VHDL Neuron Model
- VHDL Neuron Network Model
- Synthesis

Introduction

- Biologists & Engineers
- Investigate Neuron Structures
- Biological experiments
  - Live Tissue
  - Can’t Establish Connectivity
- Behavioural Modelling
  - Simulate behaviour
  - Determine network characteristics





Stained Rat Cortical Neurons [1]

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[1] - EnCor Biotechnology 2003, http://www.encorbio.com/Album/pages/ChkMAP2-GFAP-Hoe-40X-1.htm

Motivation

- Biologically realistic simulation
- Efficient Models
- Reduce run time
  - Hardware acceleration
  - Real Time Simulation
  - Virtual Animal/Nervous System
- Reusable Libraries
  - Easily configurable

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- VHDL Neuron Network Model
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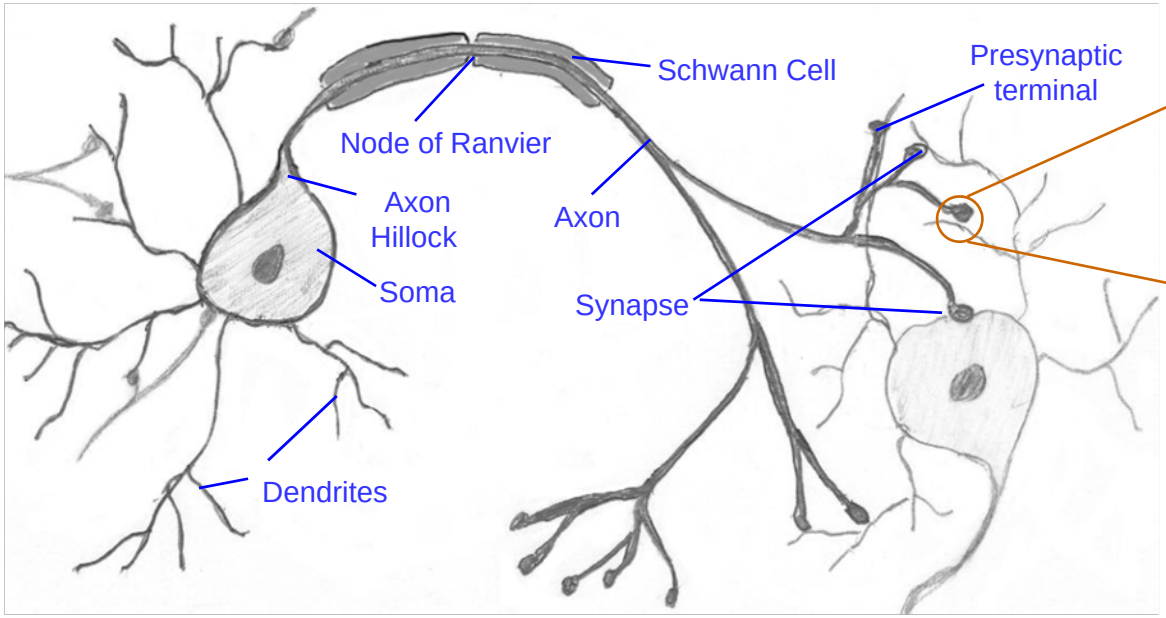
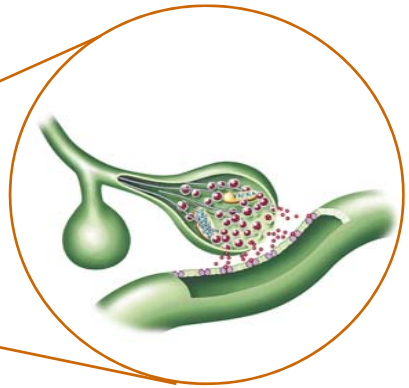
A Typical Neuron

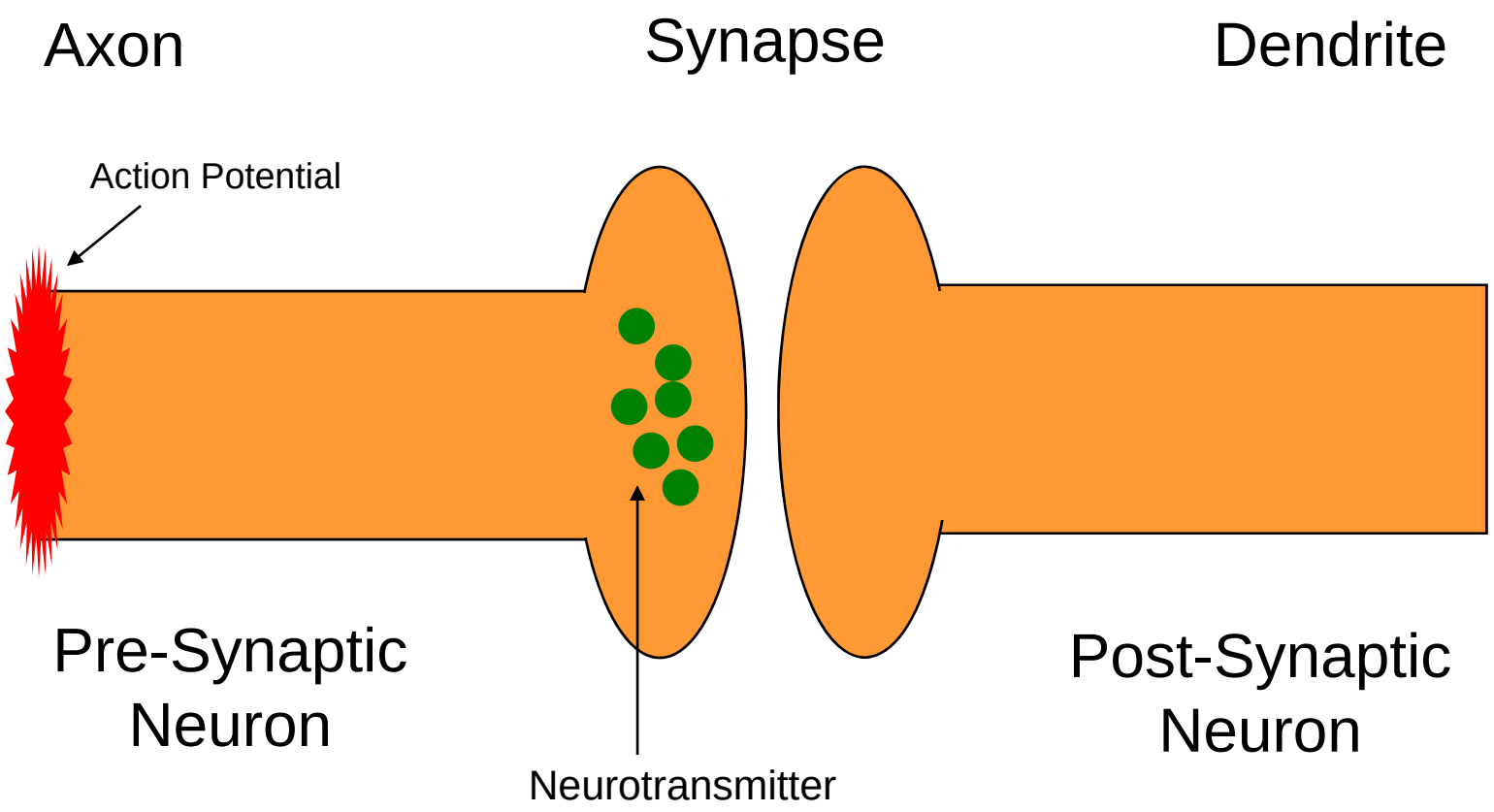


A Typical Neuron



A Synapse

Neuron Signalling



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History of the VHDL Model

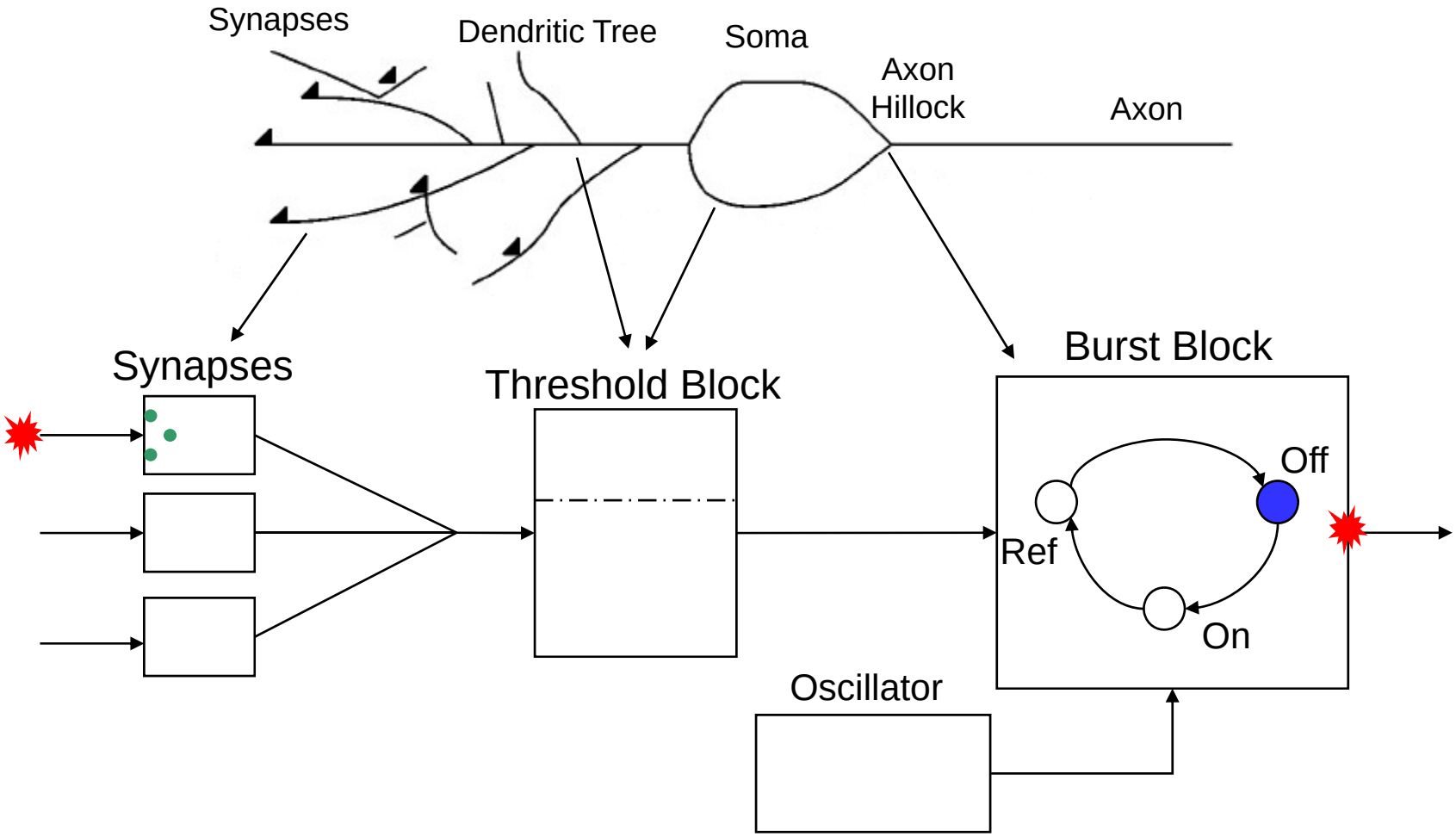
- Cell Automata Model
  - Enric Claverol, 2000

    Claverol, E.T. Brown, A.D. Chad, J.E., ”Message Based Event Driven Model (MBED) A large-scale simulation of the piriform cortex by a cell automaton-based network model”, IEEE Trans. Biomedical Engineering, Vol. 49(9), pp 921-935, Sept 2002.

- System C Neuron Model
  - Sankalp Modi, BMAS, 2004

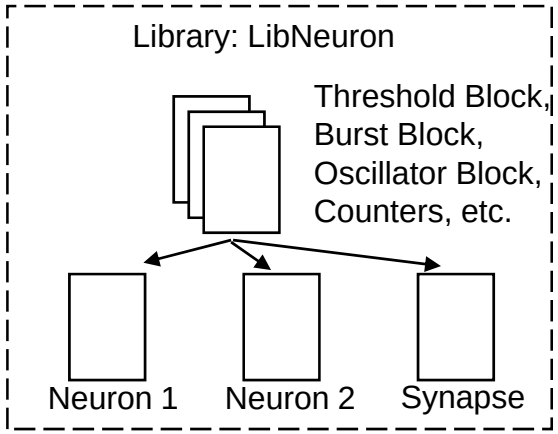
- VHDL Biologically realistic neuron model
  - Julian Bailey, BMAS 2007

Model Overview

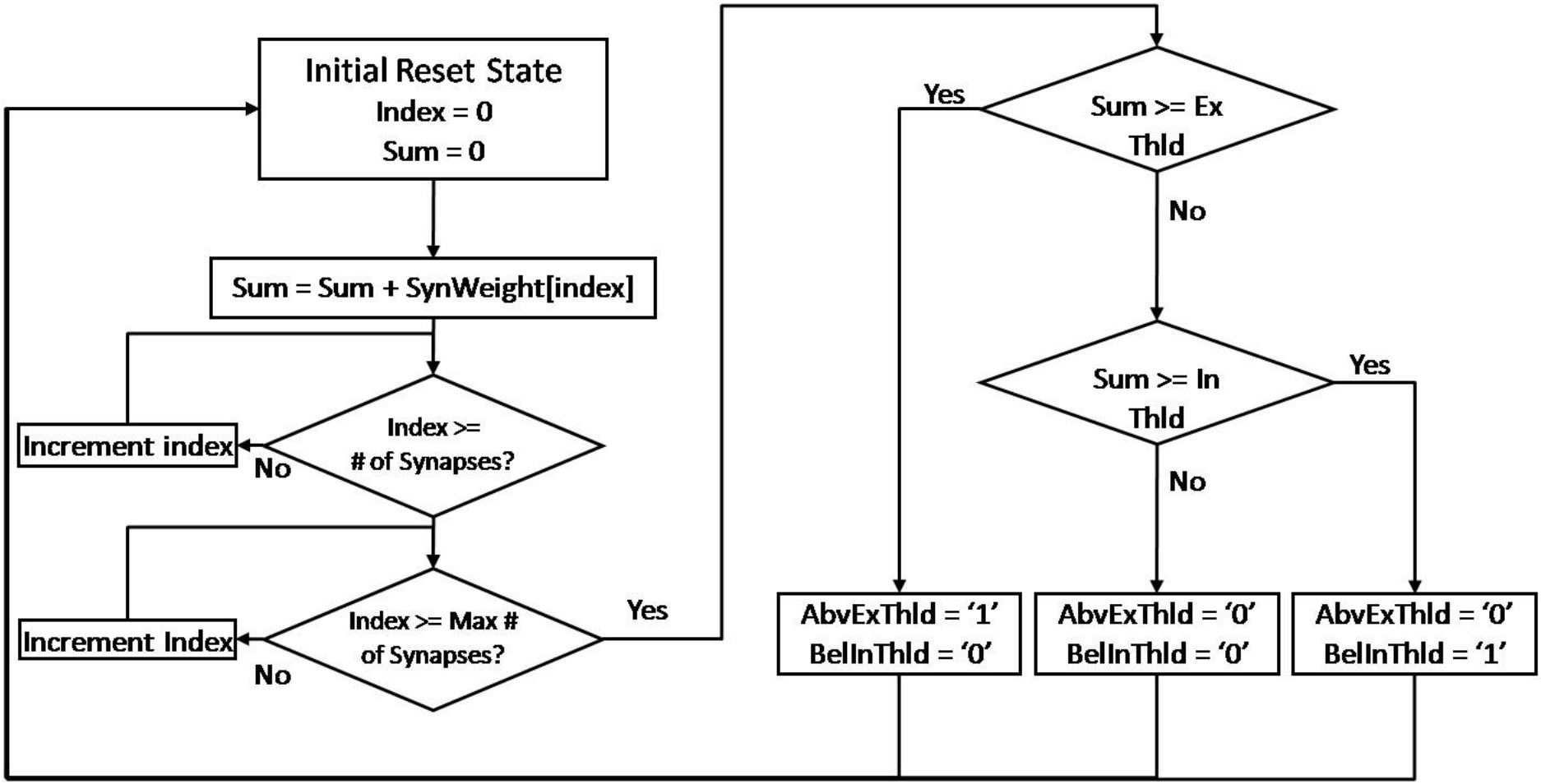


More Model Details

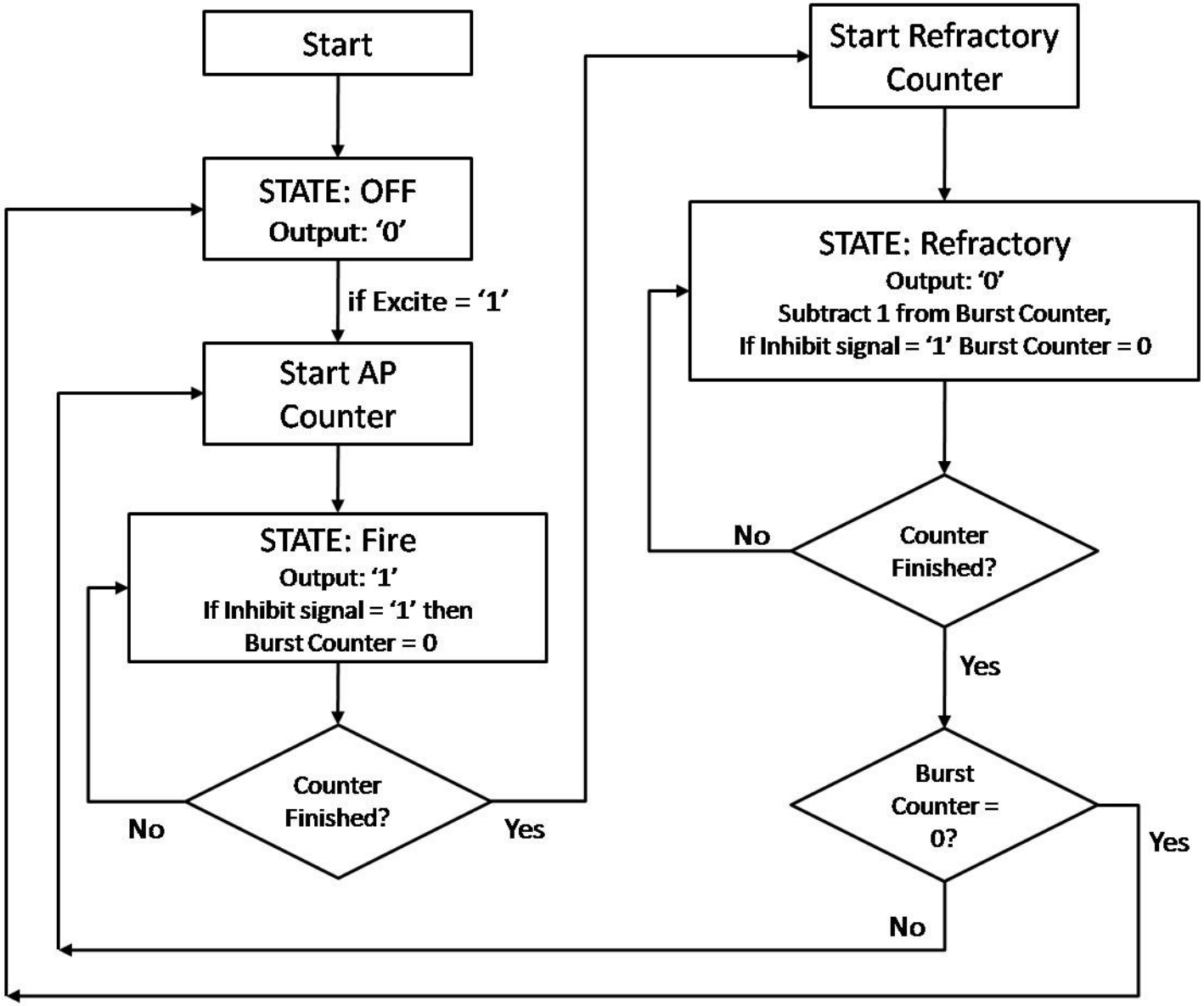
- Neuron Library - LibNeuron
  - Contains all Sub Components
- Three top level entities
  - Neuron 1
  - Neuron 2 (Oscillator Activated Neuron)
  - Synapse
- Each Configurable using Generics



Sub Component – Threshold Block

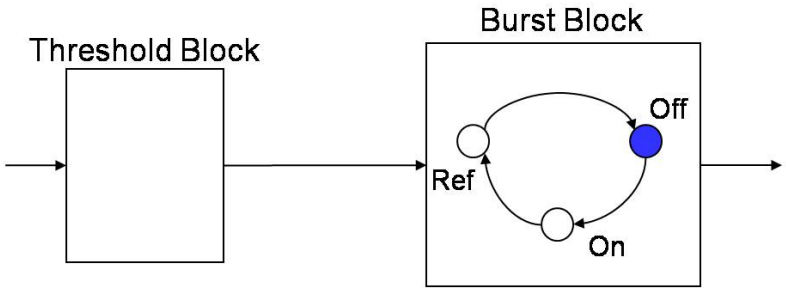


Sub Component – Burst Block

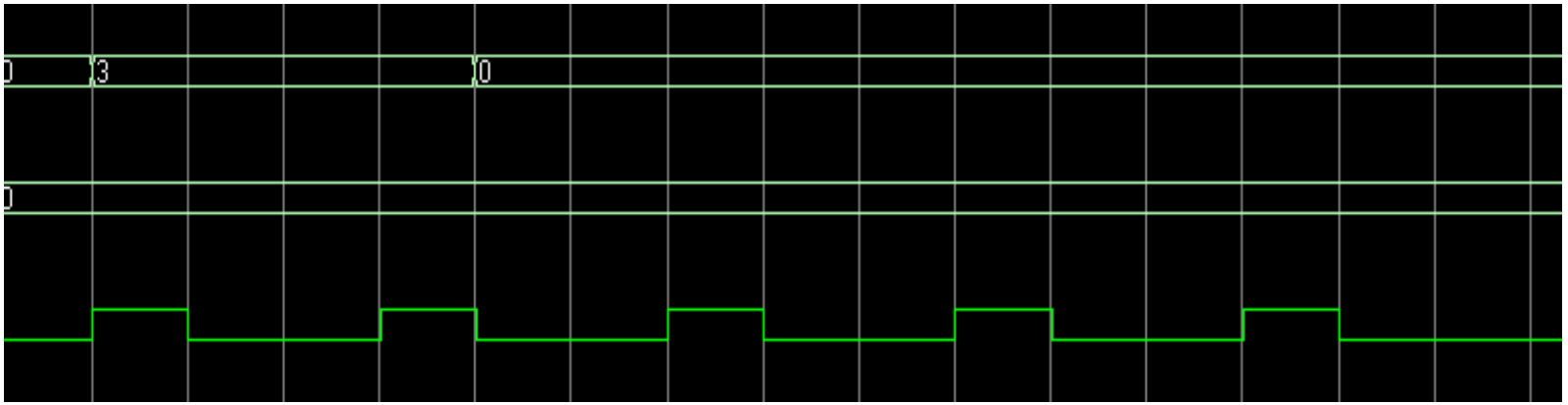


Neuron 1

- “Standard” Neuron
- Activated by Synapses

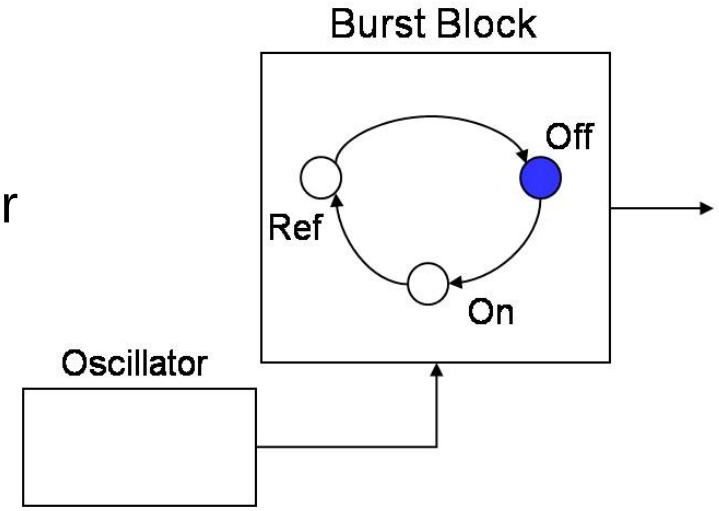


Example Parameters:- Threshold 3, AP Time 1 ms, Ref. Time 2 ms, Burst 5.

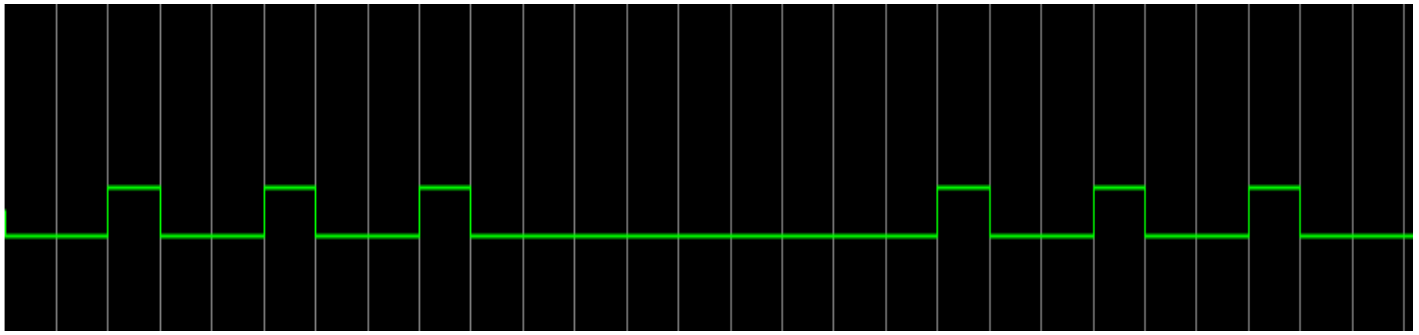


Neuron 2

- Neuron to drive network
- Activated periodically by oscillator

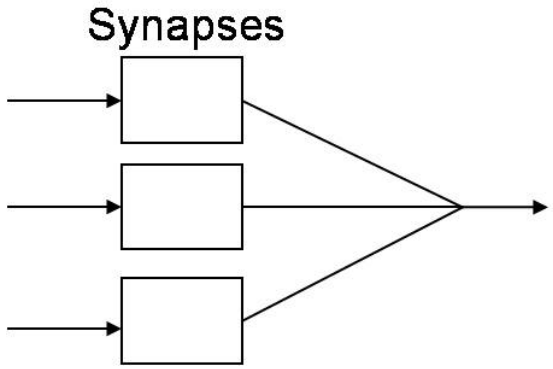


Example Parameters:- Period 16 ms, Phase 2ms, AP Time 1 ms, Ref. Time 2 ms, Burst 3.

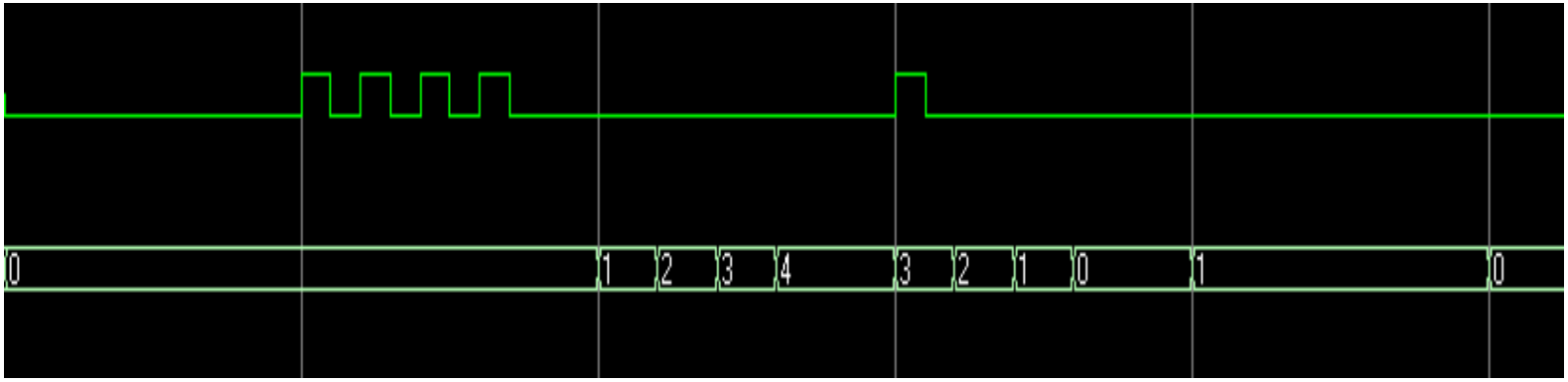


Synapse

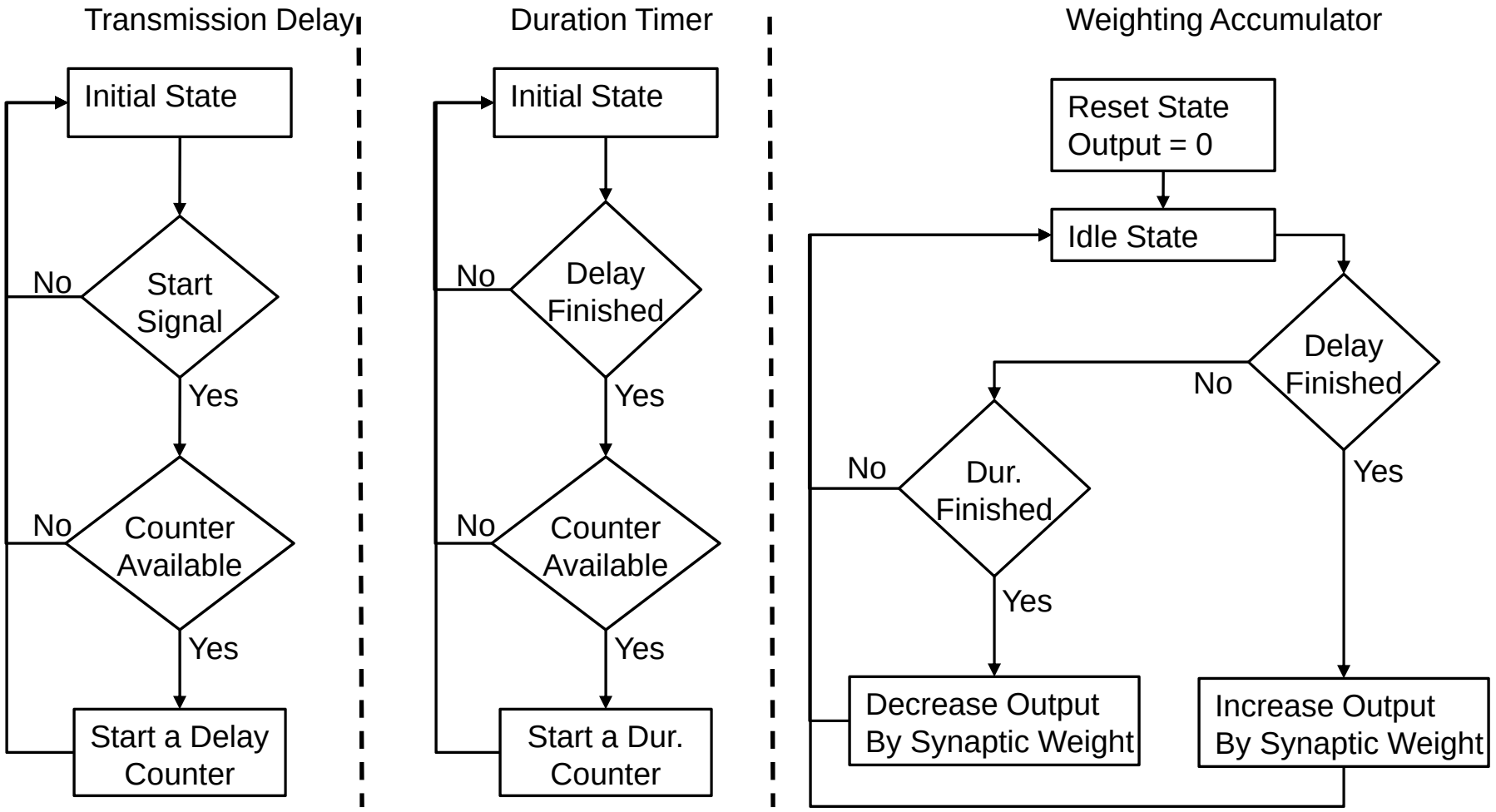
- Connect Neurons
- Model Delays & Activation Duration
- Can be activated once already active



Example Parameters:- Delay 1ms, Duration 1ms, Weighting 1.



Inside the Synapse



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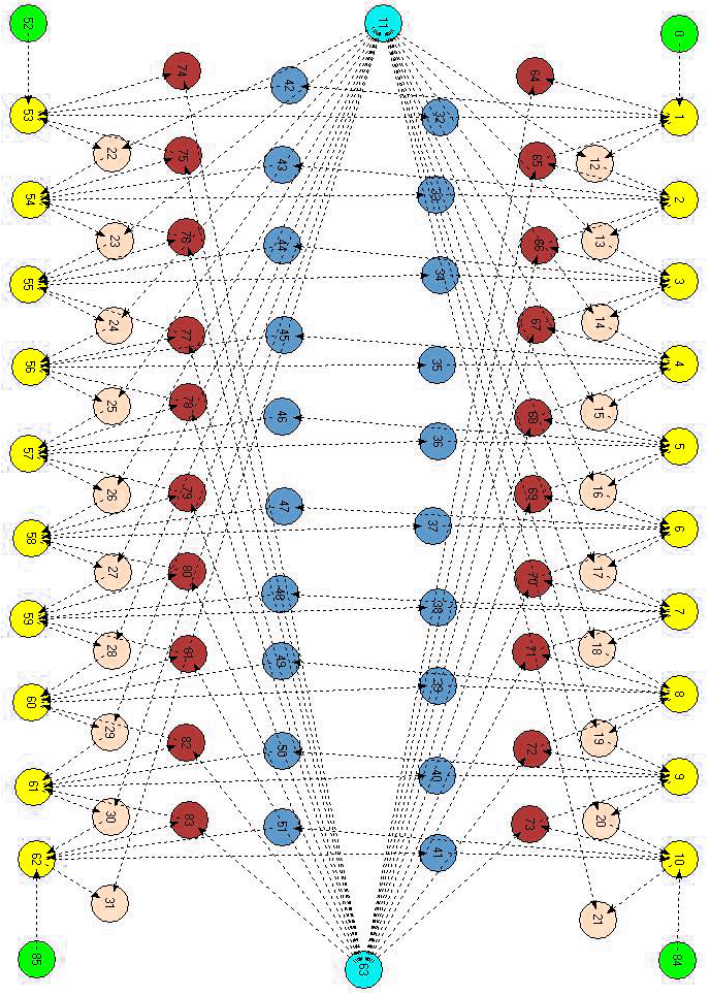
Model Verification

- Nematode, C Elegans
  - 302 Neurons
  - Extensively studied
  - Connections partially known



Muscle

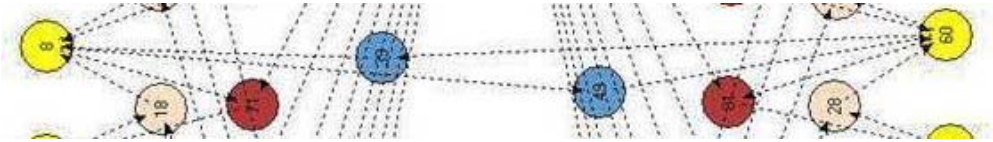
Cross Inhibition

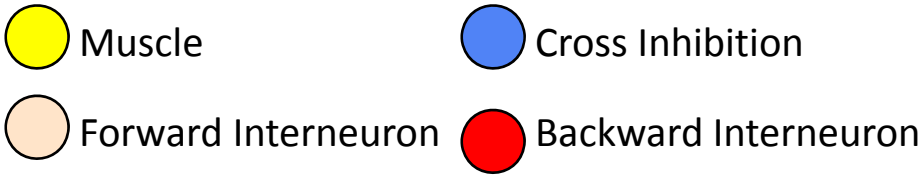
Forward Interneuron

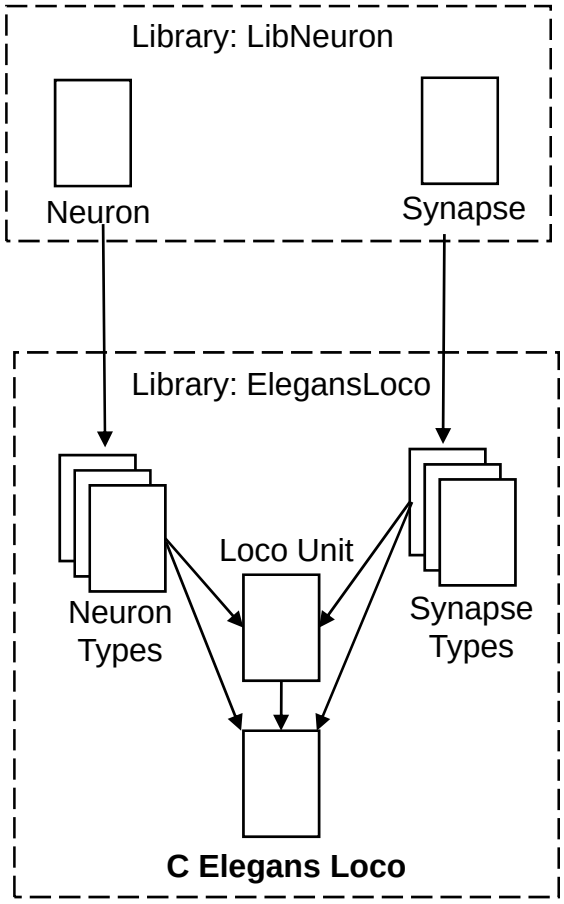
Backward Interneuron

LibElegans VHDL Library

- Animal Library
  - ElegansLoco
- Specifies Generics
  - Creates Types
  - Repeated Pattern “Loco Unit”







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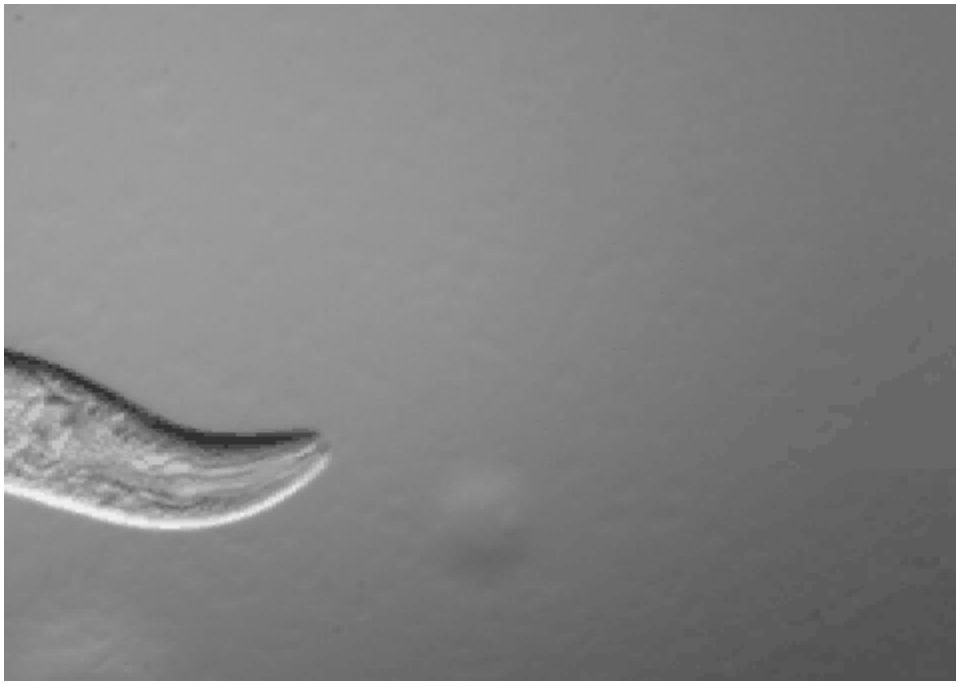
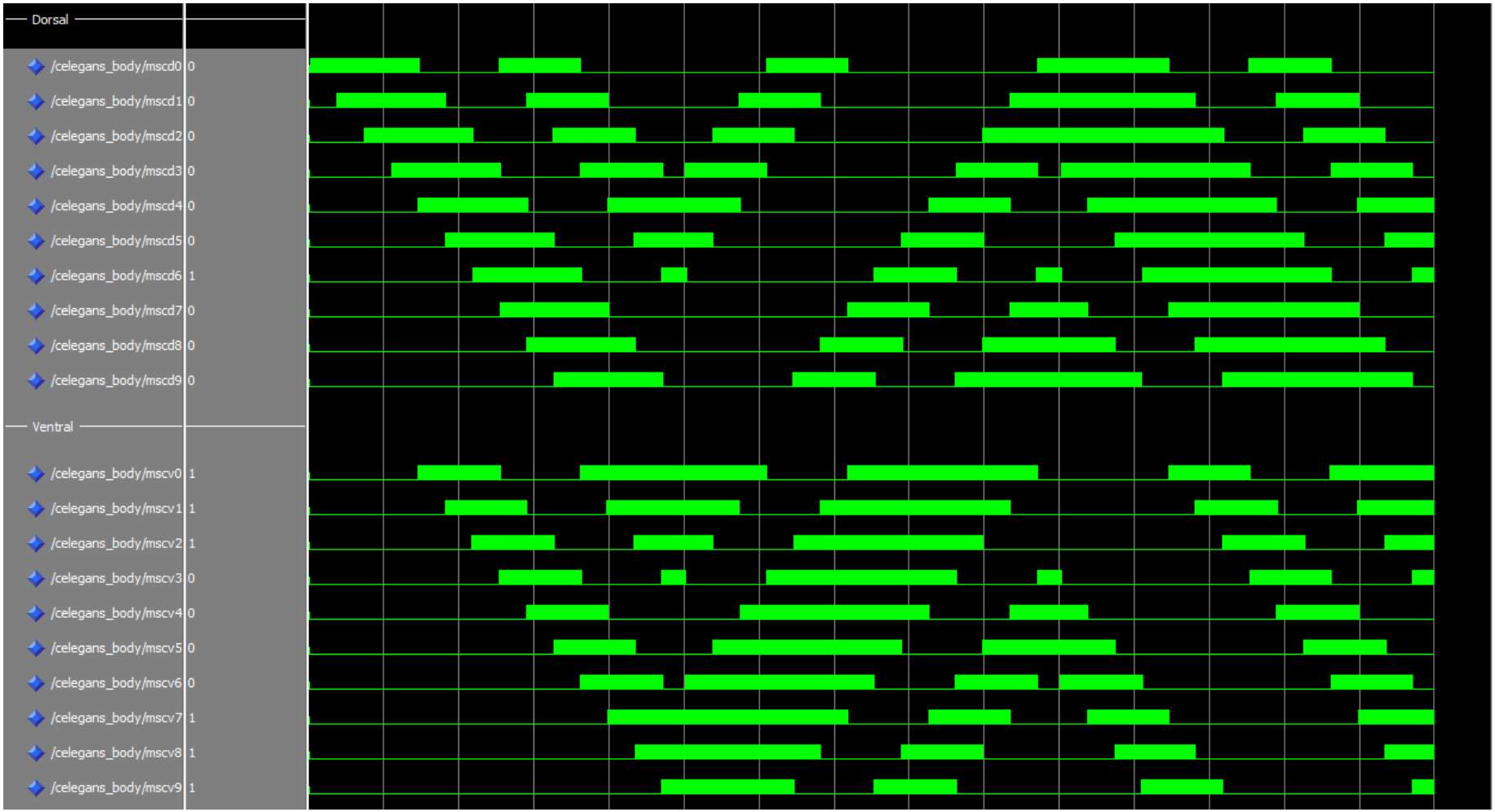
C Elegans



Simulation Results



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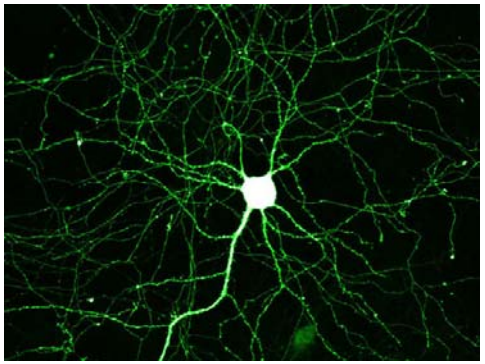
Synthesis

- Previous work
  - C Elegans Design Size (200k FG, 85k DFF's)
- Optimisation
  - 2 Types of Neuron
  - User Definable Length Counters
  - Up Counters only
  - Disable Pins on all blocks
- Design fits on many more devices
  - 60,506 FG's & 48,891 DFF's
- Hardware acceleration



Stained Hippocampal Neuron [1]

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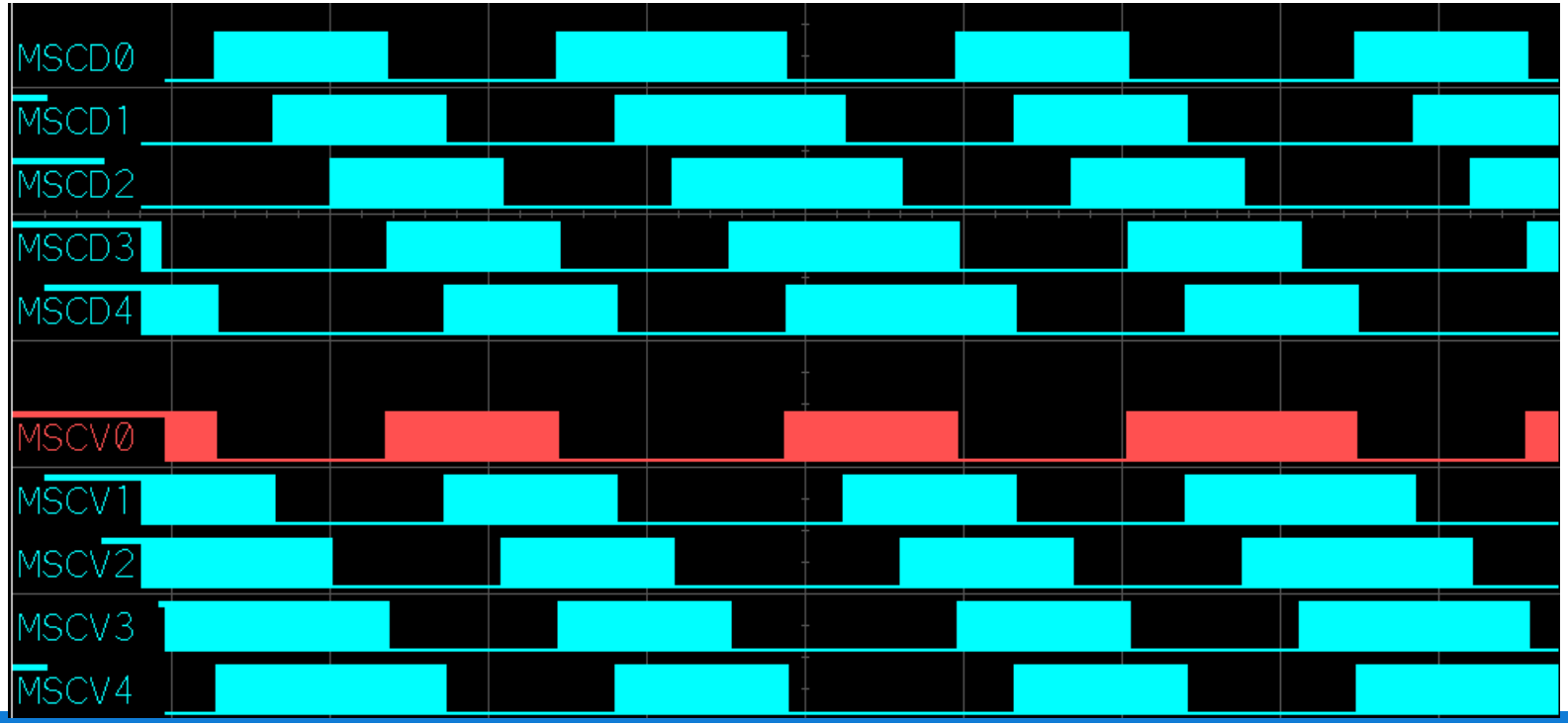
[1] - EnCor Biotechnology 2003, http://strangepaths.com/wp-content/uploads/2006/10/neuron.jpg

Synthesis Example

- A section of C Elegans (Mini Elegans)
  - 33 Neurons, 50 Synapses
  - Only goes forwards



Hardware Acceleration

- Traditional Simulations
  - Hours -> Days
  - Example: Mini Elegans (6 Sec) – 3 hours 20 mins
  - Example: C Elegans (15 Sec) – 32 hours 12 mins
- In Hardware
  - Real-Time
  - Example: Mini Elegans (6 Sec) – 6 Seconds! (2000x Faster)
  - Near Future : C Elegans (15 sec) – 15 Seconds! (7728x Faster)
- However...
  - Limited by Current FPGA Technology
  - Large Scale Multi-Processor Hardware Simulation Frameworks
    - Spinnaker - Univ. Southampton, UK & Univ. Manchester, UK

Summary

- Synthesizable Neuron Library
- Post-Synthesis Verification
  - Compared against previous work
  - C Elegans
- Post Synthesis design
  - Reasonably sized
  - Download onto FPGA
  - Hardware acceleration
  - **Virtual Animal/Nervous System on FPGA!!!**

Thanks For Listening!

- Any Questions ?