Improved Phase Noise Model for Ultra Wideband VCO

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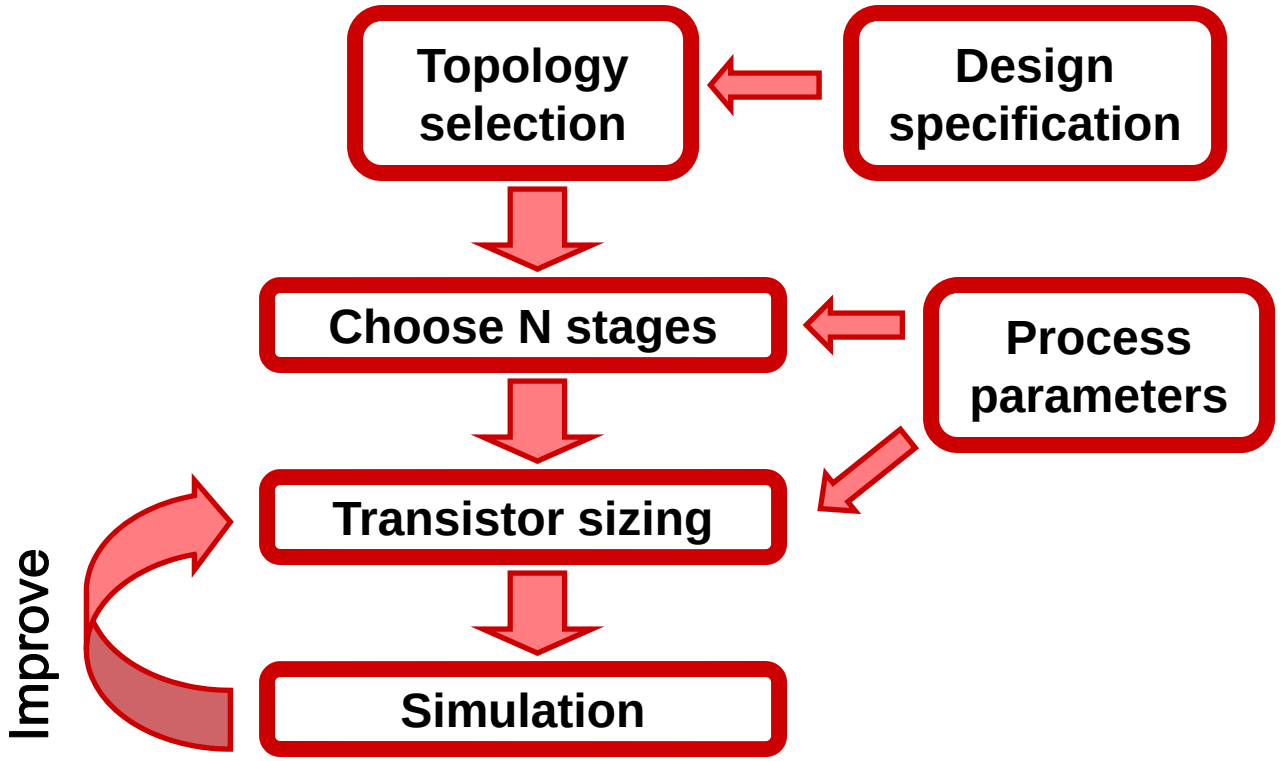
Presentation outline

- Research motivation
- Improved phase noise model
- Simulation results
- Measurement results
- Conclusions

Research motivation

- **Typical VCO design flow**
  - Topology and number of stages chosen from experience
  - Starting point and simulation led improvement



Research motivation

- **Voltage controlled oscillator design challenges**
  - Lack of detailed transistor sizing guidelines which relate high level specifications to W and Ls.
  - Small signal model (Barkhausen Criteria) only holds valid for linear operation.
  - Jitter/Phase noise performance is an important specification in VCO design.
  - Phase noise and jitter simulations in leading simulators (e.g. SpectreRF) are extremely time consuming.

Requirement for a phase noise targeted transistor sizing model.

Research motivation

- **Previous work has considered a number of factors when modelling VCO phase noise**
  - Process parameters
  - Power supply
  - Topology
  - Transistor dimensions
  - Oscillation frequency

- **However:**

No one has considered the effect of frequency tuning on phase noise.

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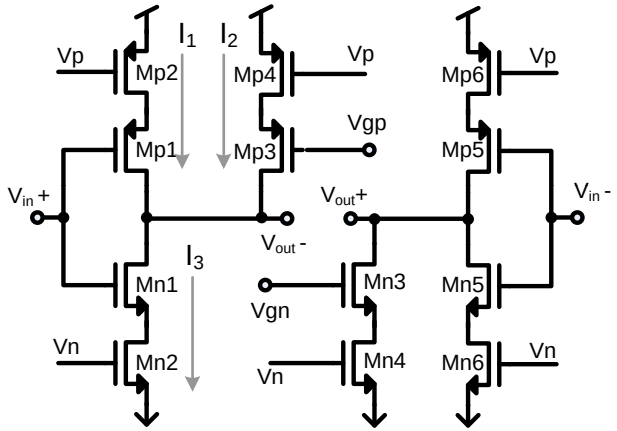
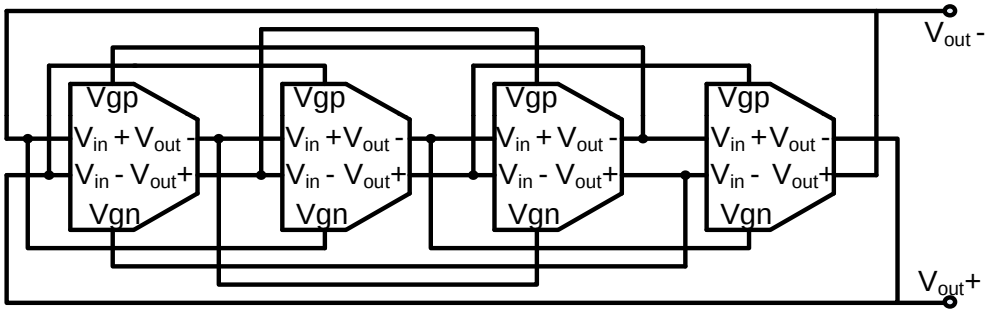
Improved Phase Noise model

- **The proposed model is based on the new dual inverter delay cell which has 10 octave tuning range.[1]**





- **Previous design guidelines for this cell simply ensure that $I_1 + I_2 = I_3$**

$$\left(\frac{W}{L}\right)_n = \frac{\mu_p}{\mu_n}\left[\frac{\frac{V_{DD}}{2}-|V_{tp}|}{\frac{V_{DD}}{2}-|V_{tn}|}\right]^2\left[\left(\frac{W}{L}\right)_{p1}+\left(\frac{W}{L}\right)_{p3}\right]$$

[1] Li Ke, Reuben Wilcock, Peter Wilson "Improved 6.7GHz CMOS VCO Delay Cell With Up To Seven Octave Tuning Range ", *Proceddings of IEEE ISCAS*, May 2008

Improved Phase Noise model

- **For a phase noise orientated design approach, existing models can be expressed as[2] :**

$$L(f) = \frac{1}{2NV_{eff}^2 C_{ox}} \left(\frac{K_{fn}}{W_{n1}L_{n1}} + \frac{K_{fp}}{W_{p5}L_{p5}} \right) \left(\frac{f_0^2}{f^3} \right)$$

- **Takes account of:**
  - Oscillation frequency: f_0
  - Process parameter: K_{fn},K_{fp}, C_{ox}
  - Transistor dimensions: W_{n1},L_{n1}, W_{p5}, L_{p5}
  - Topology: N

(Generally accepted that 1/f noise dominates the spectrum up to a few MHz)

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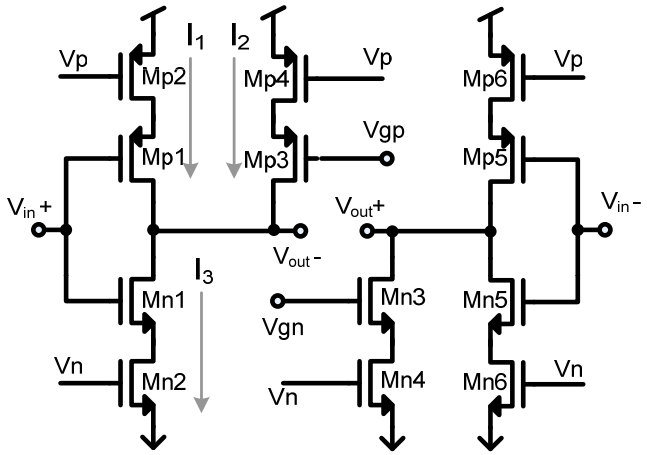
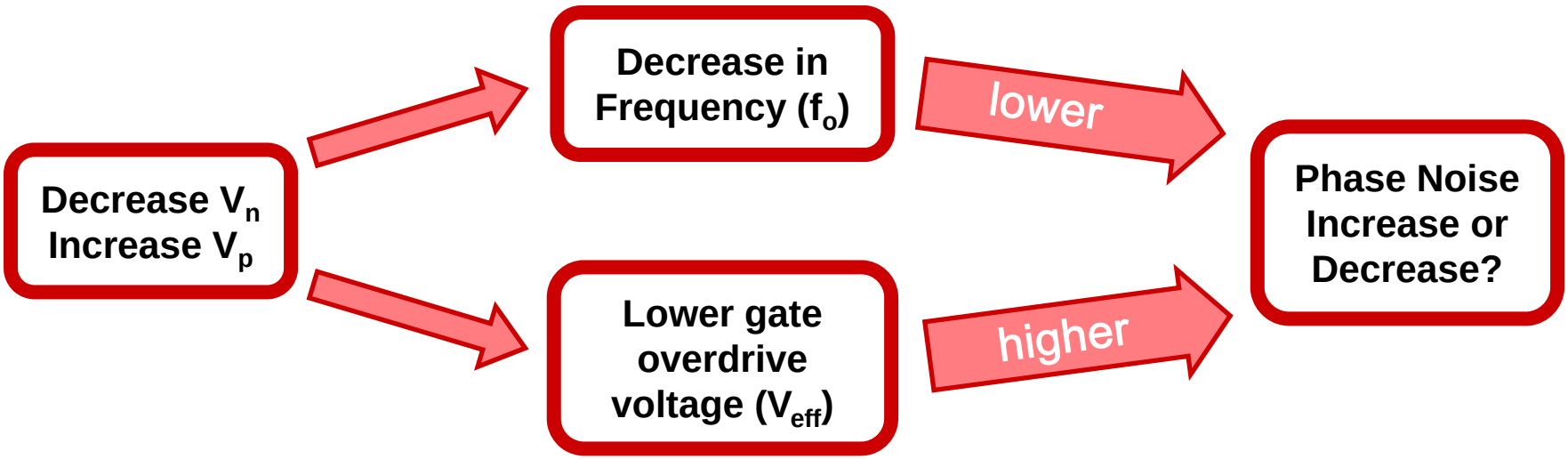
[2] Sohrab Samadian, Michael M. Green, **"Phase Noise in Dual Inverter-Based CMOS Ring Oscillator"**, *Proceddings of IEEE ISCAS*, May 2006

Improved Phase Noise model

- **What happens when the tuning voltage changes?**

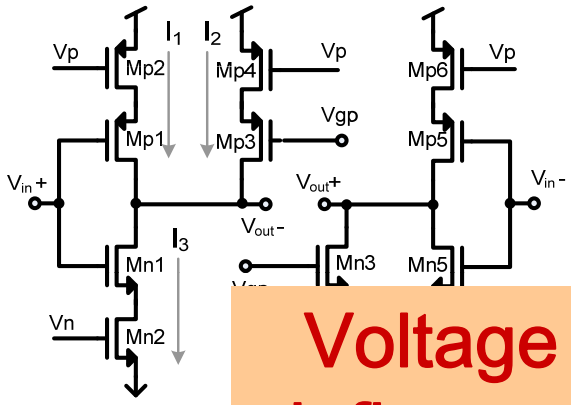


$$L(f) = \frac{1}{2NV_{eff}^2 C_{ox}} \left(\frac{K_{fn}}{W_n L_n} + \frac{K_{fp}}{W_p L_p} \right) \left(\frac{f_0^2}{f^3} \right)$$



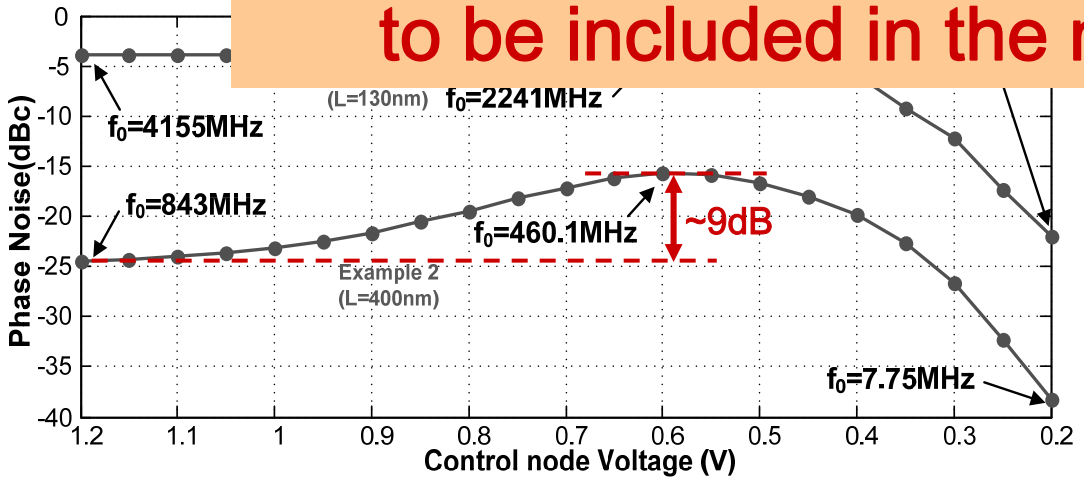
Improved Phase Noise model

- **Post layout simulation results (SpectreRF-PSS-Pnoise)**



Example 1(W/L)um		Example 2(W/L)um	
Mn1,Mn2	40/0.13	Mn1,Mn2	64/0.4
Mp5,Mp6	103/0.13	Mp5,Mp6	202/0.4
Mn3—Mn6	20/0.13	Mn3—Mn6	32/0.4
			101/0.4

Voltage tuning mechanism does influence phase noise and needs to be included in the model.

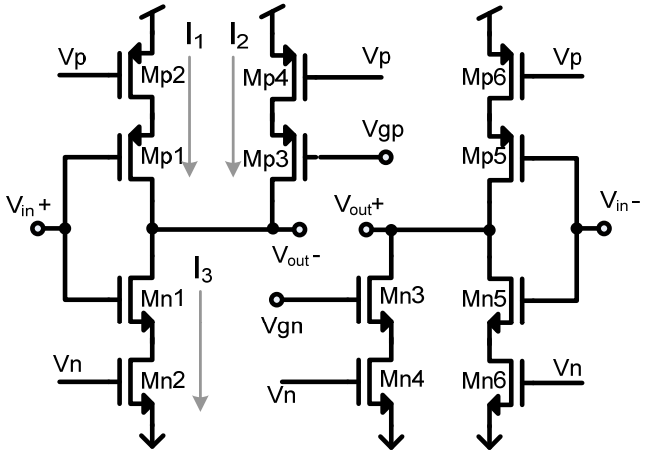


tuning voltage effect on phase noise

- The worst case occurs at half the tuning range.
- Above half tuning range, phase noise improves

Improved Phase Noise model

- **Including the voltage tuning mechanism in the model: part 1**



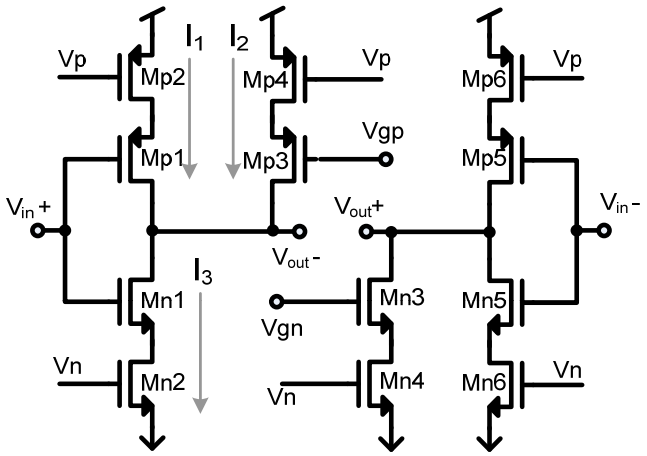
- We introduce the terms instantaneous current I_{inst} and maximum achievable current I_{max} .
- I_{inst} corresponds to the V_{ninst} and I_{max} correspond to V_{nmax} which is the maximum achievable control node voltage (normally equal to V_{dd}).
- Use the I_3 as an example, from the simulation, the ratio of these two values can be expressed as:

$$P = \frac{I_{3\max}}{I_{3inst}} = \frac{V_{\mathrm{nmax}} - ((L_{\min} + L_{n1}) / 2L_{\min})V_{tn}}{V_{\mathrm{ninst}} - ((L_{\min} + L_{n1}) / 2L_{\min})V_{tn}}$$

- L_{min} is the minimum allowable transistor length defined by process

Improved Phase Noise model

- **Including the voltage tuning mechanism in the model: part 3**



- Combine the two equations, and consider all the noise contributors.
- Valid when Mp2, Mp4, Mn2, Mn4, Mn6, Mp6 are working in the deep triode region.
- In practice I_{n1} and I_{3max} have the same amplitude because Mn1 and Mn2 have the same dimensions so this term cancels.

$$\mathcal{L}(f) = \left(\frac{V_{nmax} - \left(\frac{L_{min} + L_{n1}}{2L_{min}}\right)V_{tn}}{V_{ninst} - \left(\frac{L_{min} + L_{n1}}{2L_{min}}\right)V_{tn}}\right)^2 \left(\frac{I_{n1}^2}{I_{3max}^2}\right) \frac{\left(\frac{K_f}{W_{n1}L_{n1}} + \frac{K_f}{W_{p5}L_{p5}}\right)}{2N\left(\frac{V_{dd}}{2} - V_t\right)^2 C_{ox}} \left(\frac{f_0^2}{f^3}\right)$$

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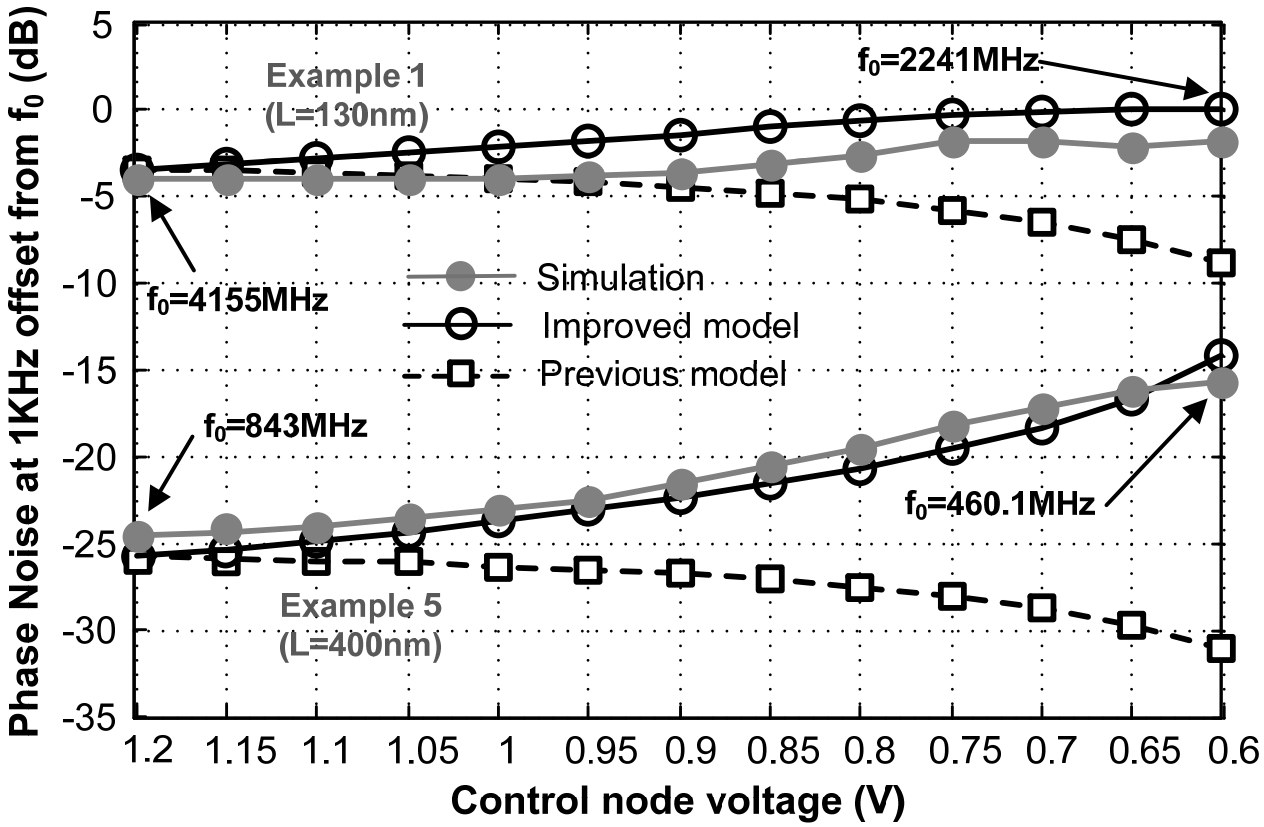
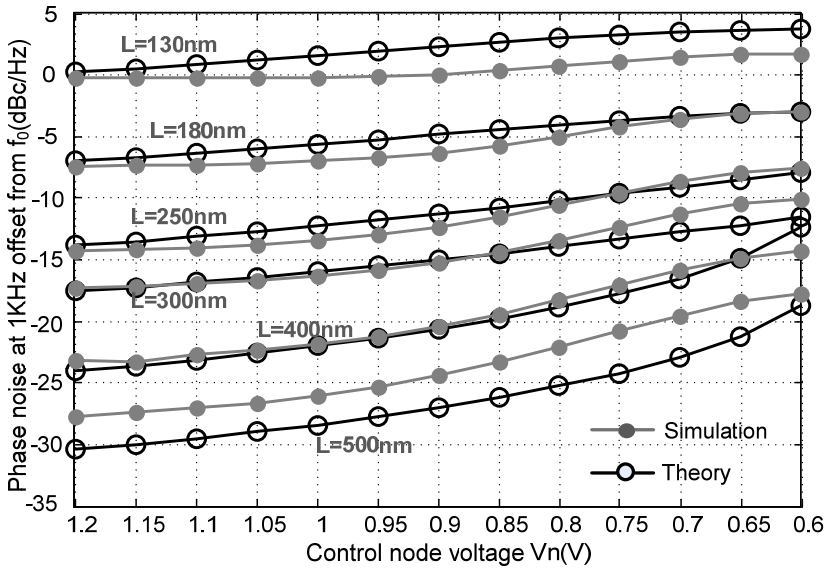
Simulation results

- **The results show good comparison with simulation.**
  - Previous model only valid at highest frequency



Simulation results

- **Further model validation**
  - Transistor lengths from 120nm to 500nm
  - Phase noise simulations
  - Error is less than 3dB over 0.6-1.2V tuning range

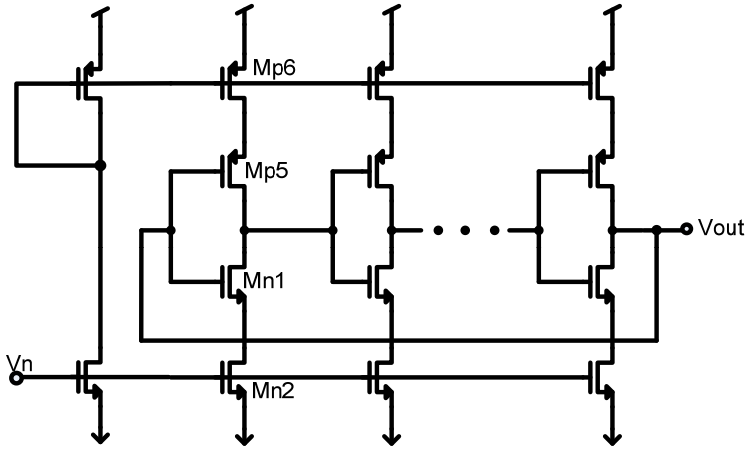


Example number:	Transistor Dimensions:		Performance at Vn=1.2V		Performance at Vn=0.6V	
	Wp5/Lp5 (um)	Wn1/Ln1 (um)	Oscillation frequency(MHz)	Phase Noise at 1KHz offset from f_0(dBc/Hz)	Oscillation frequency(MHz)	Phase Noise at 1KHz offset from f_0(dBc/Hz)
1	103/0.13	40/0.13	6521	-0.237	3592	1.645
2	132/0.18	48/0.18	3934	-7.4	2144	-2.94
3	168/0.25	56/0.25	2301	-14.25	1258	-7.53
4	153/0.3	50/0.3	1695	-17.27	928.8	-10.03
5	202/0.4	64/0.4	1026	-23.21	566	-14.32
6	260/0.5	80/0.5	687.5	-27.72	380.5	-17.77

Simulation results

- **Verification of model for single ended designs**

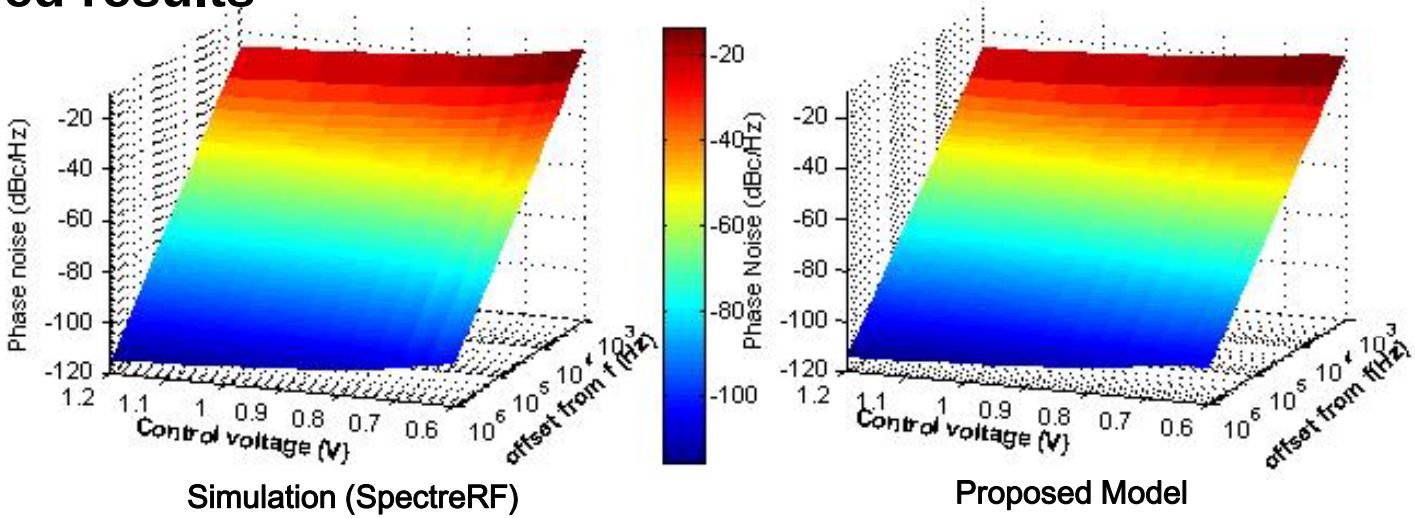
```
eox = 3.45e-11; % permittivity of the silicon oxide F/m
tox = 2.462e-9; %gateoxide thickness m
Cox = eox/tox; % gate oxide capacitance per unit areaf/m^2
Kfp = 1e-24; % Flcker noise coefficient
Kfn = 1e-24; % Flcker noise coefficient
Vt=0.25;  % Threshold voltage for the process
Vdd=1.2; % Vdd
Veff= (Vdd/2-Vt) ;
f= 1e3:1e3:1e6; % offset frequency with 1KHz step size
Wp=202e-6; % PMOS width
Wn=64e-6;  % NMOS width
L=400e-9;  %Transistor length
N=5;   % number of delay stages
p=(130+400)/(2*130);  %  Coefficient

Vninst=0.6:0.05:1.2; %Vn instant control voltage
Vpinst=1.2:-0.05:0.6; %Vp instant control voltage
f0=364e6:26.8e6:686e6; %oscillation frequency
for j =1:length(f0)
   for i=1:length(f)
   Lf2(i) = ((Vdd-p*Vt)/(Vninst(j)-p*Vt))^2*(1/(1*N*Veff^2))*((Kfn/(Wn*L*Cox)))*(f0(j)^2/f(i)^3)+((Vpinst(13)-
p*Vt)/(Vpinst(j)-p*Vt))^2*(1/(1*N*Veff^2))*((Kfn/(Wp*L*Cox)))*(f0(j)^2/f(i)^3); %phase noise  calculation
logf2(i)=10*log10(Lf2(i));
   end
   logfcaltotal(j,:)=logf2;
end
load phasenoise_simulation   %(Load the Simulation results from cadence spectreRF)
logfsimulation=phasenoise_simulation';
error=abs(logfsimulation-logfcaltotal);  % Calculate the abslute error between the Theory and simulation
```



singled ended design

Simulation results

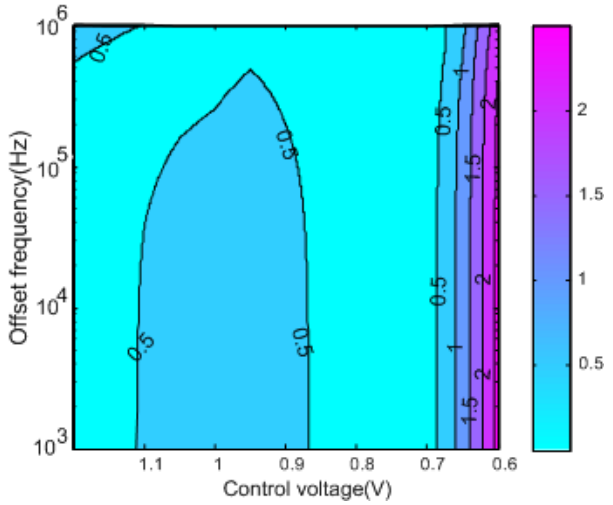
- **Single ended results**



Simulation (SpectreRF)

Proposed Model

- **Error analysis**
  - From the surface plots, the maximum error is less than 3 dB.
  - The proposed phase noise model holds valid for single ended oscillators as well.



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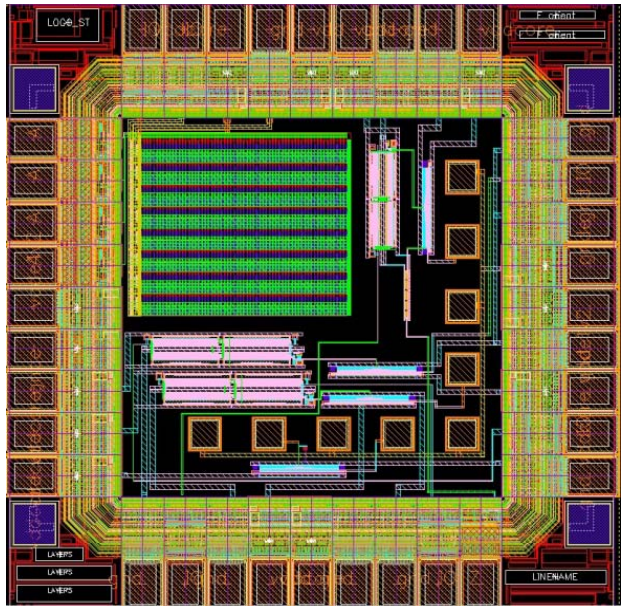
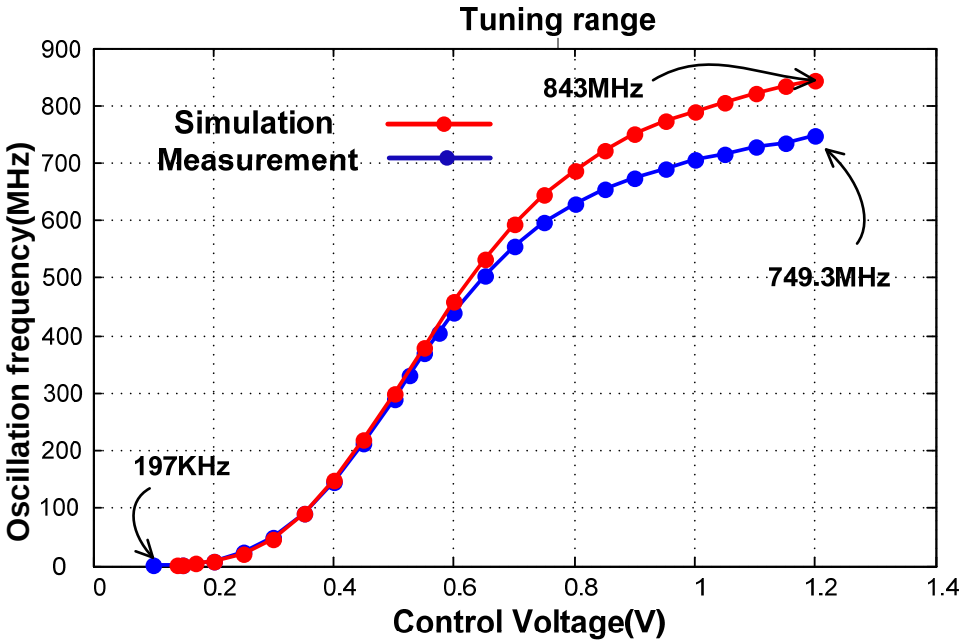
Measurement results

- **Tuning summary**
  - One design example has been fabricated on a 120nm process
  - Process model inaccuracies account for reduction in measured frequency.

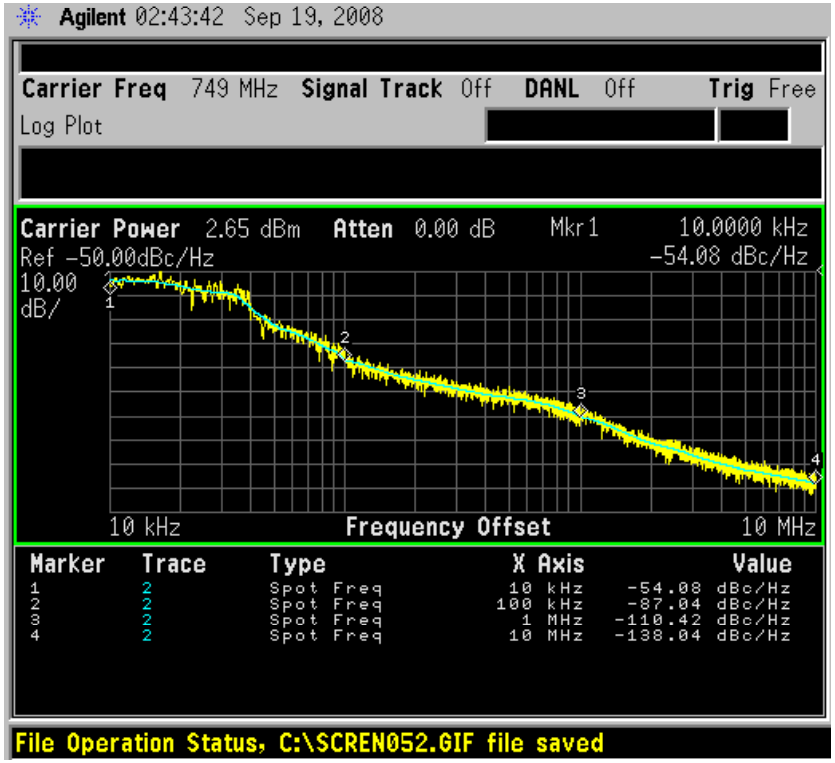
Specification:	Design Example 1
Supply voltage	1.2V
Process	120nm
Frequency range (measurement)	197KHz-749MHz
Size	249μm×57μm

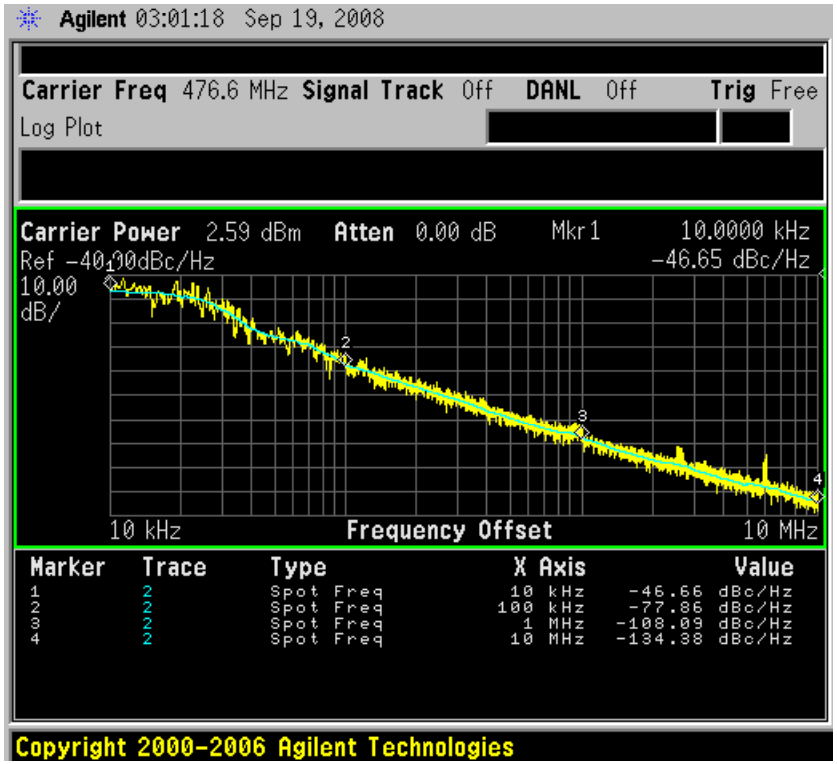




Measurement results

- **Phase Noise measurements**





L(f)=-87dBc@100KHzoffset from 749MHz

L(f)=-77.9dBc@100KHzoffset from 477MHz

Measurement results

- **Tuning voltage effect on phase noise**
  - Results at 100KHz offset from carrier
  - Measured results compare well with improved model

Control Voltage Vninst(V)	Oscillation frequency f_0(MHz)	Theoretical Phase Noise (dBC/Hz)	Measurement Phase Noise (dBC/Hz)
1.2	749	-86.775	-87.04
0.97	688.1	-83.9935	-84.45
0.74	573.2	-79.5658	-79.45
0.65	476.6	-76.8662	77.85

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Conclusions

- We have demonstrated that VCO tuning voltage does has an impact on phase noise performance.
- Existing phase noise models for differential delay cells have been extended to include this factor.
- The improved phase noise model has been shown to hold true over a large design space.
- Silicon prototype results indicate that the model can accurately predict the phase noise results.
- The proposed model has been built into a matlab model to reduce the design time of delay cell based VCOs.

Questions?

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Measurement results

- **Jitter summary**

Specification:	Design Example 2			
Supply voltage	1.2V			
Process	0.13μm(St120nm)			
Frequency range	197KHz-749MHz			
Size	249μm×57μm			
Jitter (Measurement)	749MHz	RMS	2.41ps	0.18% of period
		P-P	20.49ps	1.5% of period
	505MHz	RMS	1.95ps	0.099% of period
		P-P	16.96ps	0.84% of period
	48.1MHz	RMS	8.75ps	0.042% of period
		P-P	84.26ps	0.4% of period
Power	749MHz		≈24mW	
	505MHz		≈15.6mW	
	48.1MHz		≈2.98mW