Implementation of Optical Response of Thin Film Transistor with Verilog-A for Mobile LCD Applications

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Outline

- Background
- Model
- Model Evaluation
- Application
- Conclusion

Background

Background

Liquid Crystal Displays (LCDs) have become widely used in our daily life

Portable Game

Digital Still Camera (DSC)

Portable Music Player

T V

Personal Digital Assistance (PDA)

Portable DVD Player

Mobile Phone (MBL)

Personal Computer (PC)

Background

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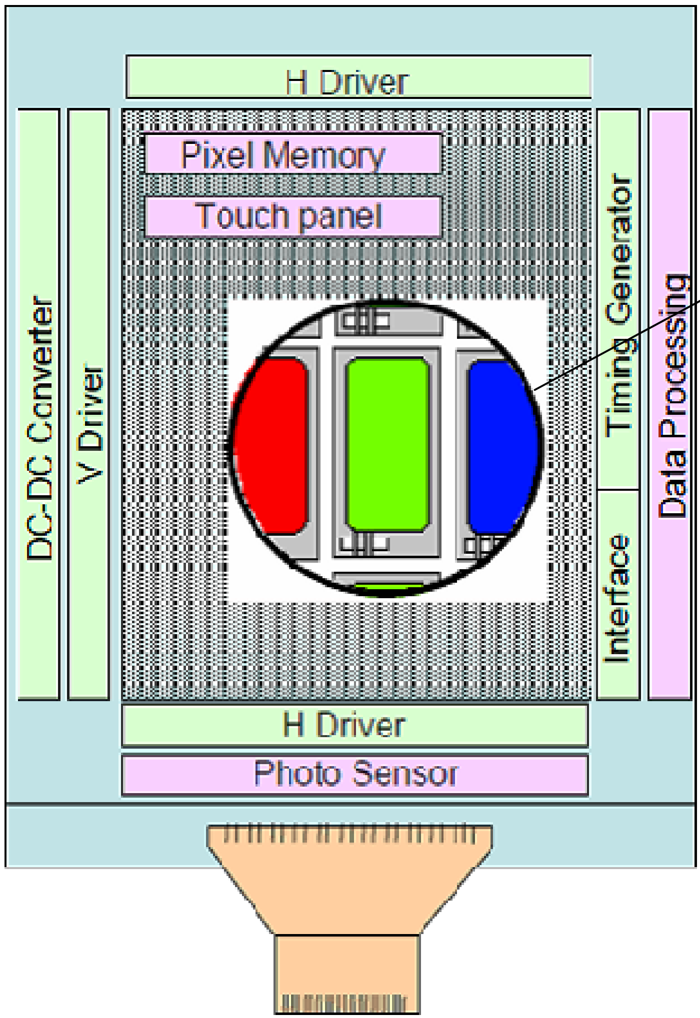
Expectations for LCDs

- High Image Quality
  - High contrast
  - Fast response
  - Low power consumption
  - Image uniformity, etc…
- Compact in Design
  - Narrow Frame
  - Thinner profile, etc…
- Inexpensive in Price

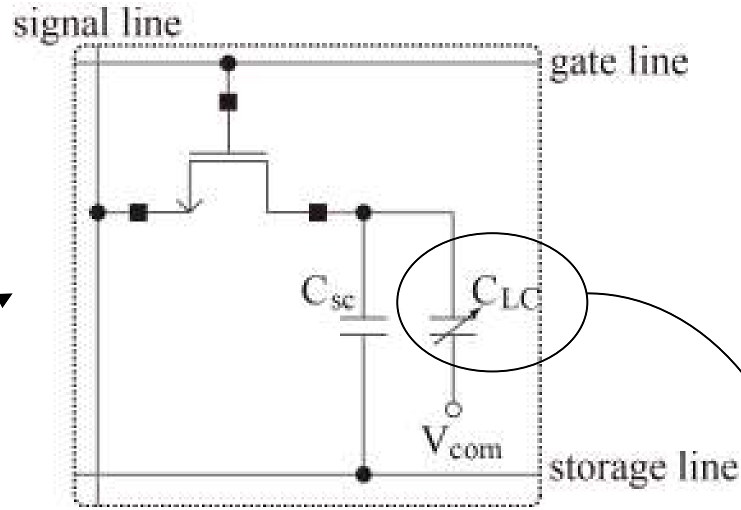
More accurate and fast simulation is in demand

Background

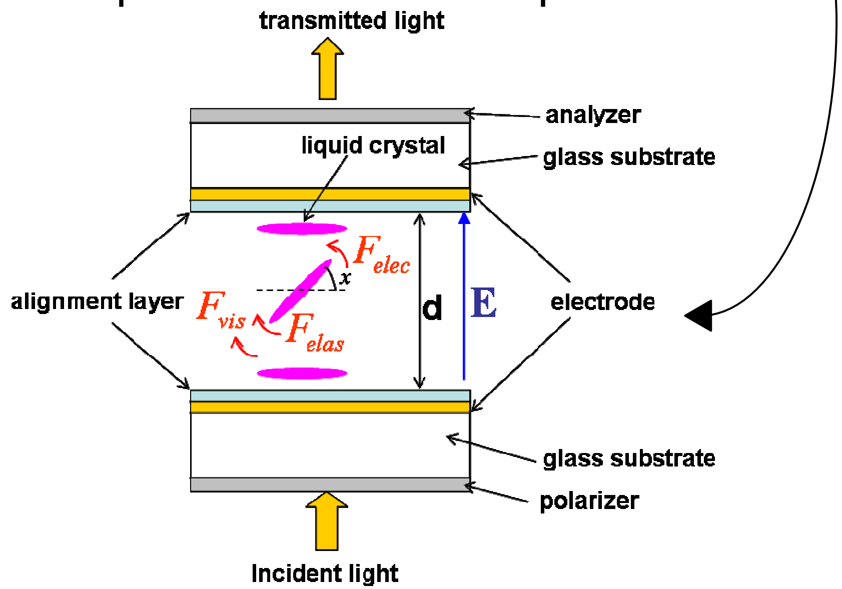
☐ Operation of general LCDs



Block diagram of typical LCD



Equivalent circuit of a pixel

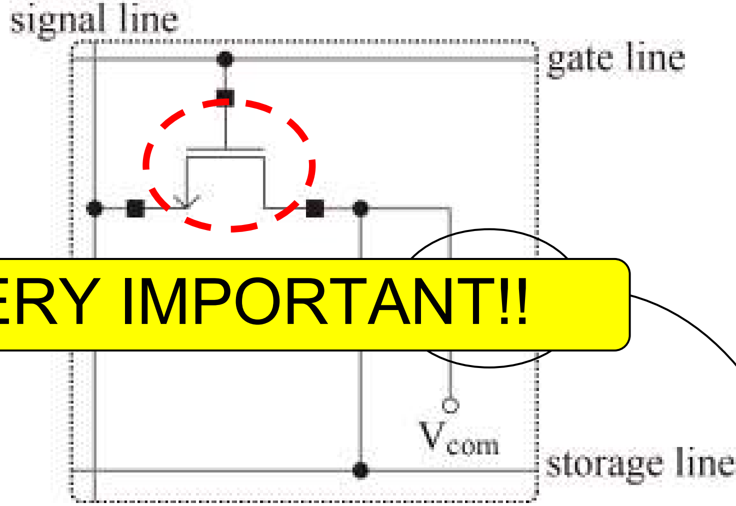


Cross sectional view of LC cell

Background

□ Operation of general LCDs

VERY IMPORTANT!!



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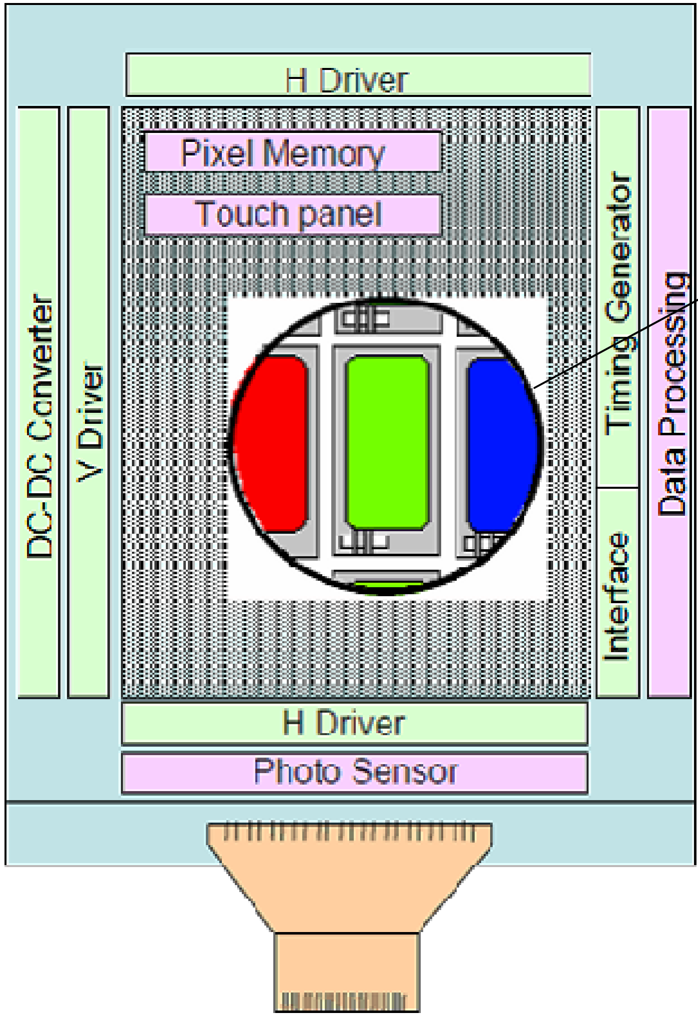

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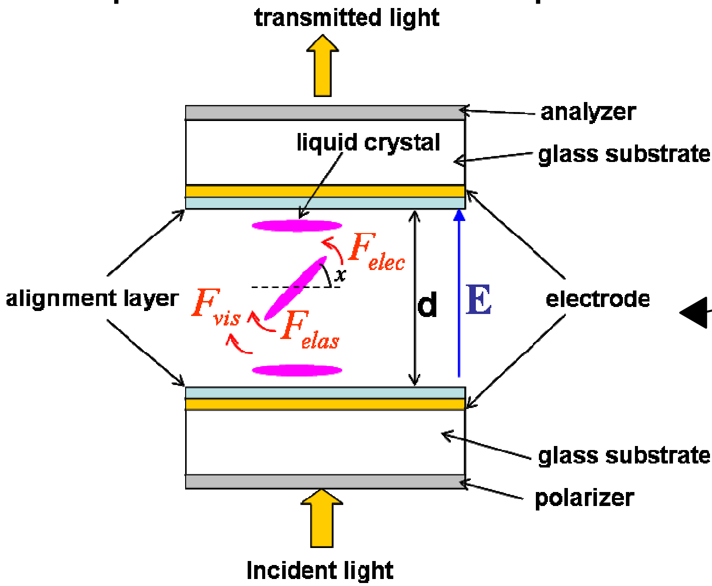
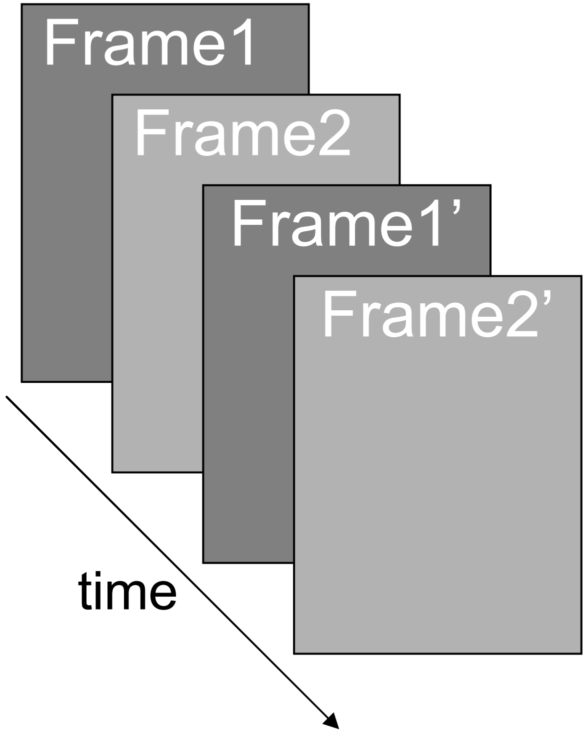


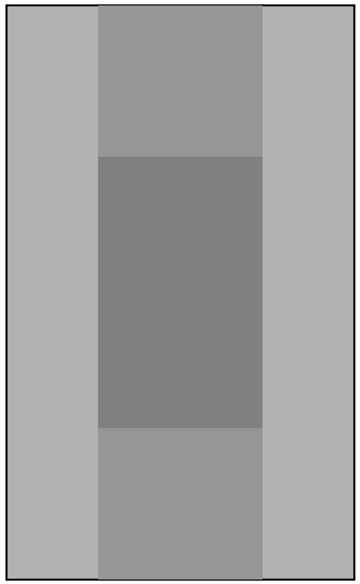
Cross sectional view of LC cell

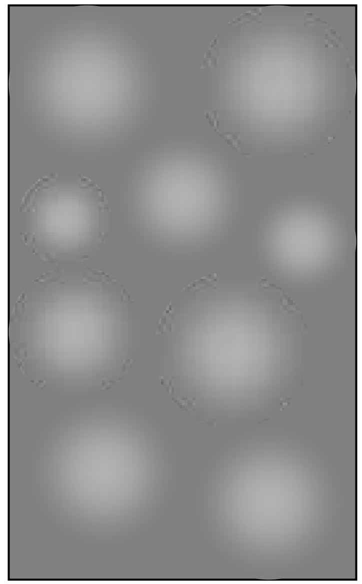
Background

☐ Issues for the display quality in LCDs (1)

Possible defects of display quality







Flicker | Vertical Cross-talk | Un-uniformity

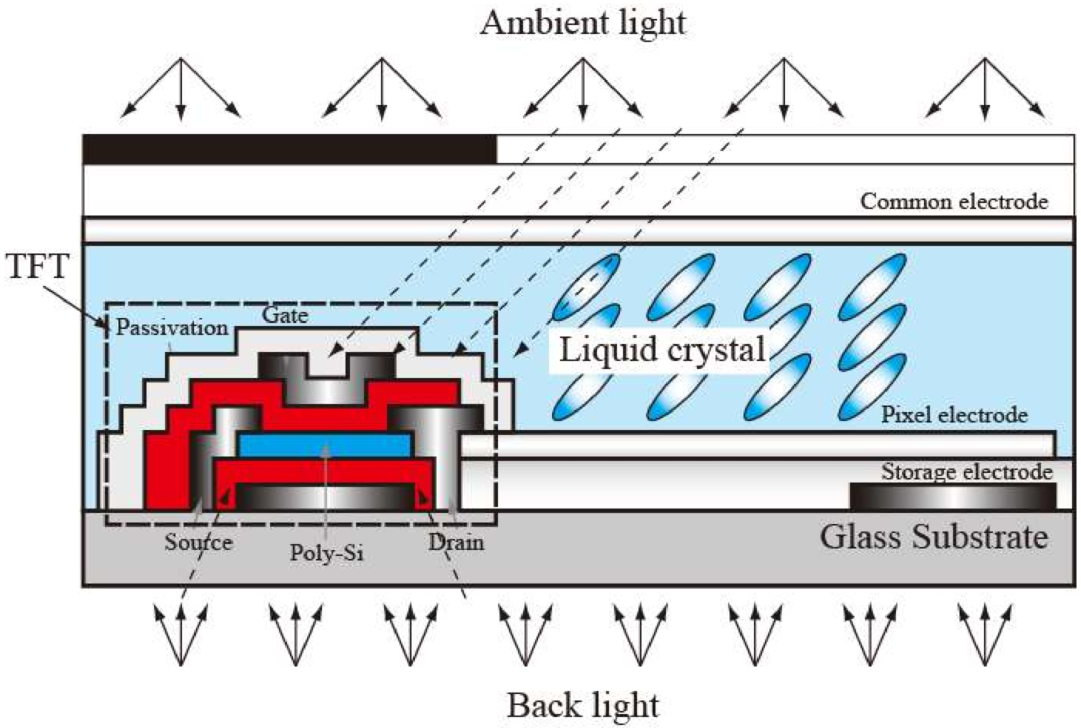
Cause of the malfunctions

"Photo-Leakage Current"

Background

Issues for the display quality in LCDs (2)

- TFTs are constantly under the influence of the light.
- They are required to maintain voltage for a long time.
- The effect of photo-leakage is significant.



Cross sectional view of a pixel

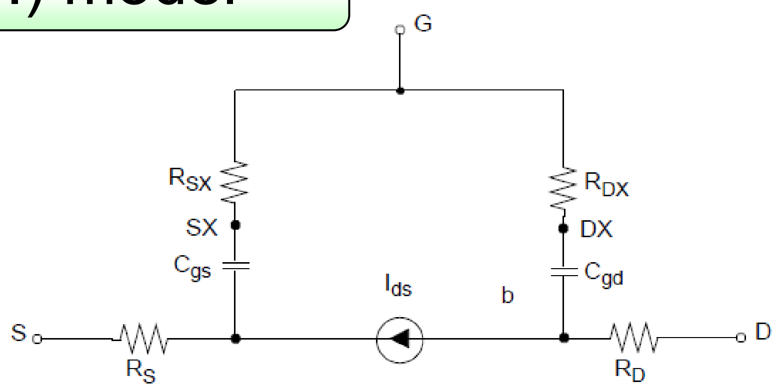
Circuit analysis considering the effect of the light is strongly in demand.

Background

□ Device model for TFT

Rensselaer Polytechnic Institute (RPI) model

- Popular TFT device model
- Accurately expresses TFT device characteristics



An equivalent circuit for RPI model

Ways to include an optical response

- Modify a proven device model

  ⇨ models provided by EDA venders are not opened for modification

- Develop an original device model

  ⇨ takes too much time!!

B. Iniguez *et al*. Unied model for short-channel poly-si tfts. Solid-StateElectronics, 43:1821-1831, 1999.

Background

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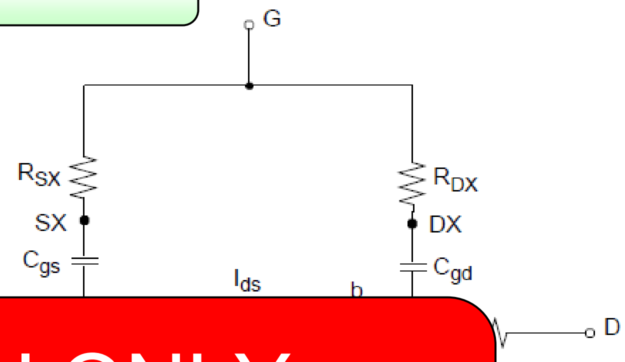

model

Use Verilog-A to model ONLY
an optical response of TFT

Ways

- Modify a proven device model
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  - ⇨ takes too much time!!

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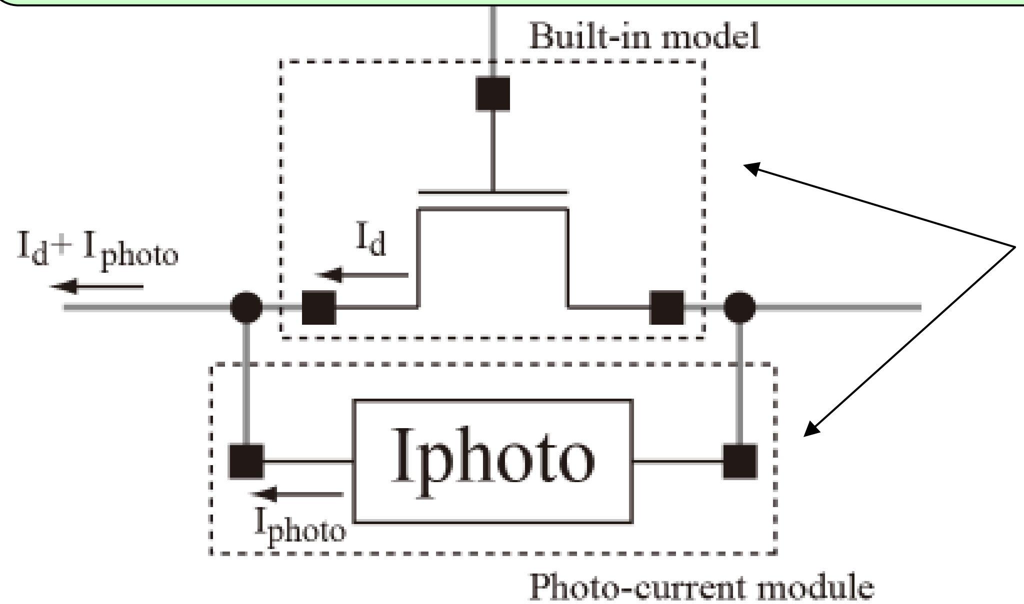
Model

Model

Proposed method

Connect photo-current module as an EXTERNAL instance of the RPI model



Transistor model and Photo-Current Module are connected in parallel.

Condition to be met

Photo-leakage current needs to be modeled as independent of characteristics calculated by the RPI model

Model

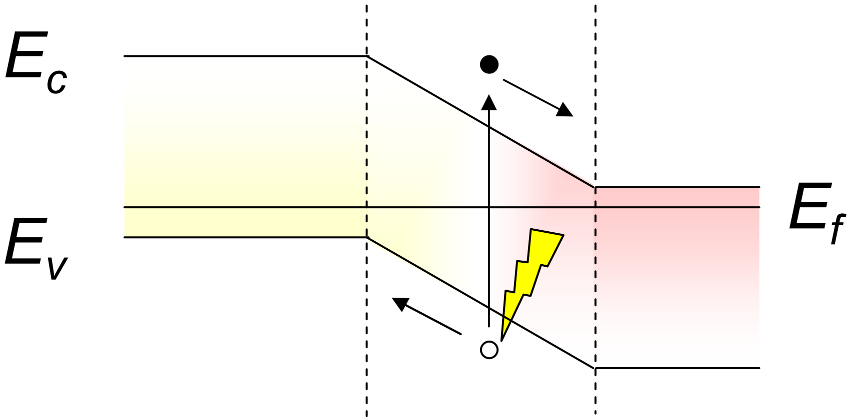
☐ Two generation paths of photo-carriers

① Inside the depletion region.

- Carriers separated by the field.

⇨ Drift component.

- Not in the RPI model.
- Empirically known to be dominant.

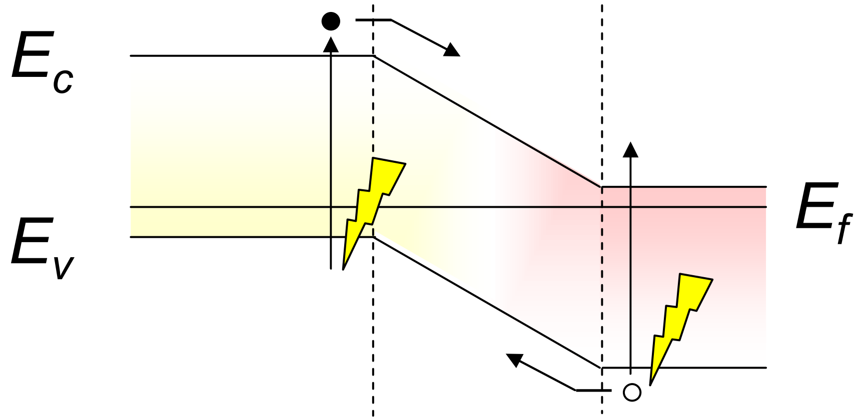


② Outside edge of the depletion region.

- Originated from the diffusion.

⇨ Diffusion component.

- Empirically known to be less dominant.



Model

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① Inside the depletion region.

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⇨ Drift component.

- Not in the RPI model.
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② Outside edge of the depletion region.

- Originated from diffusion

IGNORED

- Empirically known to be less dominant.

Photo-leakage current is assumed as an independent current of the RPI

Model

□ Generation inside the depletion region

- Photo-generation rate G ($s^{-1}cm^{-3}$)

$$G(x) = \int_{\lambda_{\min}}^{\lambda_{\max}} \alpha(\lambda, x)\Phi(\lambda, x)e^{-\int_0^x \alpha(\lambda, x)dx} d\lambda$$

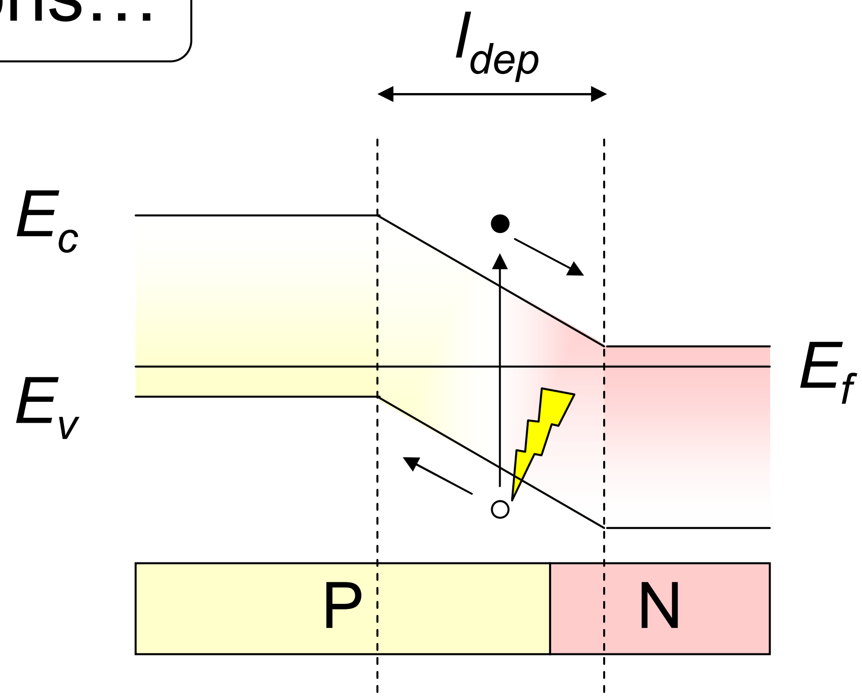
$$G = \frac{P_{in}\alpha}{h\nu}$$

assumptions…

- Photo-leakage current in the depletion region I_{photo} (A)

$$I_{photo} = qt_{Si}wl_{dep}G$$

$$l_{dep} = \sqrt{\frac{2\varepsilon_{Si}(N_a + N_d)(\phi_{bi} + V_{ds})}{qN_aN_d}}$$



C. Amano *et al.*, Fabrication and numerical analysis of algaas/gaas tandem solar cells with tunnel interconnections. IEEE Trans. Electron Devices, 36:1026-1035, 1989.

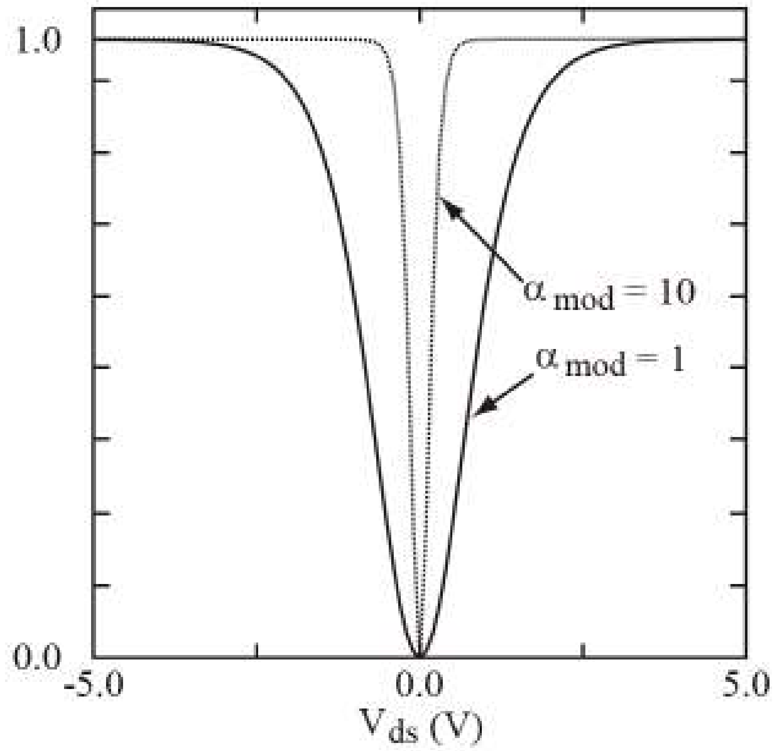
Model

Convergence issues

SPICE is based on Ohm's Law

When V_{ds} is 0 V, I_{ds} should be 0 A.

$$I_{photo_{mod}} = I_{photo} \tanh^2(\alpha_{mod} V_{ds})$$

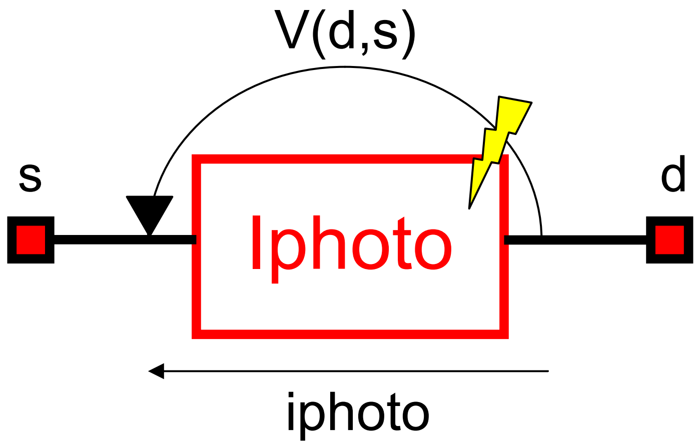


$\tanh^2(\alpha_{mod} \times V_{ds})$

Convergence is greatly improved by introducing tanh

Coding in Verilog-A

□ Excerption of the code




```
// Verilog-A for Photo-leakage current module

module iphoto(d, s);
inout d, s;
electrical d, s;
...
analog begin
begin
 if (V(d, s) >= 0.0) begin
  mode = 1;
  vds = V(d, s);
 end
 else begin
  mode = -1;
  vds = -V(d, s);
 end

 if (acm == 0)
  weff = w * scale;
 else if (acm == 1)
  weff = (w * scale * wmlt + xw - 2 * wd
* scale);

...
 ldep = sqrt(2.0 * `EPSILON_SI * (eb + vds)
/ (`Q_E * na * nd) * (na + nd));
...
  iphoto = `Q_E * tsi * weff * ldep *
(brightness * alpha) / (`H * `C / lambda);

  iphoto = iphoto * pow(tanh(alphamod
* vds), 2);

 if (mode > 0)
  I(d, s) <+ iphoto;
 else
  I(d, s) <+ -iphoto;

end
end
endmodule
```

Model Evaluation

Model Evaluation

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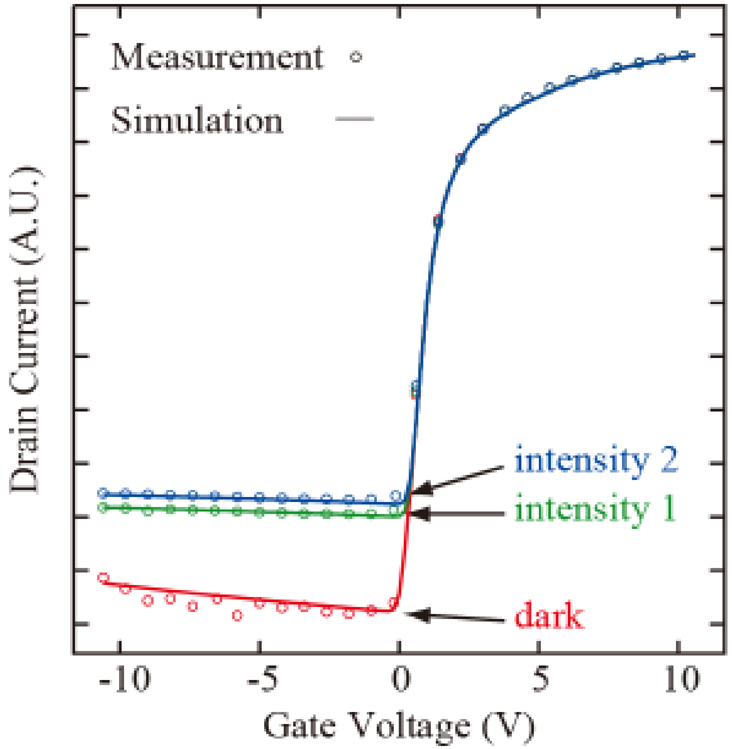
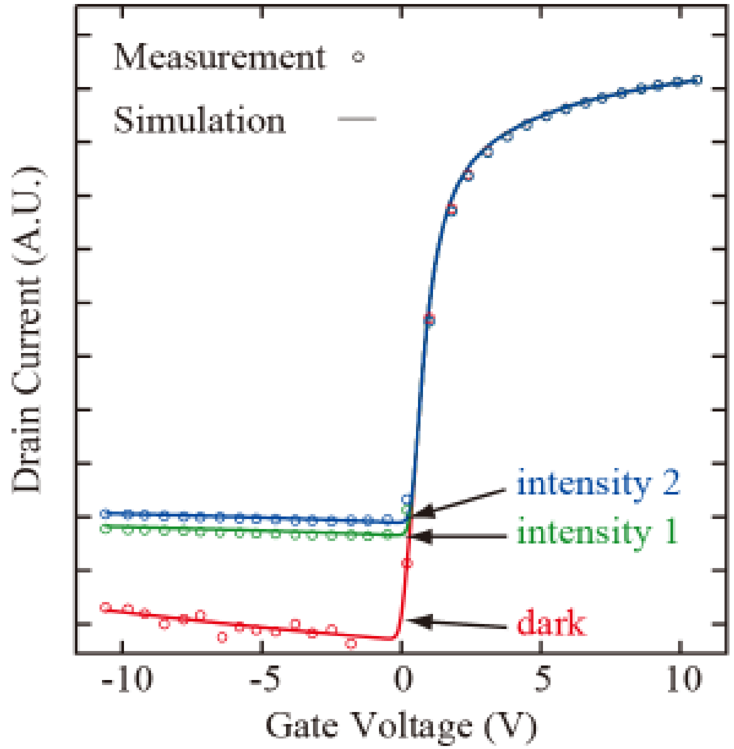
□ Validity

Intensity	TFT 1	TFT 2	Avg. Error
Intensity 1	1.23 %	5.68 %	5.33 %
Intensity 2	9.43 %	3.11 %	4.40 %



(1) TFT 1



(2) TFT 2

Good agreement with the experiment data

Model Evaluation

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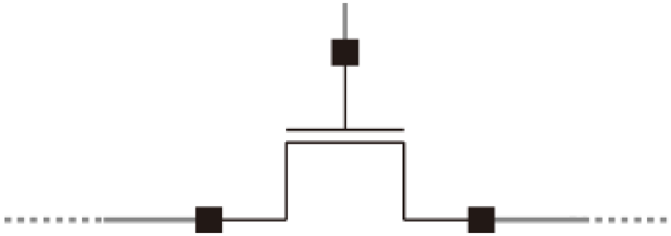
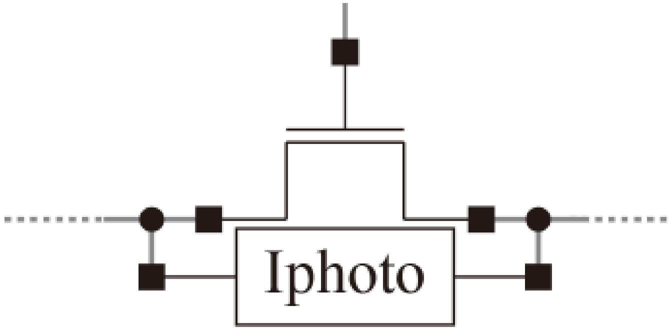
□ Simulation runtime

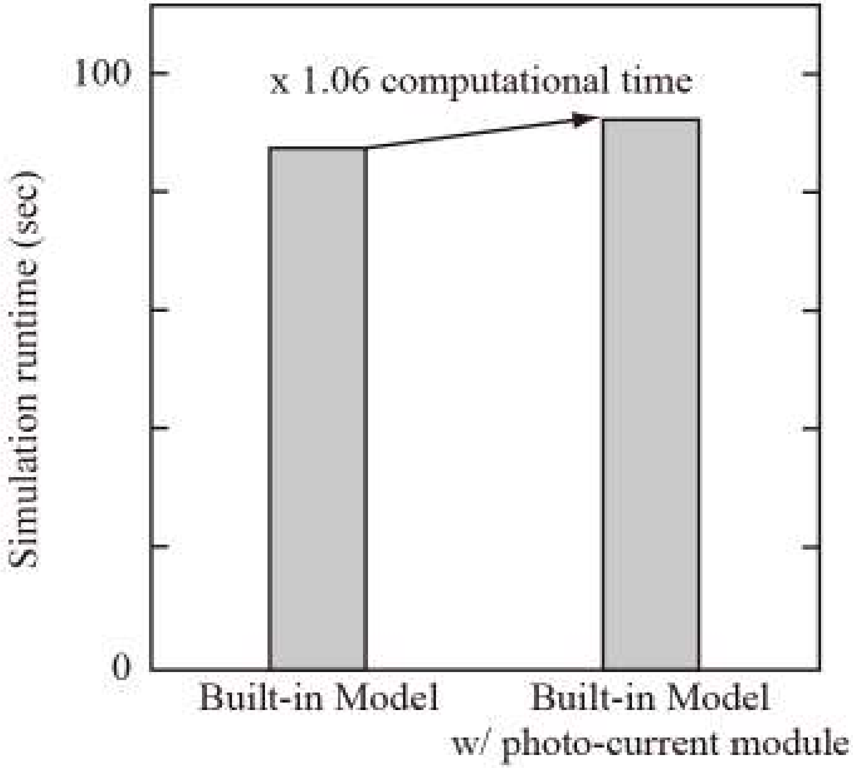
- 1001 pixels in series.
- Tran. analysis of 40 msec.



Built-in Model



Built-in Model w/ photo-current module



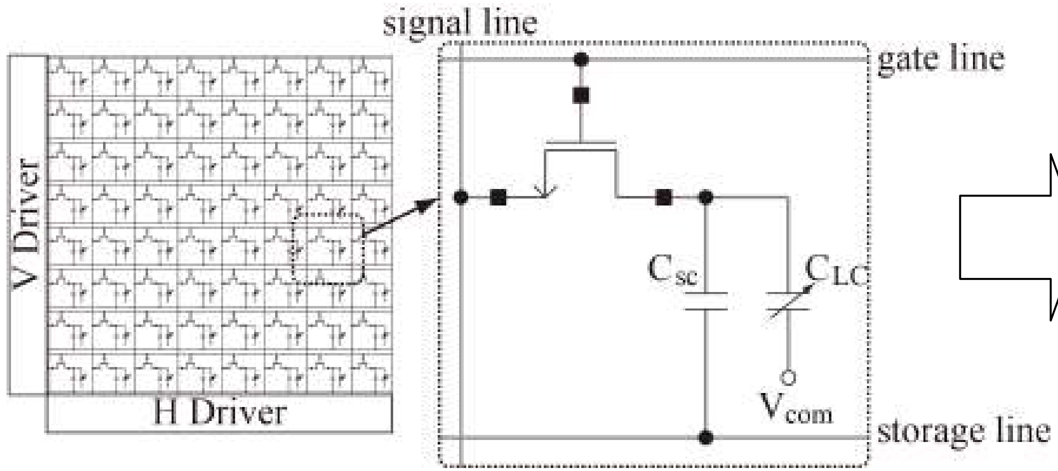
Simulation runtime comparison

Only 1.06 times more simulation runtime is consumed

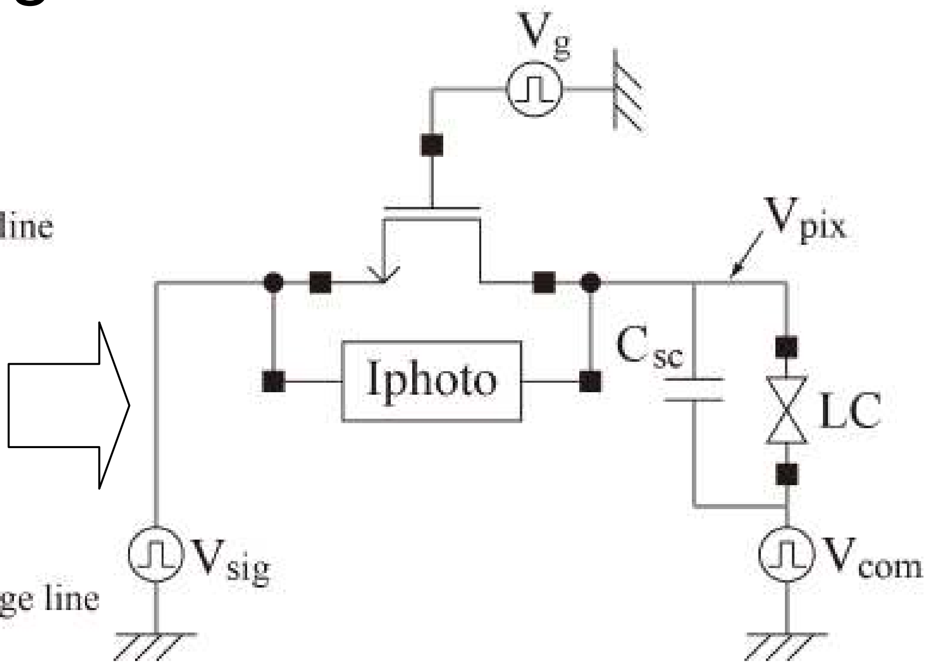
Application

Application

□ Application to the LCD design



Schematic diagram of LCD panel



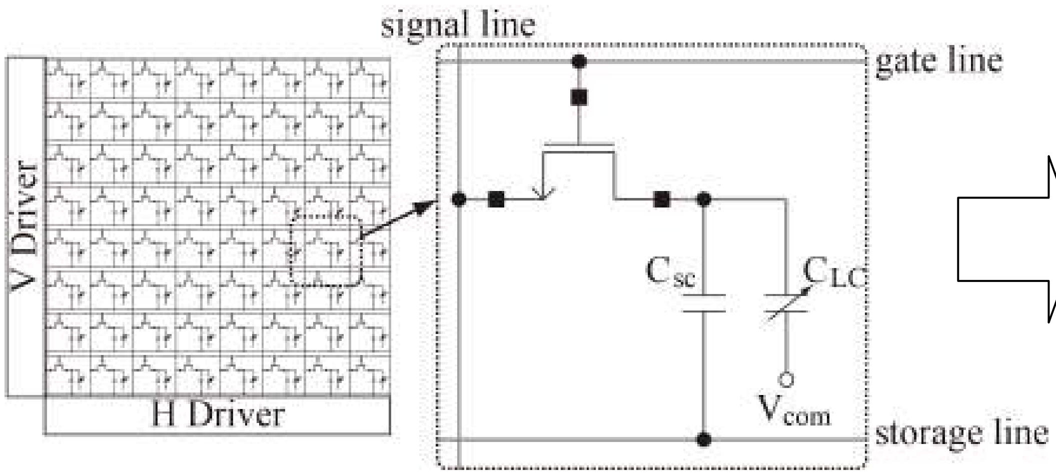
A typical pixel circuit of LCD

Photo-leakage current model and liquid crystal model described in Verilog-A are used

M. Watanabe *et al*. Macro-modeling of liquid crystal cell with veriloga. Proceedings of the 2007 IEEE International Behavioral Modeling and Simulation Workshop, pages 132-137, 2007.

Application

□ Application to the LCD design



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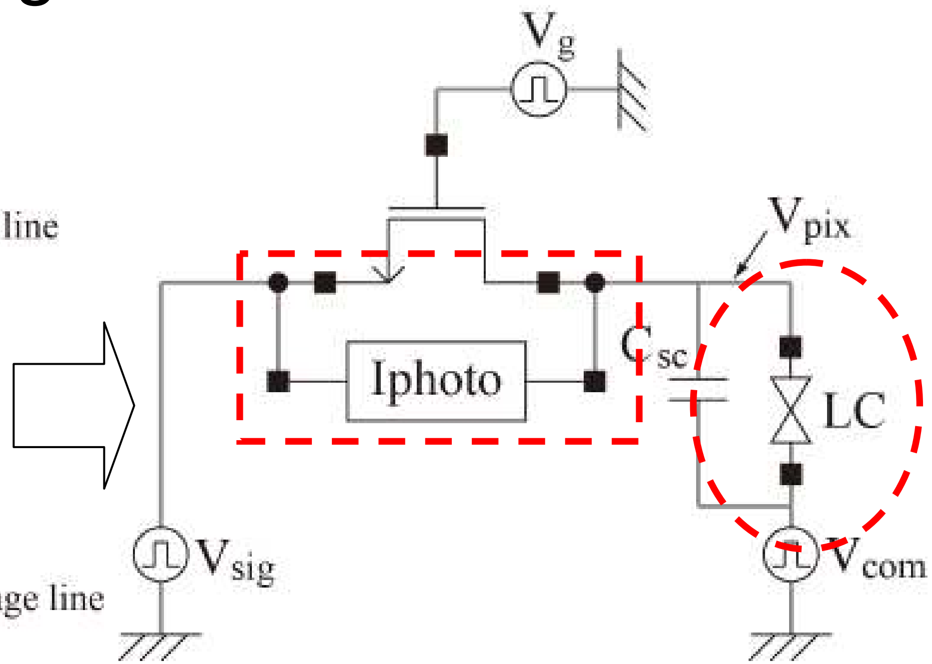

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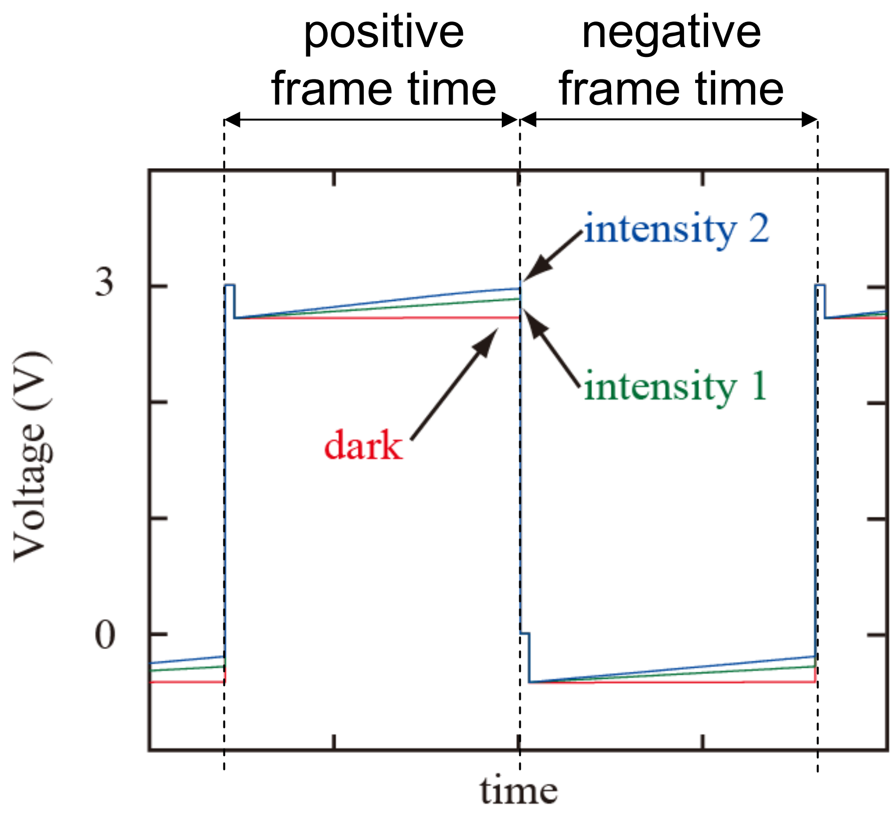
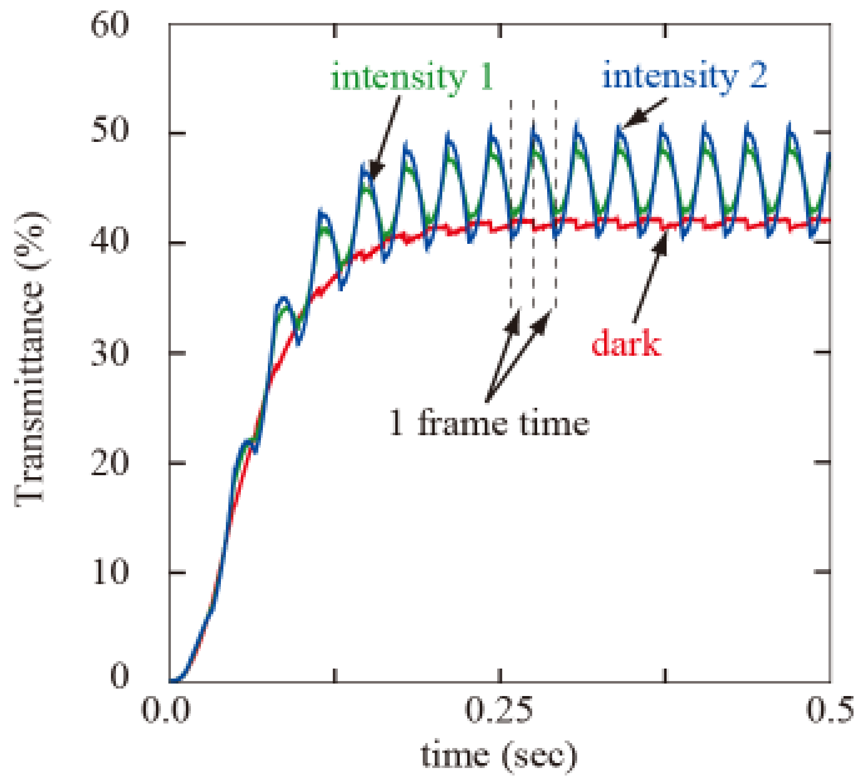


Transient characteristics of V_{pix}



Transmittance curve

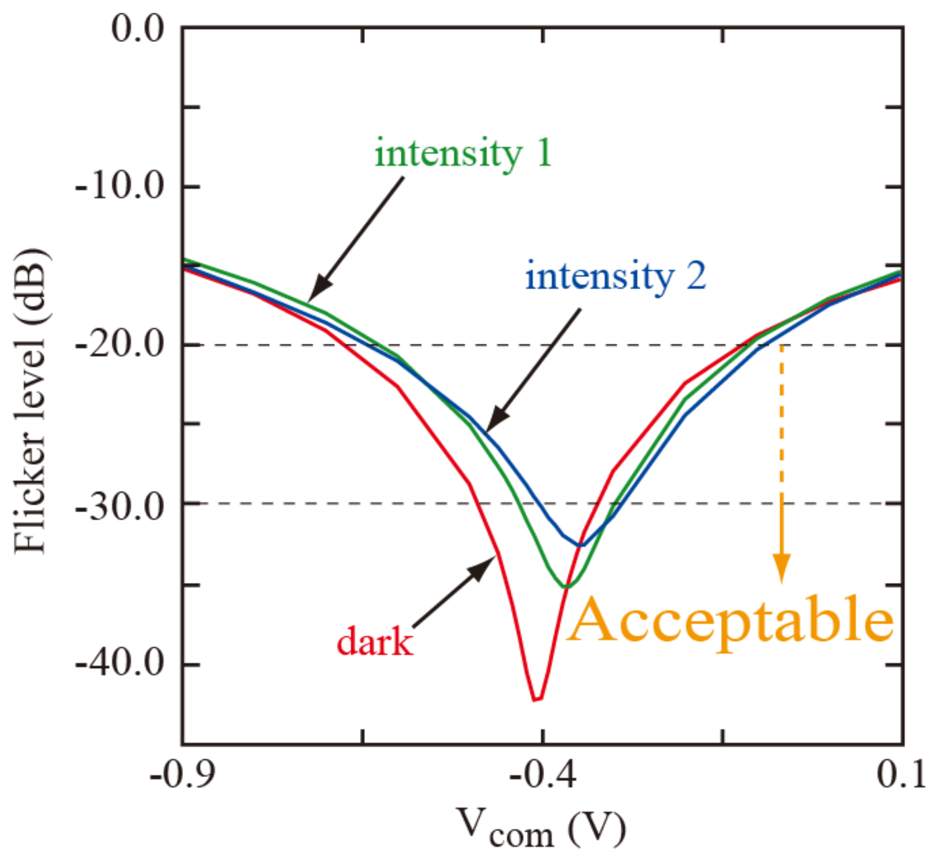
Following optimizations should be applied during LCD design processes

1. V_{com} optimization
2. C_{sc} optimization

Application

□ Optimization 1: V_{com}

- Flicker level increases with light exposure.
- Optimal V_{com} shifts with light intensities.
- Failure to optimize V_{com} may lead to flicker image.



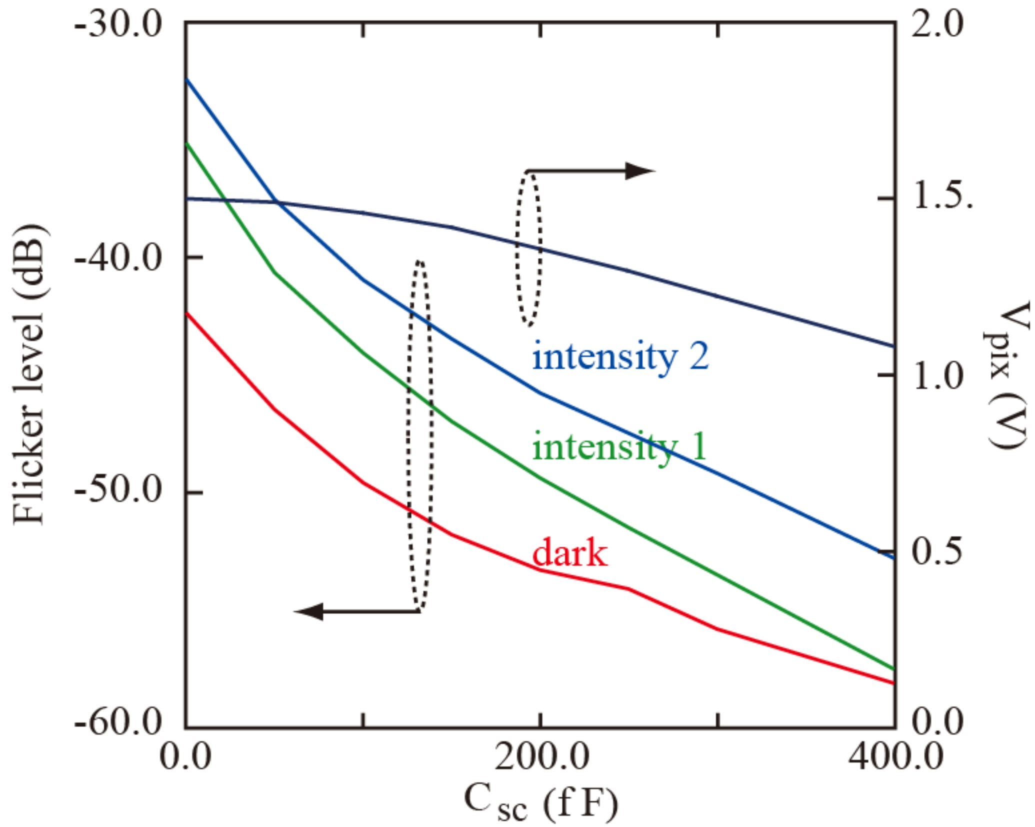
V_{com} should be ~-0.35 V

Designers can estimate the optimal V_{com} for supposed light intensities

Application

☐ Optimization 2: C_{sc}

- As C_{sc} is increased
  ⇨ flicker level is decreased
  BUT…
  ⇨ less aperture ratio
  ⇨ hard to accumulate the charge during switch-on time



Choose max C_{sc} that fulfills customer's specification

Designers can estimate the optimal C_{sc} for supposed light intensities with given specification

Conclusion

- Realized accurate and fast simulation considering optical illumination.
- Enabled detection of possible malfunctioning in the LCD property during designing process.
- Verilog-A is suitable for this plug-in approach modeling.

Thank you for your attention