Flash Memory Cell Compact Modeling Using PSP Model

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Outline

- Motivation
- Background
- PSP-Based Flash cell model
- Characterization procedure
- Simulations
- Conclusions

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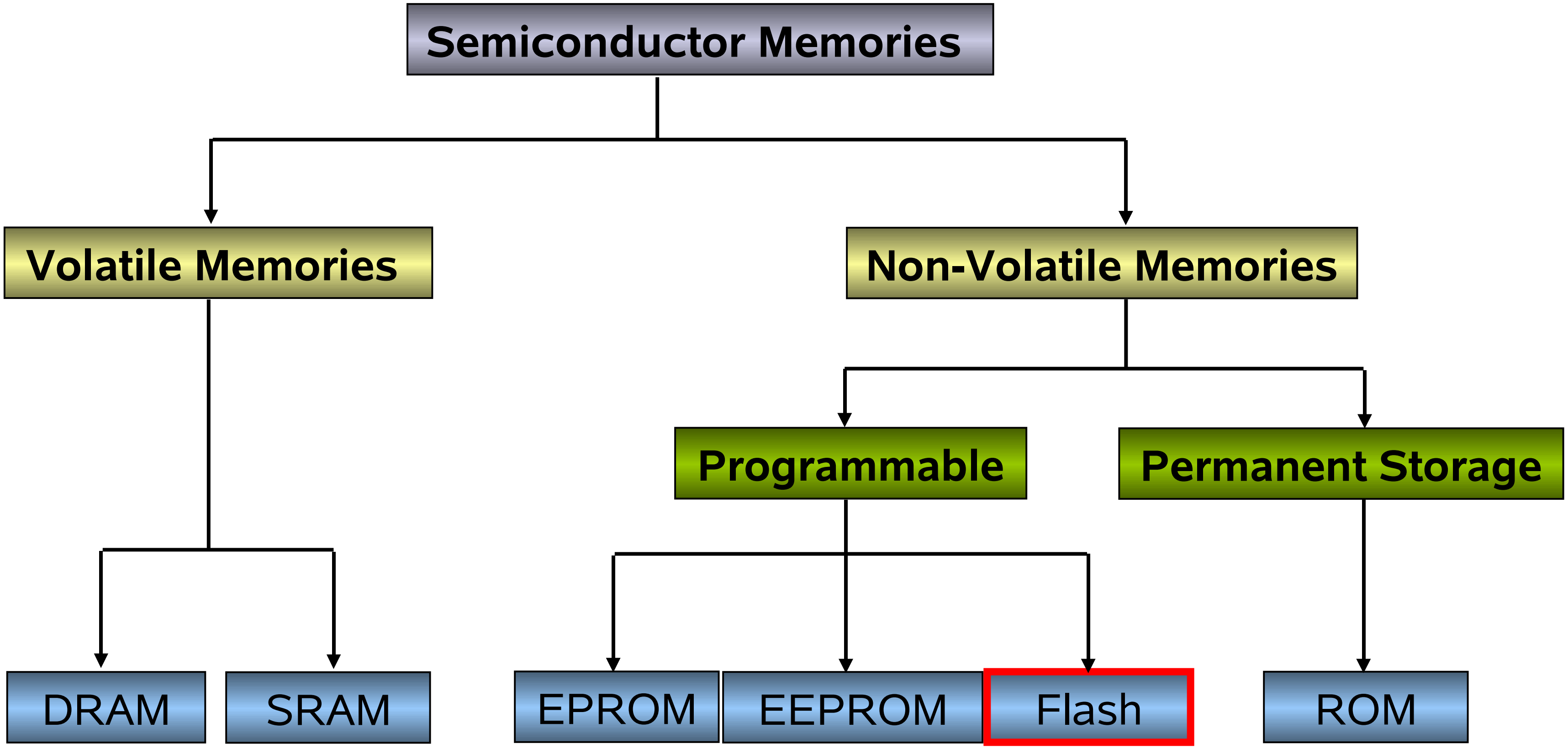
Motivation 1/4

Semiconductor memories classification



Semiconductor Memories

Volatile Memories

Non-Volatile Memories

Programmable

Permanent Storage

DRAM

SRAM

EPROM

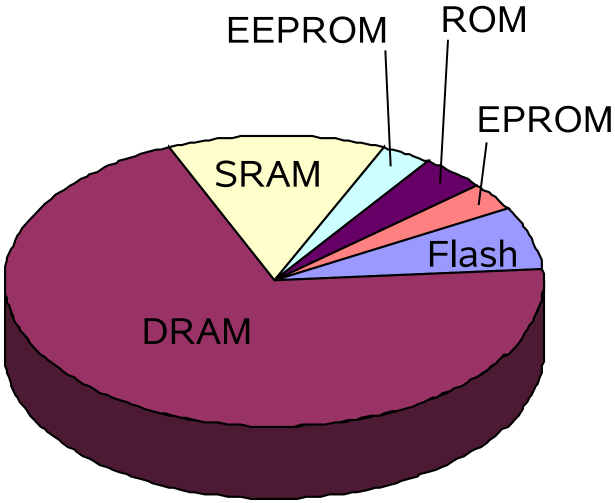
EEPROM

Flash

ROM

Motivation 2/4

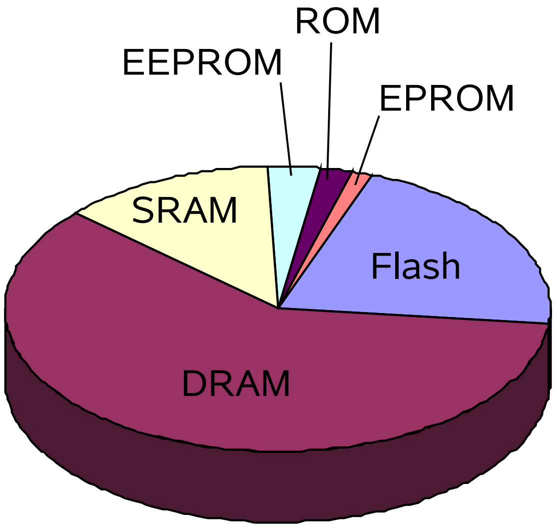
Semiconductor memories market



1996

Total : $36 billion

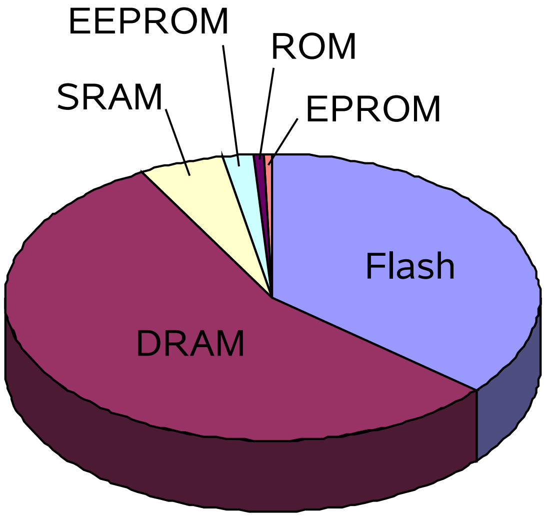
Flash → 7%



2000

Total : $49 billion

Flash → 21%



2006

Total : $61 billion

Flash → 36%

Motivation 3/4

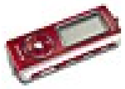
Flash memory cell applications

Memory cards

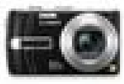
USB flash drives

Handheld computers

Digital audio players



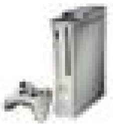
Digital still cameras



Digital video cameras

Cellular phones

Game consoles



Motivation 4/4

Flash memory cell for designers

- To integrate circuit simulators and to perform multi-cell simulations :
  > compact modeling approach
  > adapted and flexible language (Verilog-A)

- To include physical effects appropriate for small component :
  > based on an advanced description (PSP MOS model)

- Accurate electrical behavior for modern technologies:
  > complete characterization procedure

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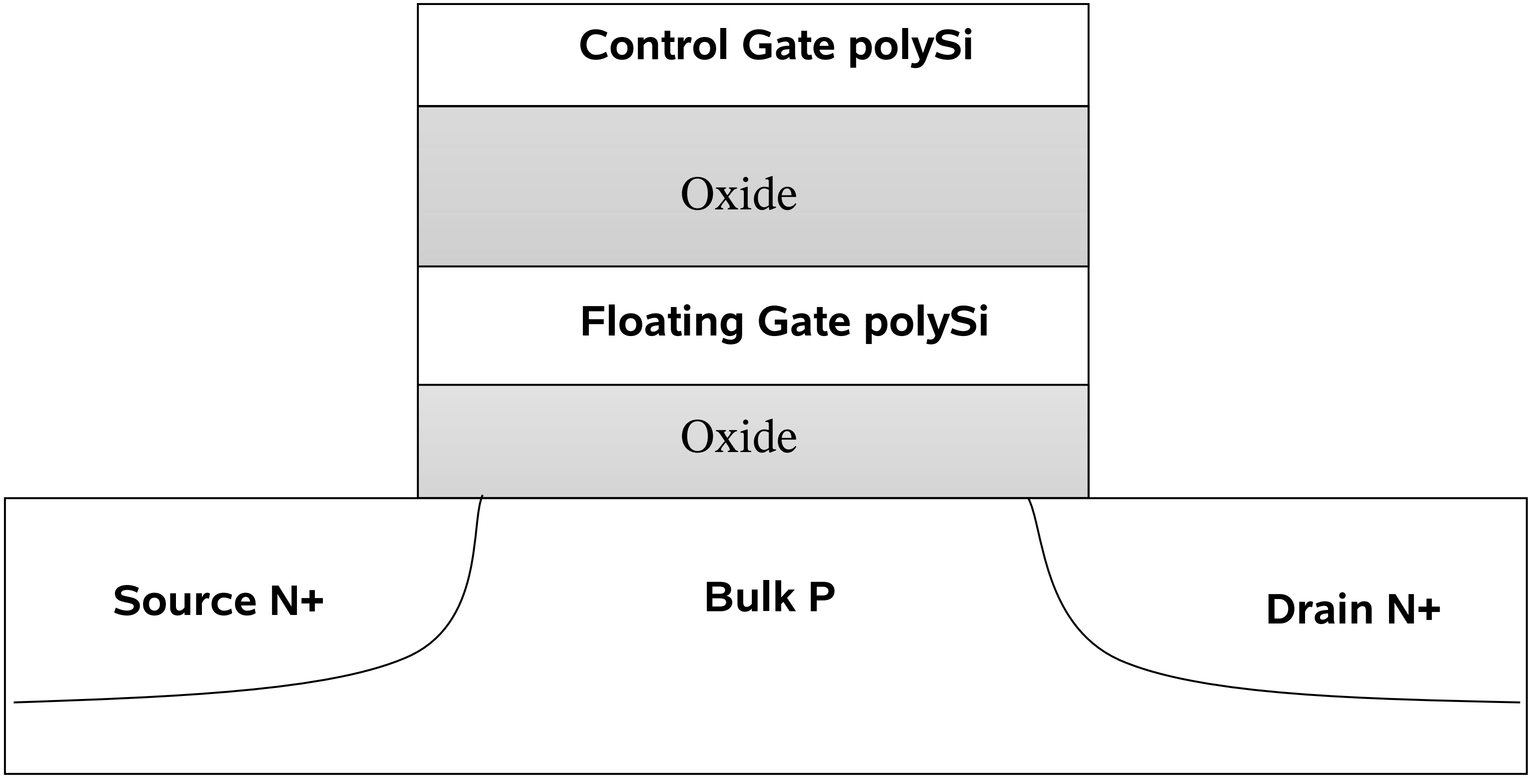
Background 1/4

Flash Memory Cell :

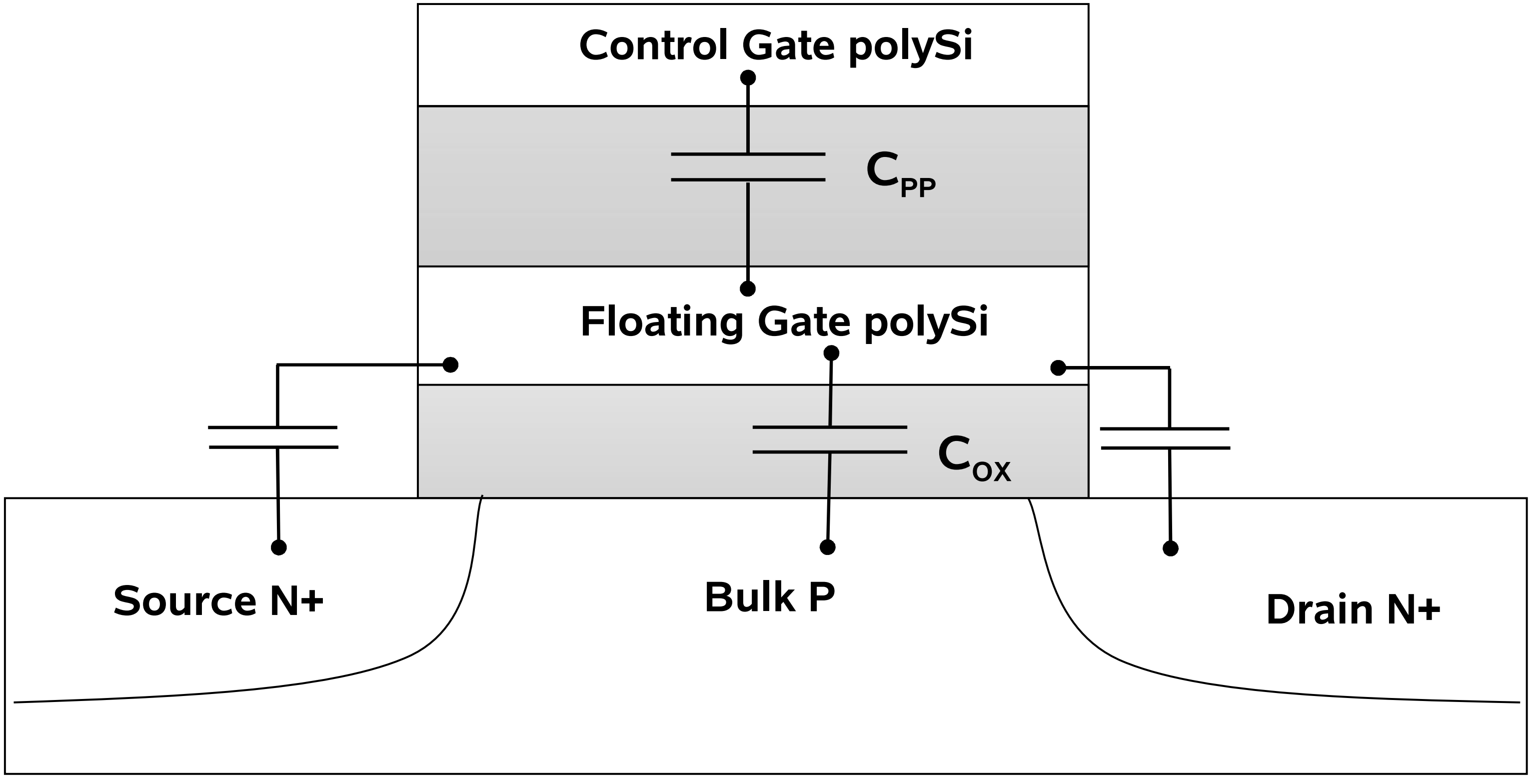
Capacitive structure and injection currents



Background 1/4

Flash Memory Cell :

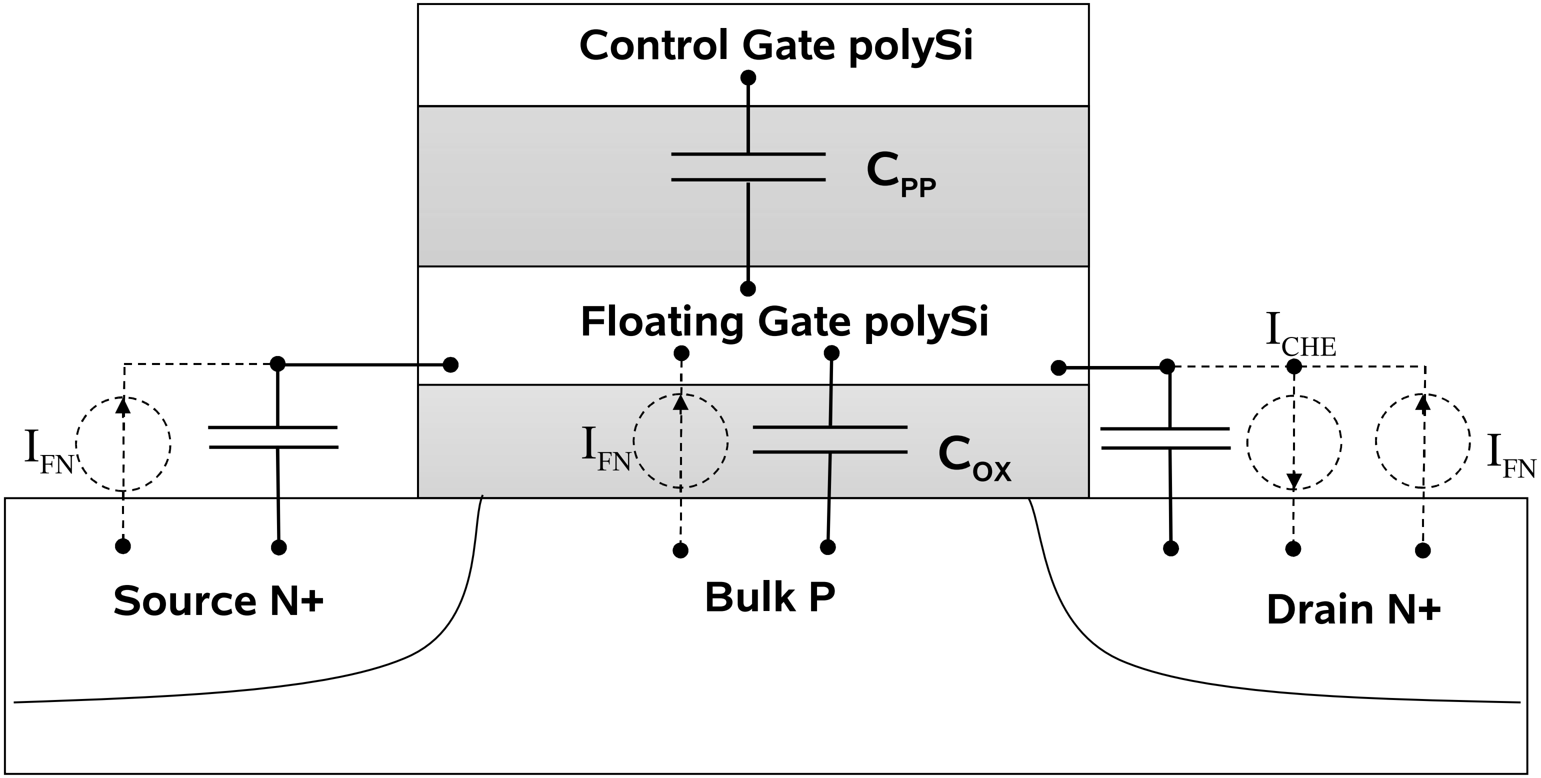
Capacitive structure and injection currents



Background 1/4

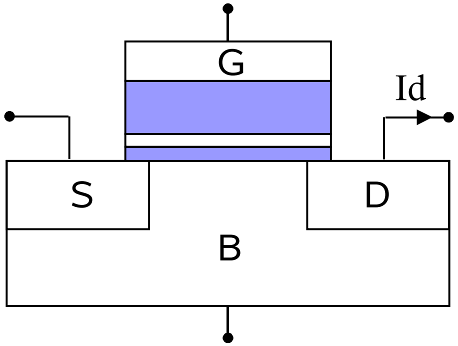
Flash Memory Cell :

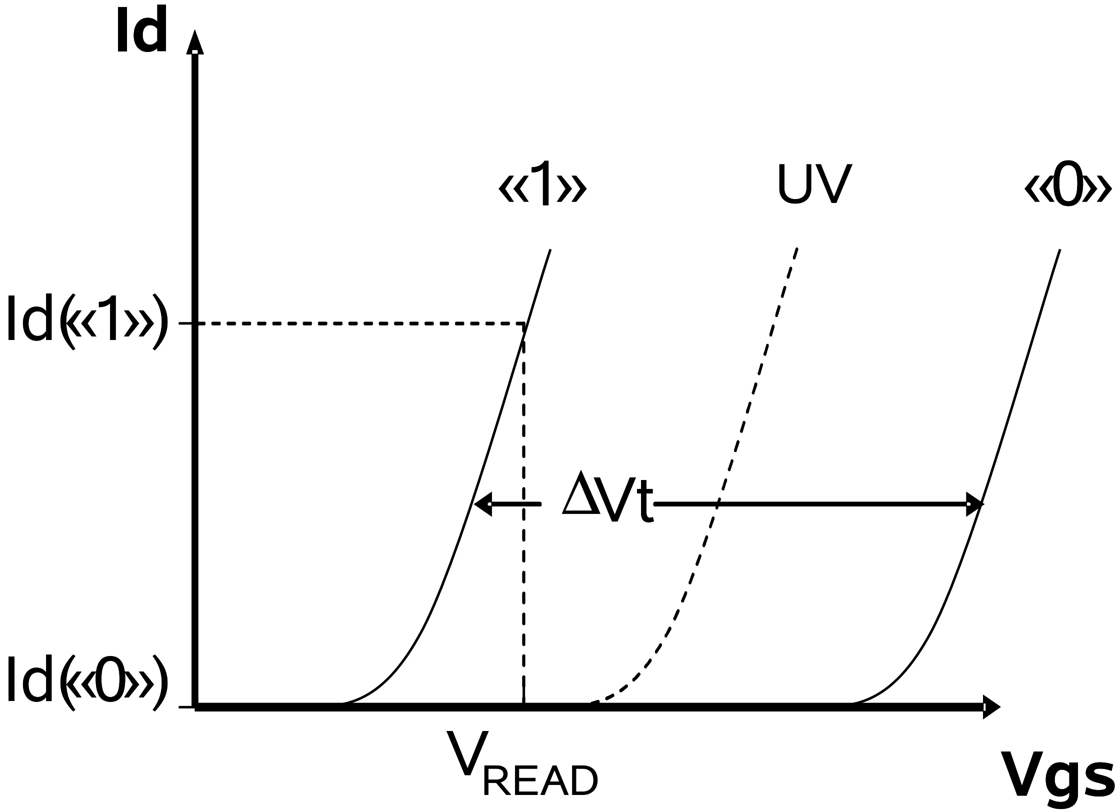
Capacitive structure and injection currents



Background 2/4

Erased and Programmed modes :



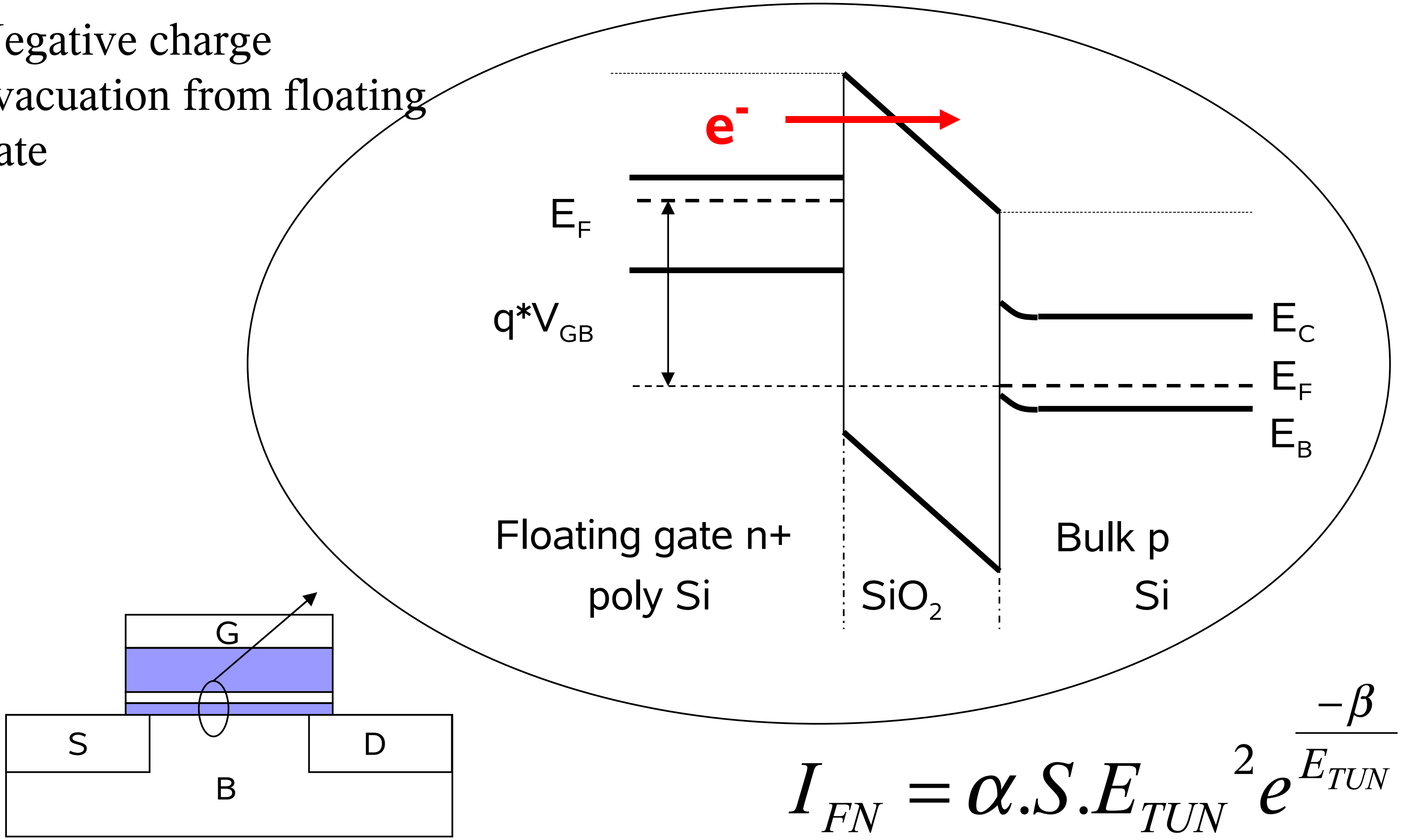


$$V_T = V_{TUV} - \frac{Q_{FG}}{C_{PP}}$$

Background 3/4

Injection Currents : Fowler-Nordheim tunneling

Negative charge evacuation from floating gate

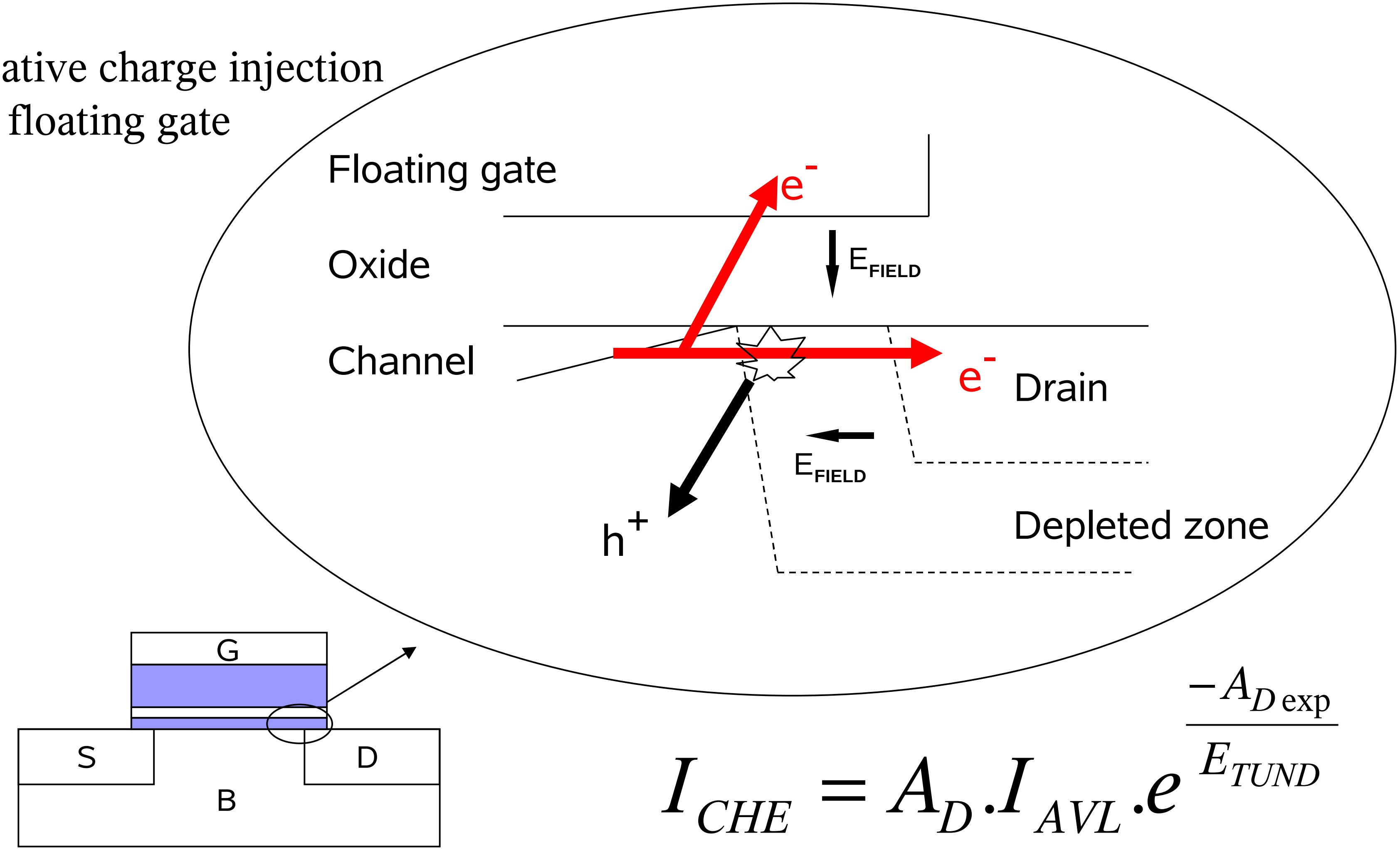


$$I_{FN} = \alpha.S.E_{TUN}{}^{2} e^{\frac{-\beta}{E_{TUN}}}$$

Background 4/4

Injection Currents : Channel Hot Electron current

Negative charge injection into floating gate



$$I_{CHE} = A_D . I_{AVL} . e^{\frac{-A_{D\,exp}}{E_{TUND}}}$$

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PSP-based Flash cell model 1/4

The PSP MOS model

- Developed by Philips Research and Penn State University. (first version 2006)
- Compact surface-potential based model.
- Relevant physical effects (mobility reduction, velocity saturation, DIBL, GIDL…)
- Source/Drain junctions are described using the JUNCAP2 diode model.
- Possibility of including temperature and geometrical scaling rules.

PSP-based Flash cell model 1/4

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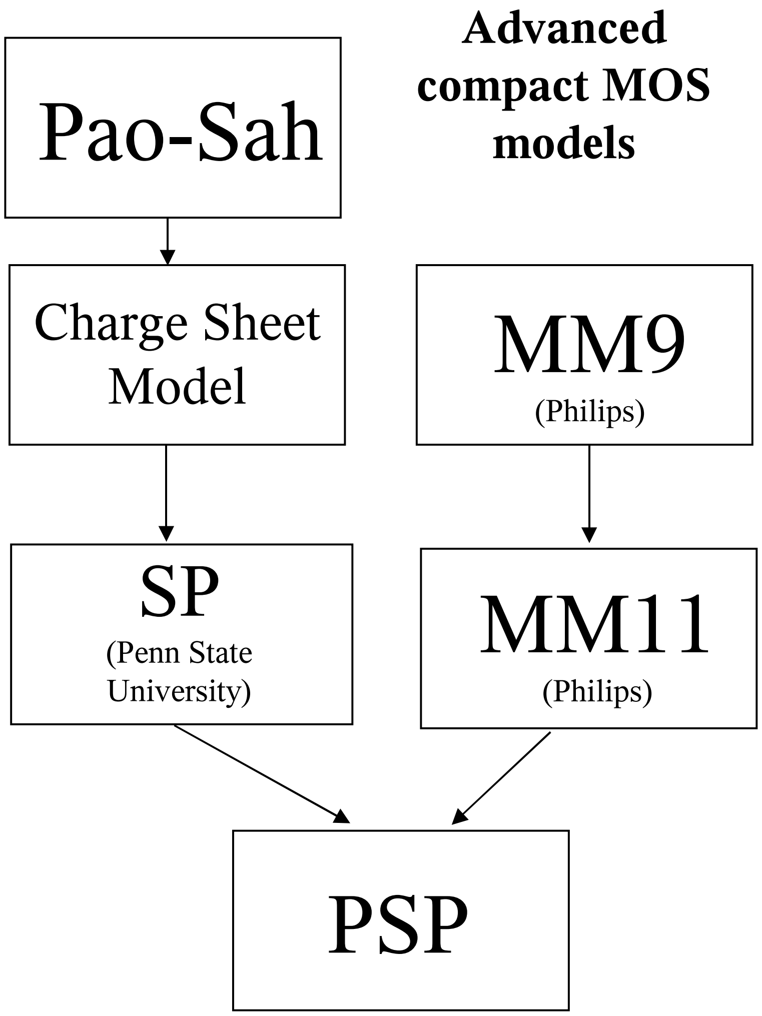


Advanced compact MOS models

Pao-Sah

Charge Sheet Model

SP
(Penn State University)

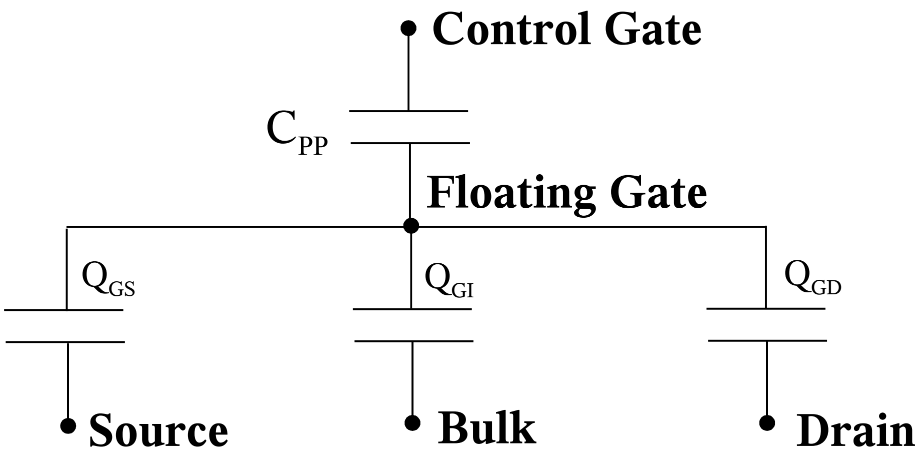
MM9
(Philips)

MM11
(Philips)

PSP

PSP-based Flash cell model 2/4

Addition of the C_{PP} capacitor using a charge neutrality equation



- Q_{GI}, Q_{GS} and Q_{GD} values are calculated by PSP model.
- They depend on V_{FG}, V_B, V_S and V_D (Equivalent MOS electrodes).

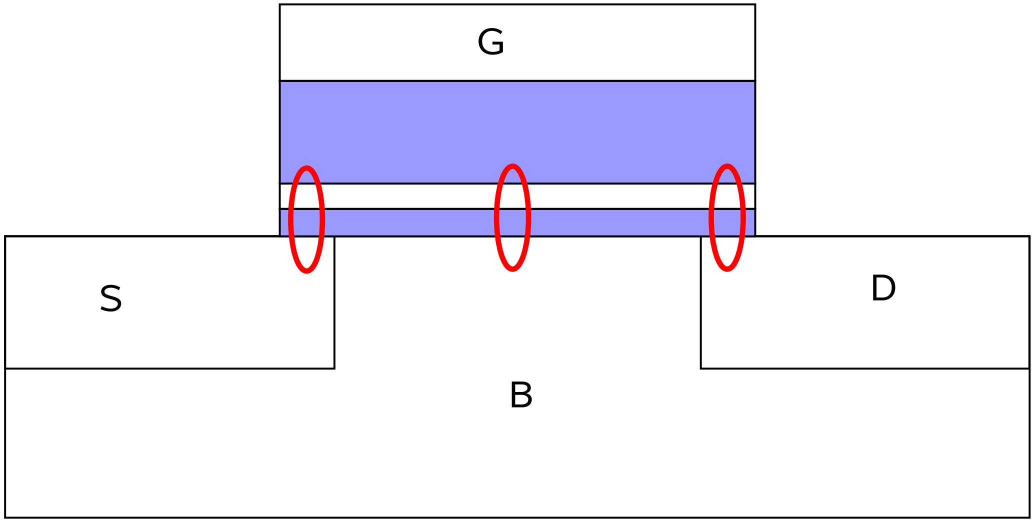
$$Q_{FG} = Q_{GI} + Q_{GS} + Q_{GD} + C_{PP}\left(V_{FG} - V_{CG}\right)$$

→ **Implicit computation of V_{FG}**

PSP-based Flash cell model 3/4

Addition of the injection currents

- From surface potentials, vertical electric fields through tunnel oxide can be computed



Fowler-Nordheim current

$$I_{FN} = \alpha . S . \boxed{E_{TUN}}^{2} e^{\frac{-\beta}{\boxed{E_{TUN}}}}$$

PSP-based Flash cell model 3/4

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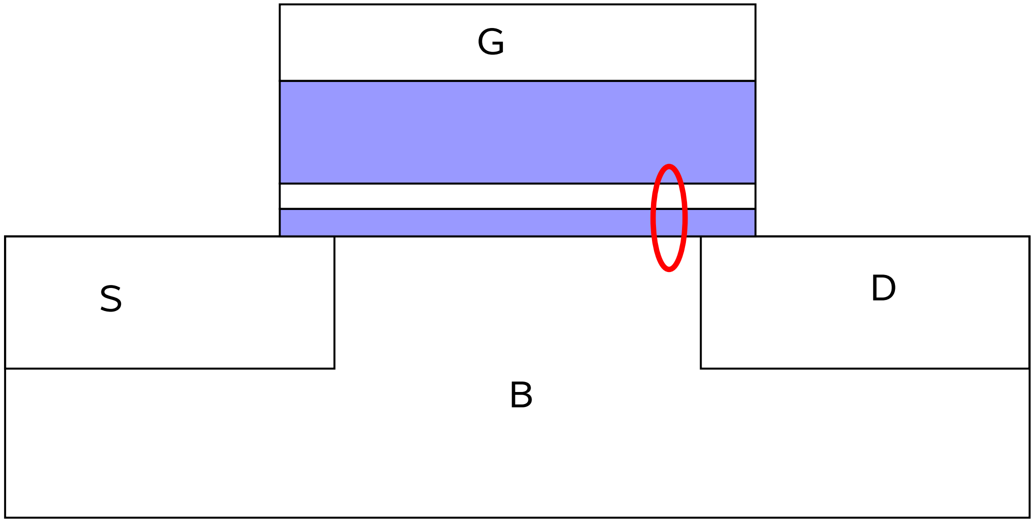

Channel Hot Electron current

$$I_{CHE} = A_D . I_{AVL} . e^{\frac{-A_{D\exp}}{\boxed{E_{TUND}}}}$$

PSP-based Flash cell model 4/4

Computation scheme

- Static relation $$Q_{FG} = Q_{GI} + Q_{GS} + Q_{GD} + C_{PP}\left(V_{FG} - V_{CG}\right)$$
- Dynamic relation $$Q_{FG} = Q_{FG0} + \int (I_{FN} + I_{CHE})dt$$

PSP-based Flash cell model 4/4

Computation scheme

- Static relation $$Q_{FG} = Q_{GI} + Q_{GS} + Q_{GD} + C_{PP}\left(V_{FG} - V_{CG}\right)$$
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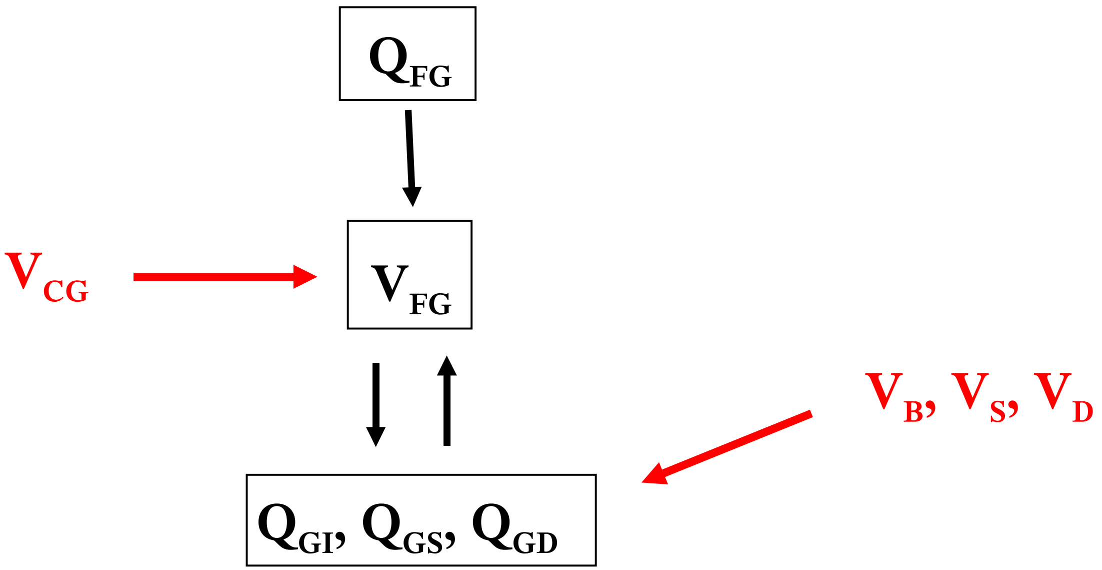

Q_{FG}

V_{CG}

V_{FG}

V_B, V_S, V_D

Q_{GI}, Q_{GS}, Q_{GD}

PSP-based Flash cell model 4/4

Computation scheme

- Static relation $Q_{FG} = Q_{GI} + Q_{GS} + Q_{GD} + C_{PP}\left(V_{FG} - V_{CG}\right)$
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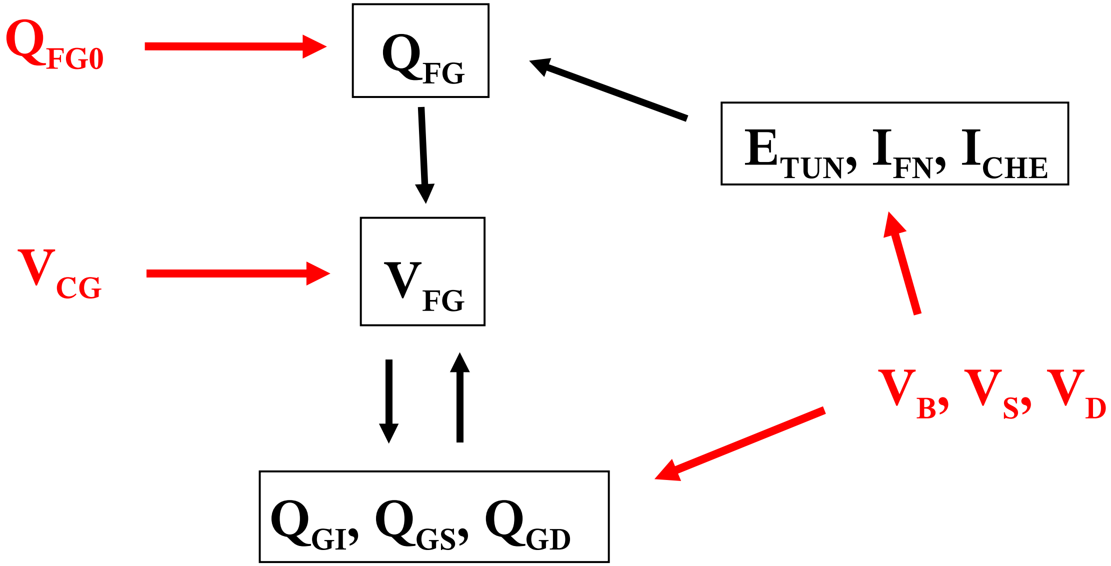

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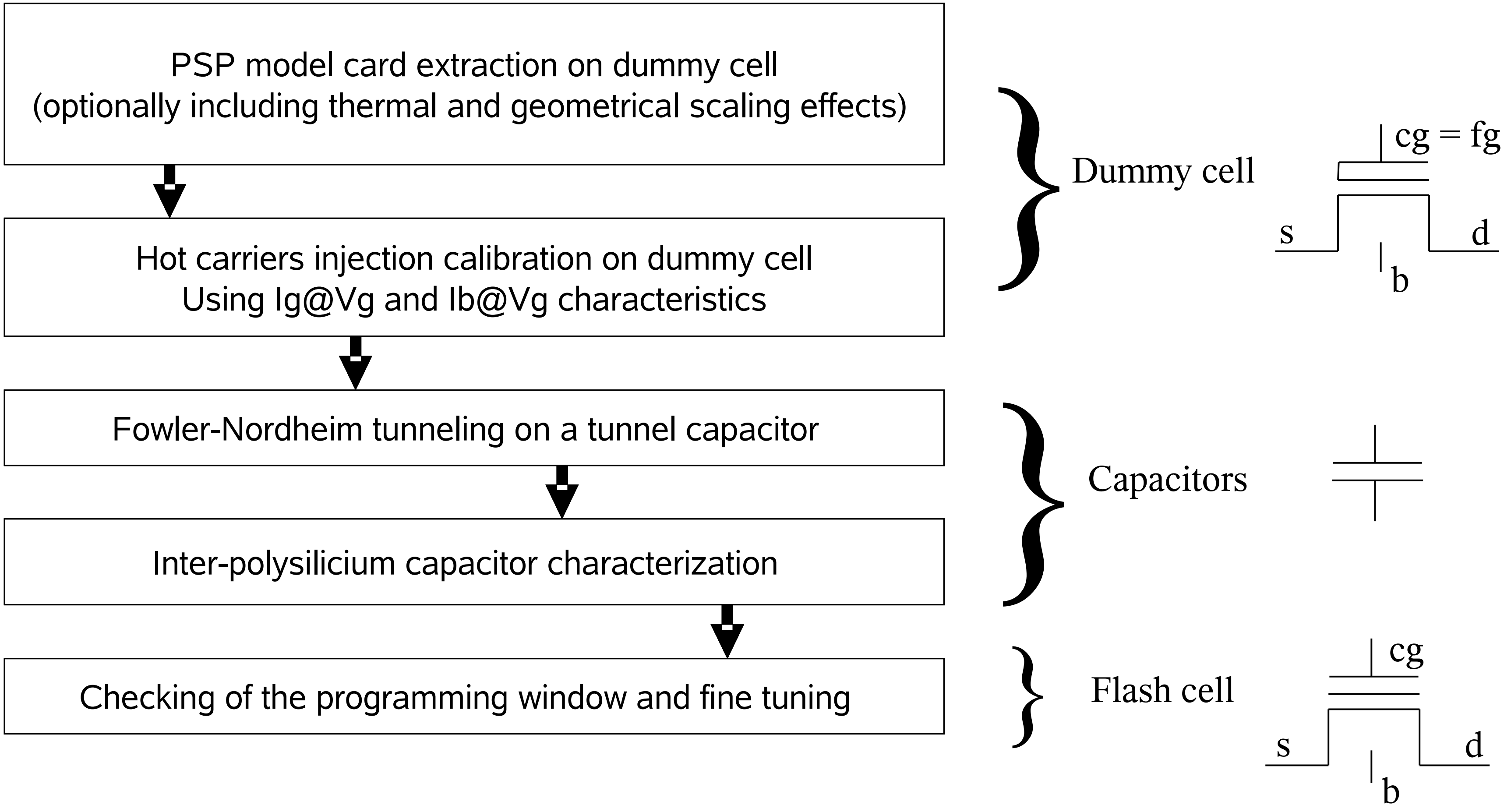
Characterization procedure 1/4

Characterization procedure diagram



PSP model card extraction on dummy cell
(optionally including thermal and geometrical scaling effects)

Hot carriers injection calibration on dummy cell
Using Ig@Vg and Ib@Vg characteristics

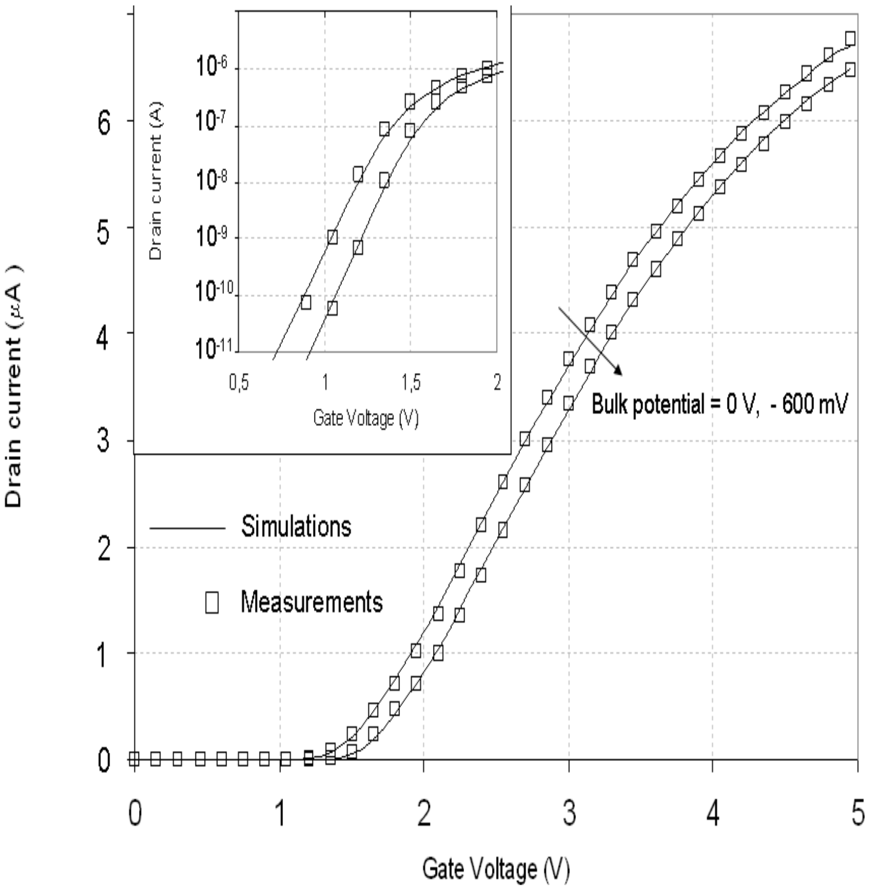
Fowler-Nordheim tunneling on a tunnel capacitor

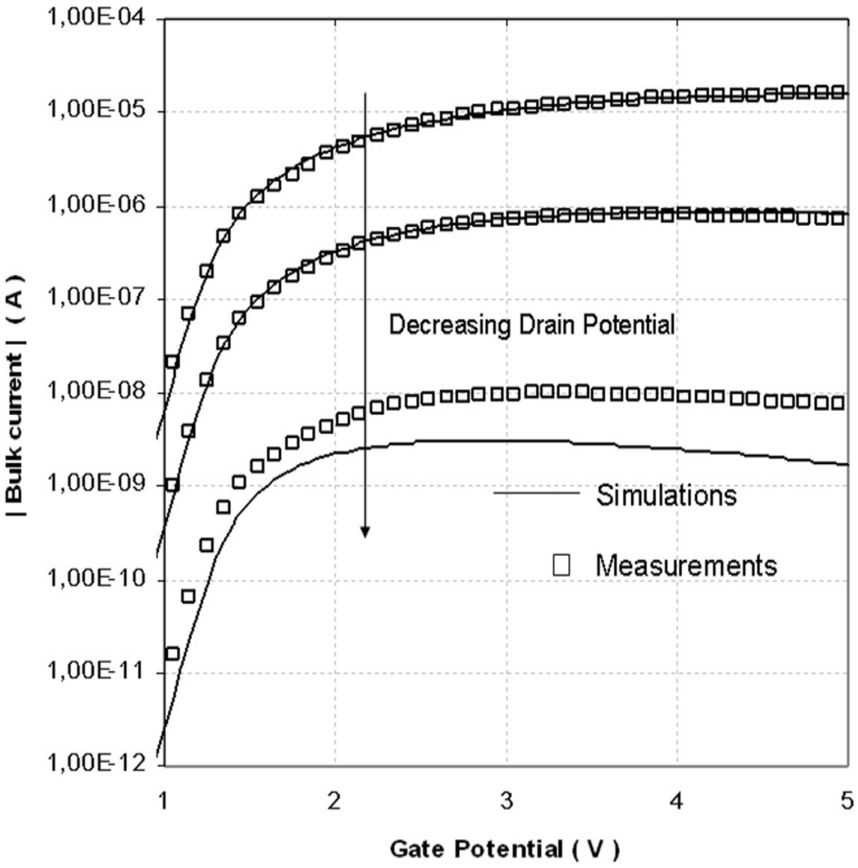
Inter-polysilicium capacitor characterization

Checking of the programming window and fine tuning

Characterization procedure 2/4

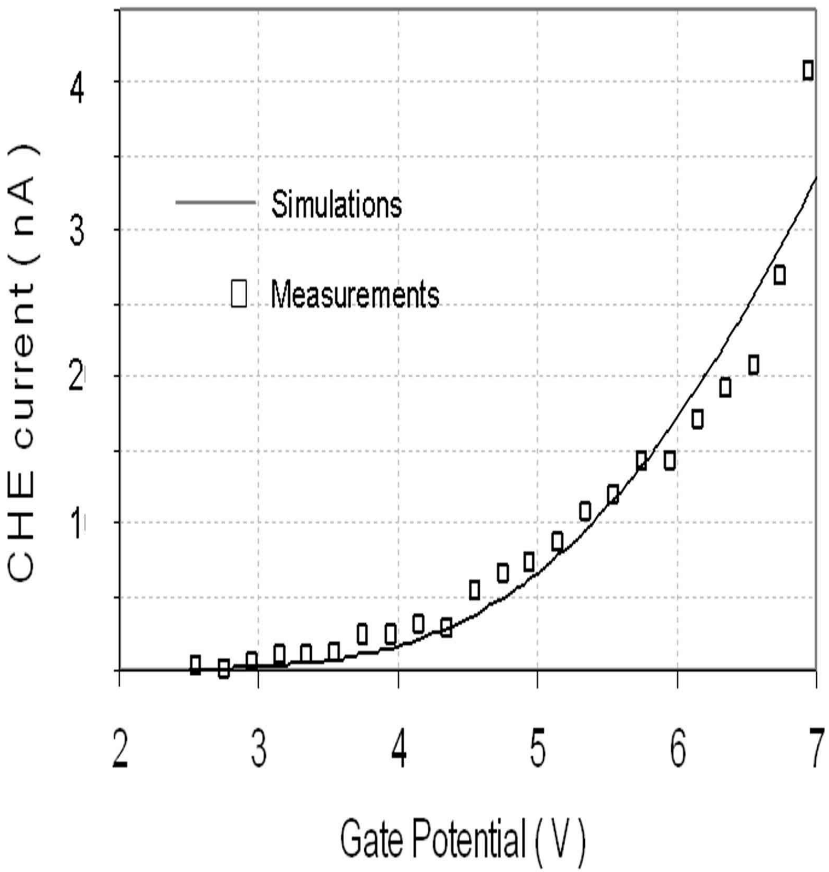
PSP model card extraction using a dummy cell

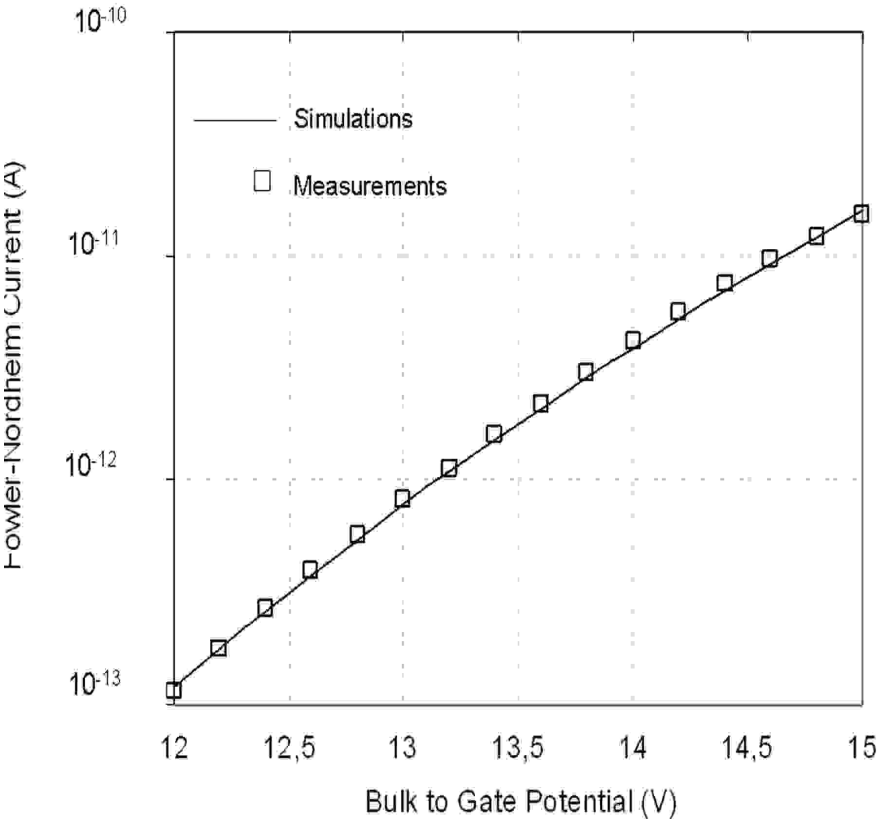




Characterization procedure 3/4

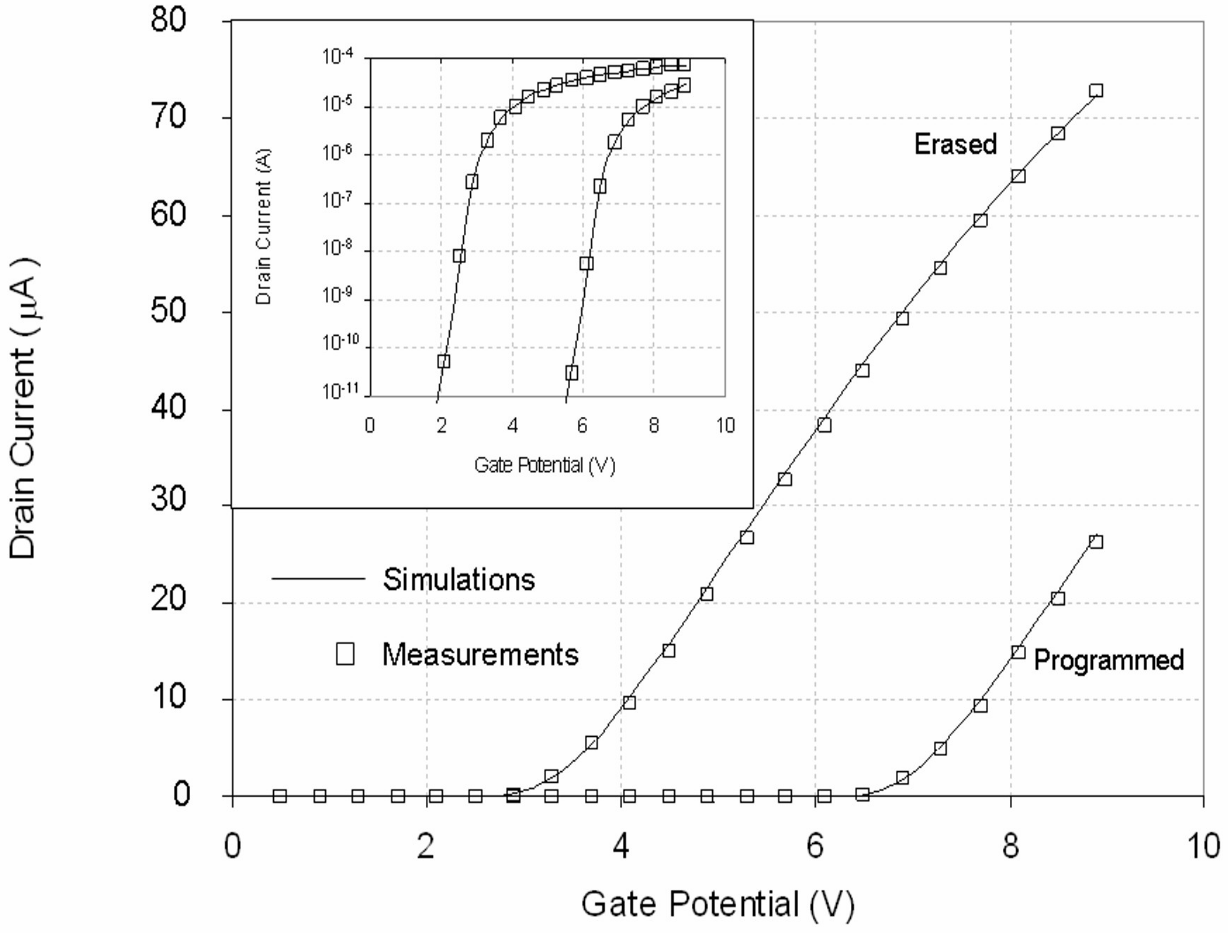
Injection current calibration





Characterization procedure 4/4

Fine tuning on real cell characteristics



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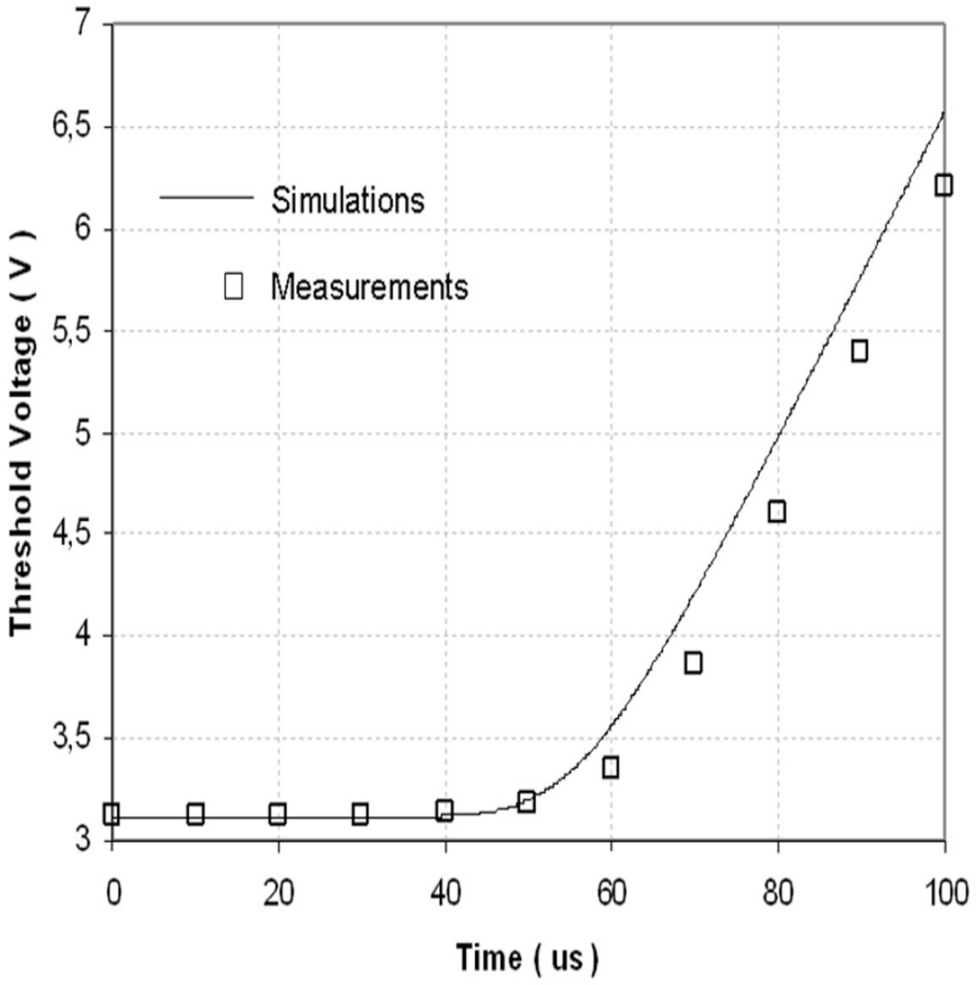
Simulations 1/2

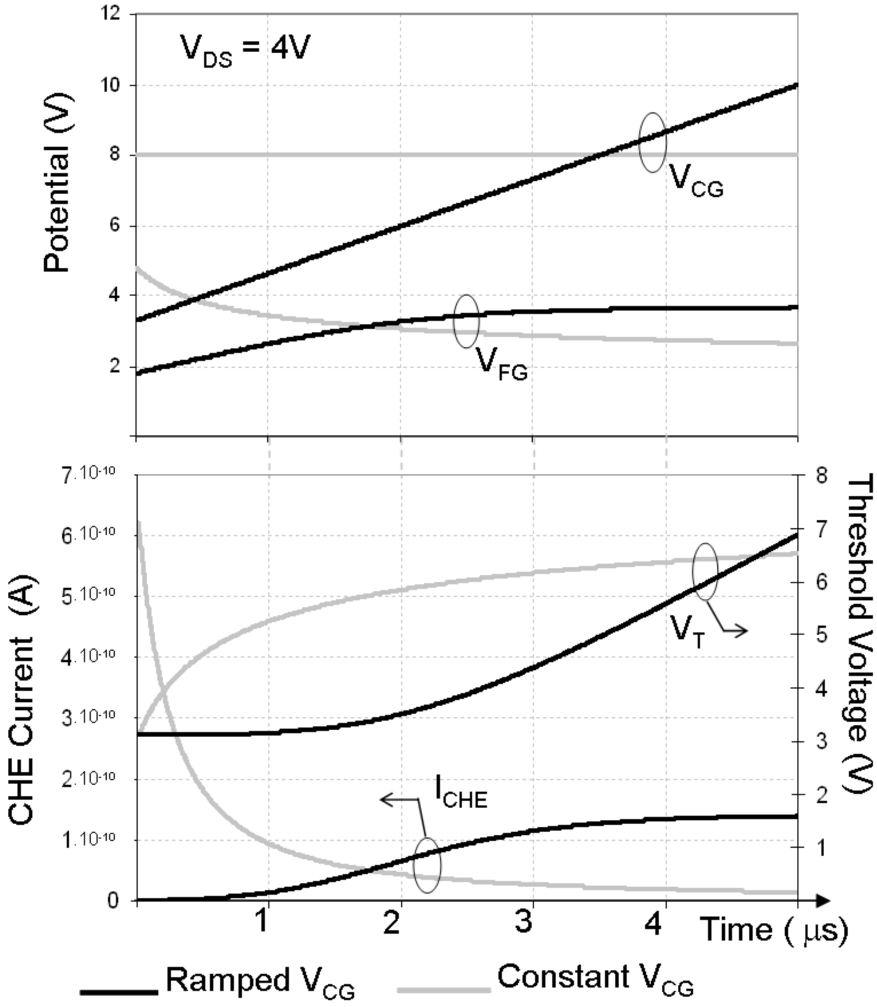
Dynamic reliability (example)



- V_T evolutions are compared with a standard programming polarization.
- V_T error after programming < 0.5 V

Simulations 2/2

Overall performances



- Simulation slower than the single PSP model

+5 % for DC simulation

+70 % for transient simulation

- Internal data can be observed (as V_{FG})

- General behavior concords with theory.

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Conclusions

The proposed Flash memory cell model :

- is compact to integrate common circuit simulators.
- takes advantage of a MOS channel advanced description (using PSP).
- is written with a flexible code (Verilog-A).
- can perform both DC and transient simulations.
- is adapted for analysis about consumption or injection rates.

Thanks for your attention