Co-Simulation of mixed HW/SW and Analog/RF systems at architectural level

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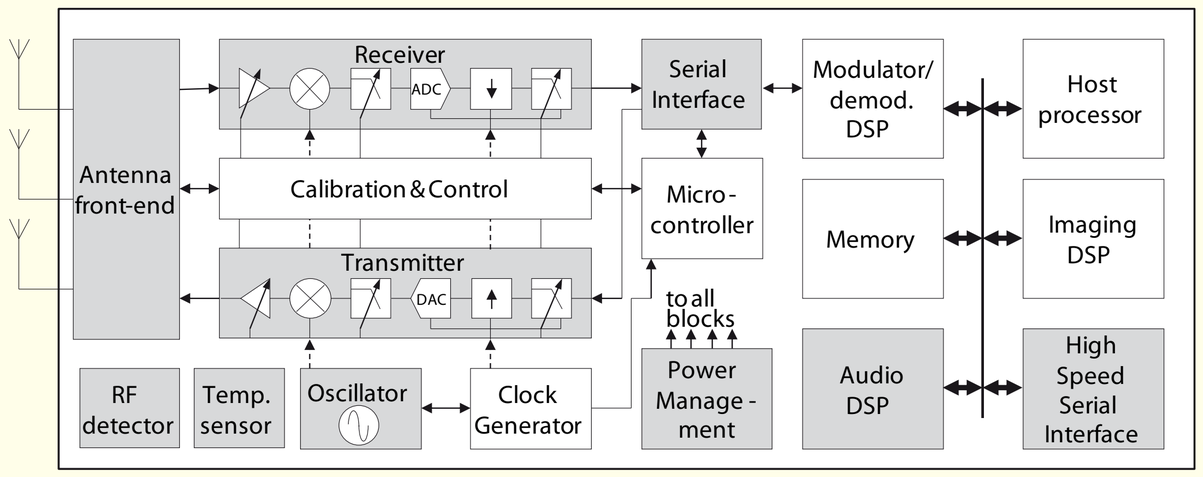
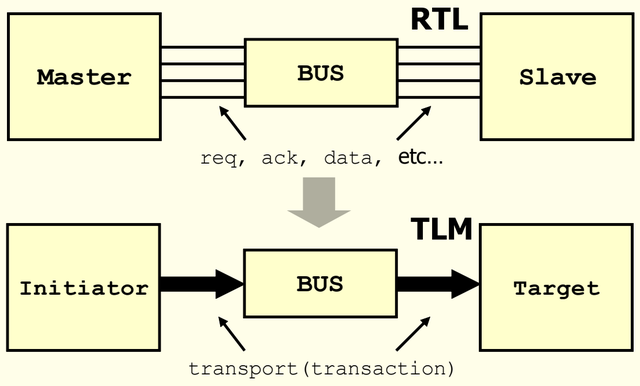
The challenge: Co-simulation of systems containing digital hardware, software and analog hardware.

The tool: SystemC with the extension libraries **SystemC AMS** and **TLM 2.0**

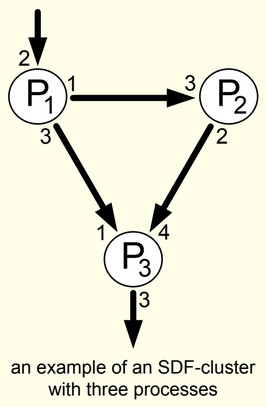


Transaction Level modelling (TLM) bundles the low-level communication events of a bus protocol into a single element called **transaction**. A pointer to the transaction is passed between **initiators** and **targets** using a **method interface**. For example, a processor might send a read request transaction to a memory, which then copies the requested data to the data section of the transaction. The TLM 2.0 data structure for a transaction is the **generic payload**.
TLM 2.0 allows the transactions to be annotated with a **timing delay** when using the **loosely timed coding style**. That is, processes can send future transactions while locally running ahead of simulation time (temporal decoupling or "time warp"). This reduces context switches, but also may introduce simulation inaccuracies like data being processed out of order.

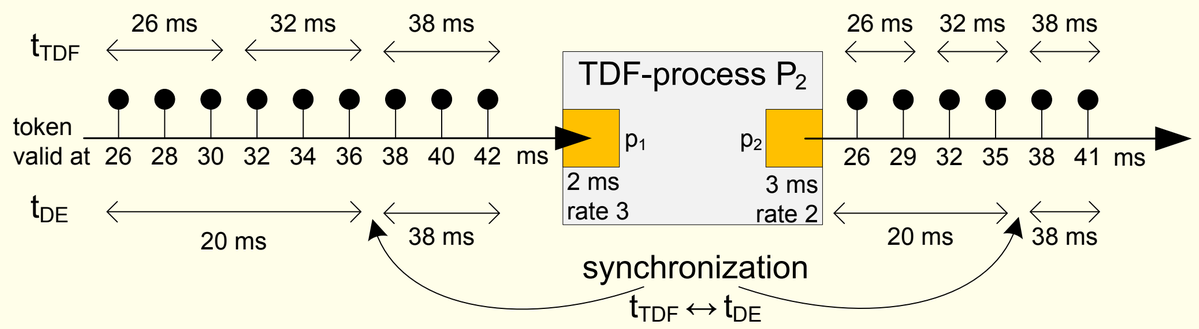


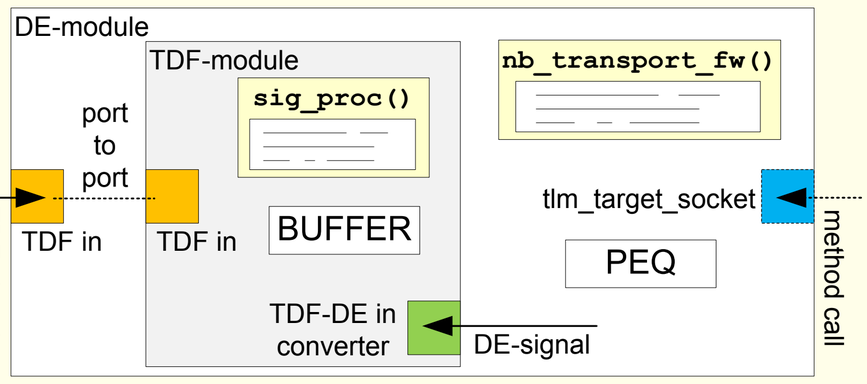
Command: `TLM_READ_COMMAND, TLM_WRITE_COMMAND, TLM_IGNORE_COMMAND`
Address: `type uint64`
Data pointer: `type unsigned char*`
Data length: `type unsigned int`
Respons status: `TLM_OK_RESPONSE, TLM_INCOMPLETE_RESPONSE, TLM_GENERIC_ERROR_RESPONSE, TLM_ADDRESS_ERROR_RESPONSE, ...`

some generic payload attributes



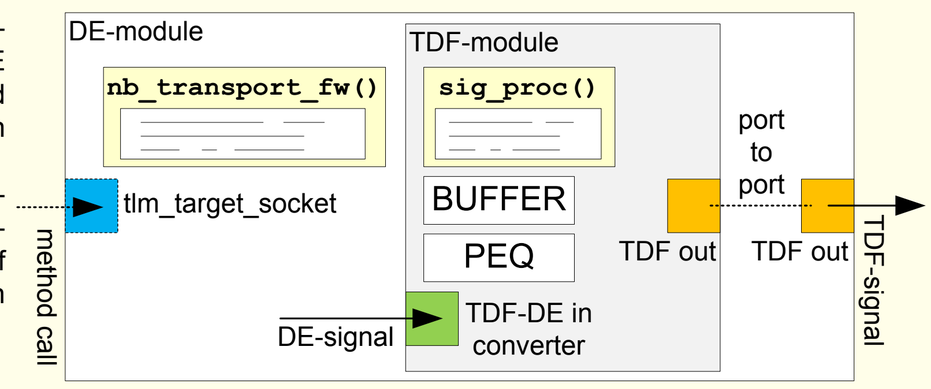
Timed Data Flow (TDF) is the main Model of Computation (MoC) used by SystemC AMS. It is a timed variant of the well known Synchronous Data-flow (SDF) MoC, where processes consume and produce data tokens with a constant **data rate** every time they are firing.
In the TDF MoC, a **sampling period** is associated with each token consumption/production. Since a static schedule can be computed before the simulation, TDF models allow very fast simulation of data flow oriented systems often found in signal processing.
SystemC AMS has its own simulation time (t_{TDF}), which usually runs ahead of SystemC simulation time (t_{DE}). The figure below shows an example, where you also see for each token the values for t_{TDF} and t_{DE}, when the token is processed, as well as the time when it is valid regarding simulated time. Therefore, we have temporal decoupling also in TDF.





The TDF→TLM converter gets READ transactions, and copies the buffer data to the transaction.
It triggers synchronization when its internal buffer is full. If it is empty, it returns an error response.

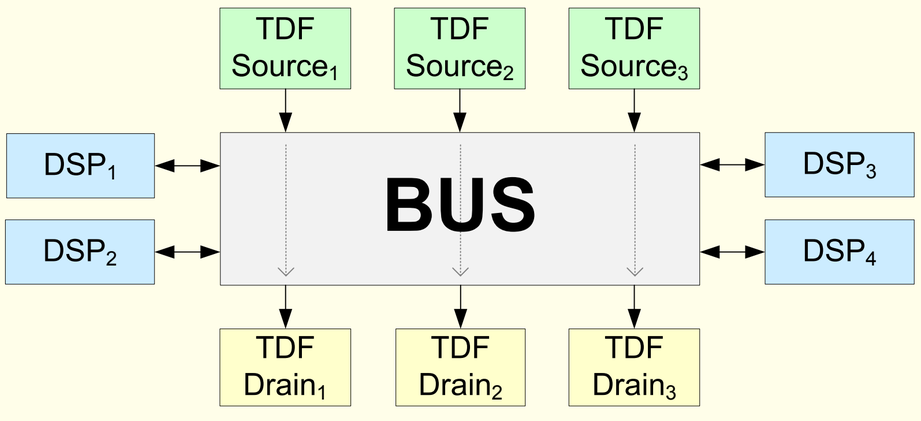
The TLM→TDF converter gets WRITE transactions, and copies the transaction data to the buffer.
It triggers synchronization when its internal buffer is empty. If it is full, it returns an error response.



Conversion between TLM and TDF: the general idea
- load streaming TDF data into transactions
- stream transaction data into TDF signals
- fit together the temporal decoupling on both sides

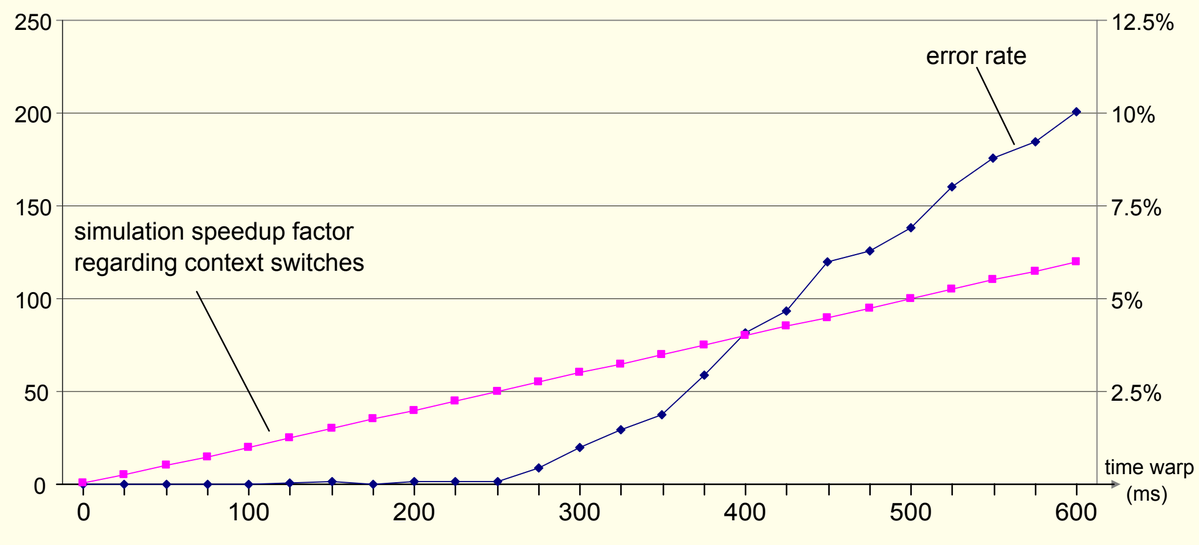
Issues to resolve:
- TLM transactions may arrive irregularly
  ⇒ a buffer for the data is used
- TLM transactions may arrive out of order
  ⇒ the transactions are stored in a payload event queue (PEQ) as long as possible. The PEQ resolves the order
- The TDF cluster may run too far ahead of TLM
  ⇒ Synchronization is triggered when needed by accessing a TDF↔DE converter port

An example system



Example system using the converters above.
The DSPs and the Bus are modelled using TLM.

An example system was implemented using the converters described above. It consists of four DSPs, which randomly read from one of three TDF sources, process the input, and write the results to the respective TDF output streams. It is an abstract system, though a possible application could a software defined radio.
This example serves two purposes: Showing the functional correctness of the conversion approach, and to observe simulation speed vs. simulation accuracy tradeoffs, typical for loosely timed TLM models. In this case, simulation speed was measured in terms of context switches of the DSPs, while simulation errors manifested themselves as data packets arriving out of order.



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