Predicting the Correlation between Analog Behavioral Models and SPICE Circuits for Robust SoC Verification

Vipin Sharma
Guha Lakshmanan
Sandeep Tare
Sudhind Dhamankar

Outline

- Problem Definition
- Co-sim BMV Workflow
- BMV flow pre-requisites
- Flow setup
- BMV flow execution
- DCO case study
- Applicability to other mixed-signal circuits
- Conclusion

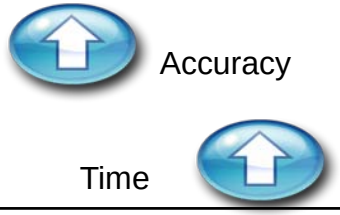
Outline

- Problem Definition
- Co-sim BMV Workflow
- BMV flow pre-requisites
- Flow setup
- BMV flow execution
- DCO case study
- Applicability to other mixed-signal circuits
- Conclusion

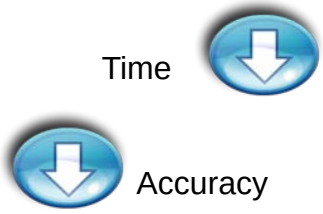
Problem Definition

SoC Verification Effort = f (accuracy, time)
How do we resolve this tradeoff?

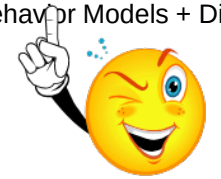
FULL CHIP SPICE
(Ideal case – does not exist)



FULL CHIP HDL
(Preferred, too inaccurate)

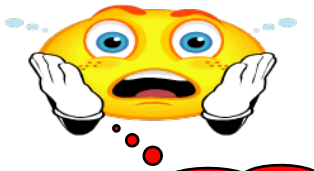


CO-SIMULATION
SPICE + RTL (Behavior Models + Digital**)**



Everything works!

Results don't look right!
What went wrong?
Are Behavioral Models correct?

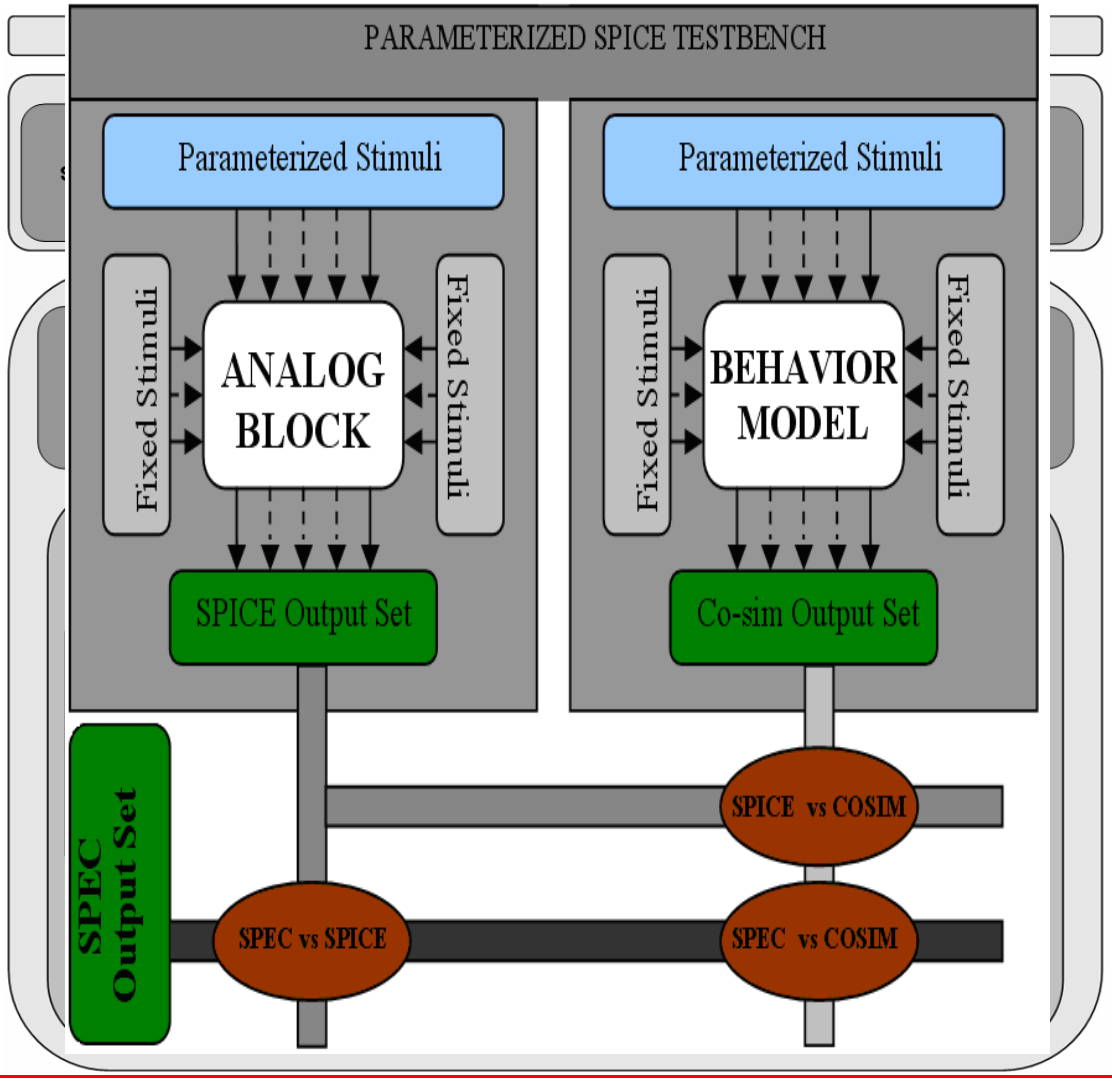


I need to verify Behavioral Models!

Outline

- Problem Definition
- Co-sim BMV Workflow
- BMV flow pre-requisites
- Flow setup
- BMV flow execution
- DCO case study
- Applicability to other mixed-signal circuits
- Conclusion

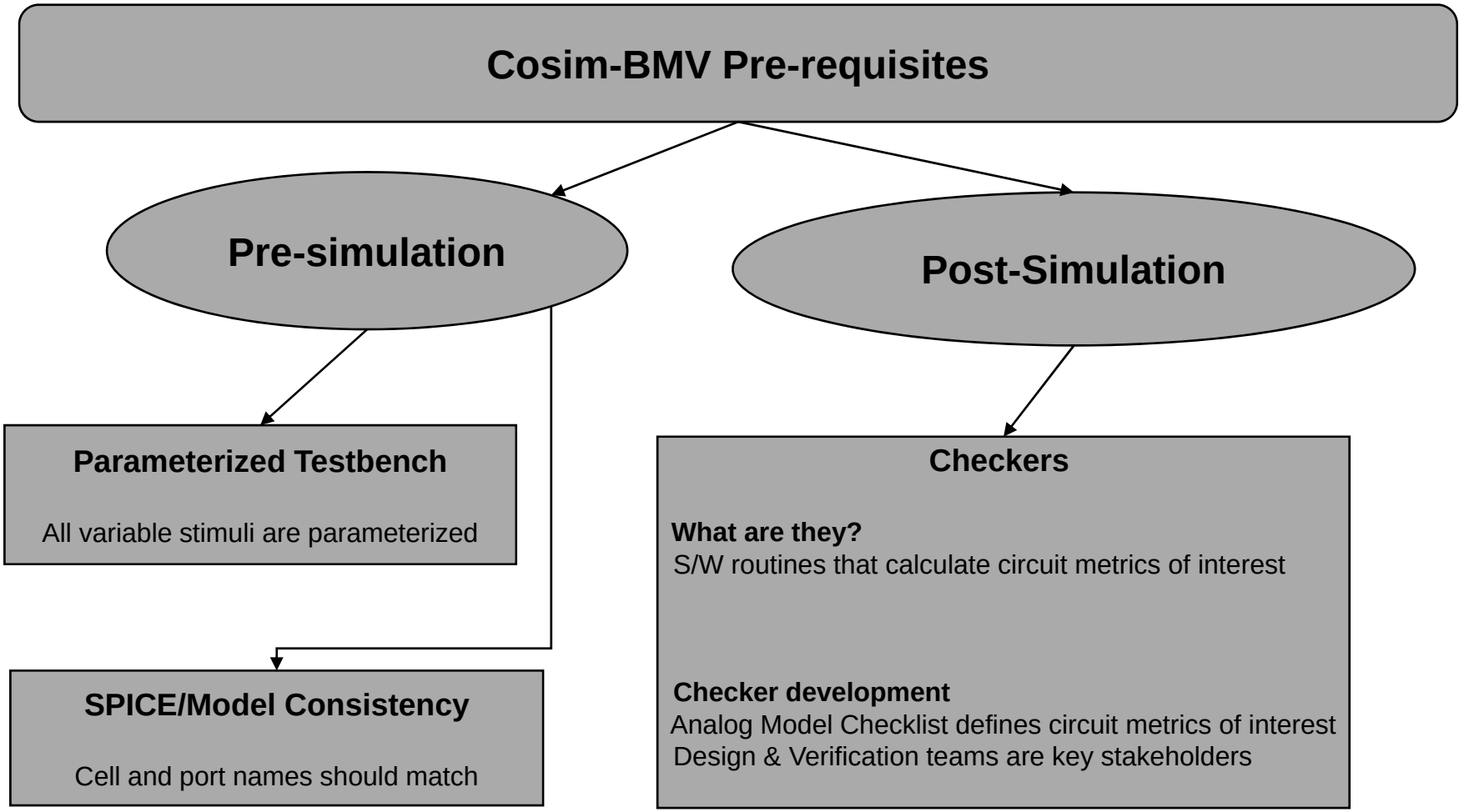
Co-sim BMV Workflow



Outline

- Problem Definition
- Co-sim BMV Workflow
- BMV flow pre-requisites
- Flow setup
- BMV flow execution
- DCO case study
- Applicability to other mixed-signal circuits
- Conclusion

Flow Prerequisites



Outline

- Problem Definition
- Co-sim BMV Workflow
- BMV flow pre-requisites
- Flow setup
- BMV flow execution
- DCO case study
- Applicability to other mixed-signal circuits
- Conclusion

Flow Setup

Circuit Parameter File (CPF)

- List of all the test cases
- Cycles the flow for every case

Parameter Template (PT)

- Parameters in SPICE bench
- Every testcase has one PT

COSIM Options File

Allows SPICE testbench & models to work in harmony

Simulator Settings File

Simulator settings for test case

Outline

- Problem Definition
- Co-sim BMV Workflow
- BMV flow pre-requisites
- Flow setup
- BMV flow execution
- DCO case study
- Applicability to other mixed-signal circuits
- Conclusion

Flow Execution

- BMV Algorithm

1. All entries in circuit parameter file (CPF) processed?
    1. If yes, go to step 6
    2. If no, go to next step 2
2. Do SPICE run
3. Post process SPICE results
4. Do Co-simulation run (Invoke cosimPostProcess.pl with –COSIM switch)
5. Post process COSIM results and go to step 1
6. Print dashboards (results)
7. Stop

Outline

- Problem Definition
- Co-sim BMV Workflow
- BMV flow pre-requisites
- Flow setup
- BMV flow execution
- DCO case study
- Applicability to other mixed-signal circuits
- Conclusion

DCO

- DCO
  witho
- Only

Coarse
(PB[6:0]

Mediu
AB[64:0

Fine
TIB[128:

Finest
TFB[3:0

Some Nomenclature…

PVT/PB = Coarse Tuning
ACQ/AB = Medium Tuning
TIB = Fine Tuning
TFB = Finest Tuning

Also,
Freq = 1/(period of osc)

Conversely,
Period of osc = 1/(Freq)

DCO case study – metrics, checkers

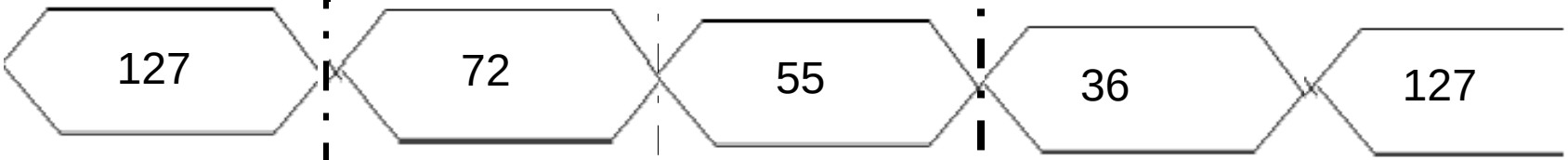
- DCO circuit metrics of interest
  - Tuning precision
  - Monotonicity
  - Other controls
- DCO checker development
  - Oscillator frequency/period measurement
  - Monotonicity detection

DCO case study – Monotonicity

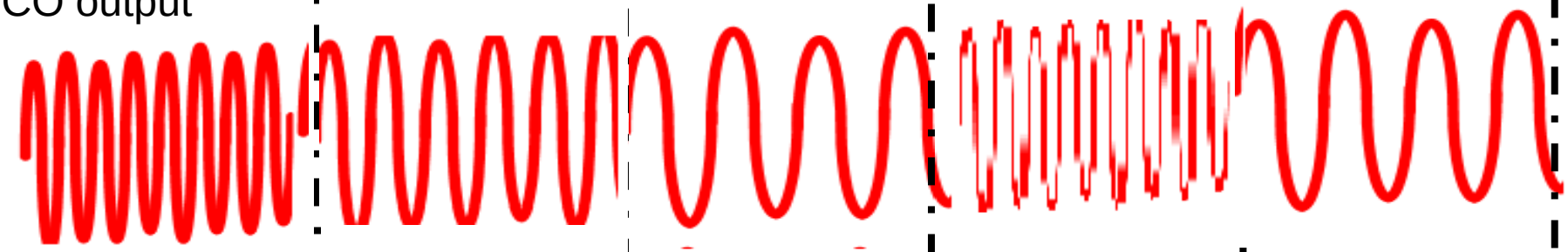
TEST ID	CATEGORY	DESCRIPTION
dco_PVT_t1	PVT (Coarse Tuning)	Tune DCO PB inputs from Fmin to Fcenter to Fmax
dco_PVT_t2	PVT (Coarse Tuning)	Tune DCO PB inputs from Fmax to Fcenter to Fmin
dco_AB_t1	ACQ (Medium Tuning)	Tune DCO AB inputs from FminAB to FcenterAB to FmaxAB
dco_AB_t2	ACQ (Medium Tuning)	Tune DCO AB inputs from FmaxAB to FcenterAB to FminAB
dco_TFB_t1	TFB (Fine Tuning)	Tune DCO TFB inputs from FminTFB to FmaxTFB

DCO case study - Tuning precision

DCO frequency control word



DCO output



Expected Frequency (from spec)

1.9 Ghz | 1.8 Ghz | 1.7 Ghz

Computed Frequency (from simulation)

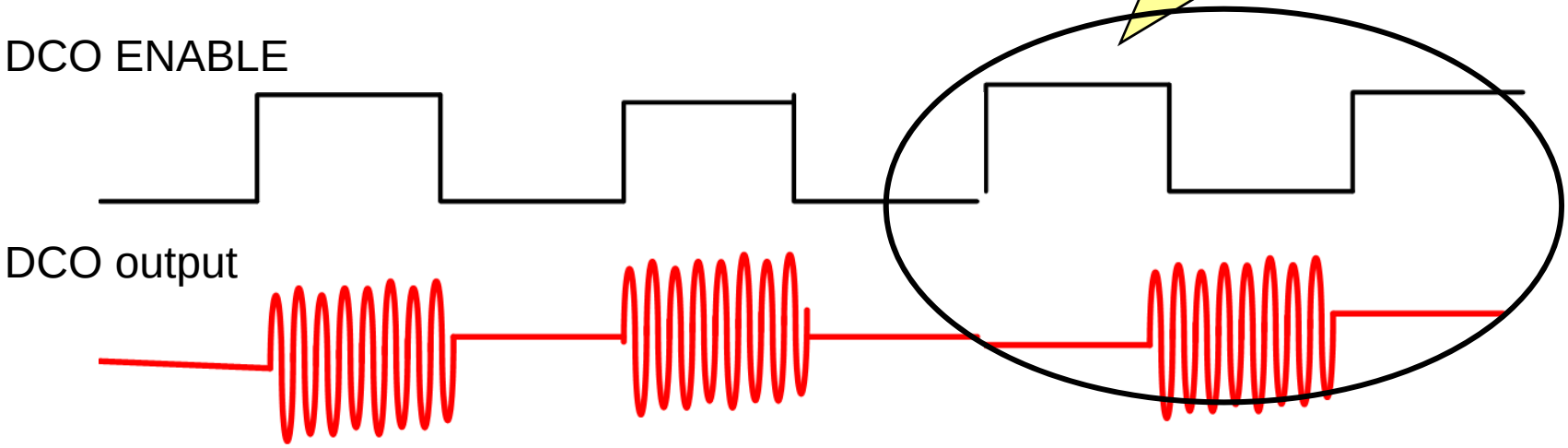
1.9 Ghz | 1.8 Ghz | 1.7 Ghz

1.6 Ghz | 1.85 Ghz

1.9 Ghz | 1.7 Ghz

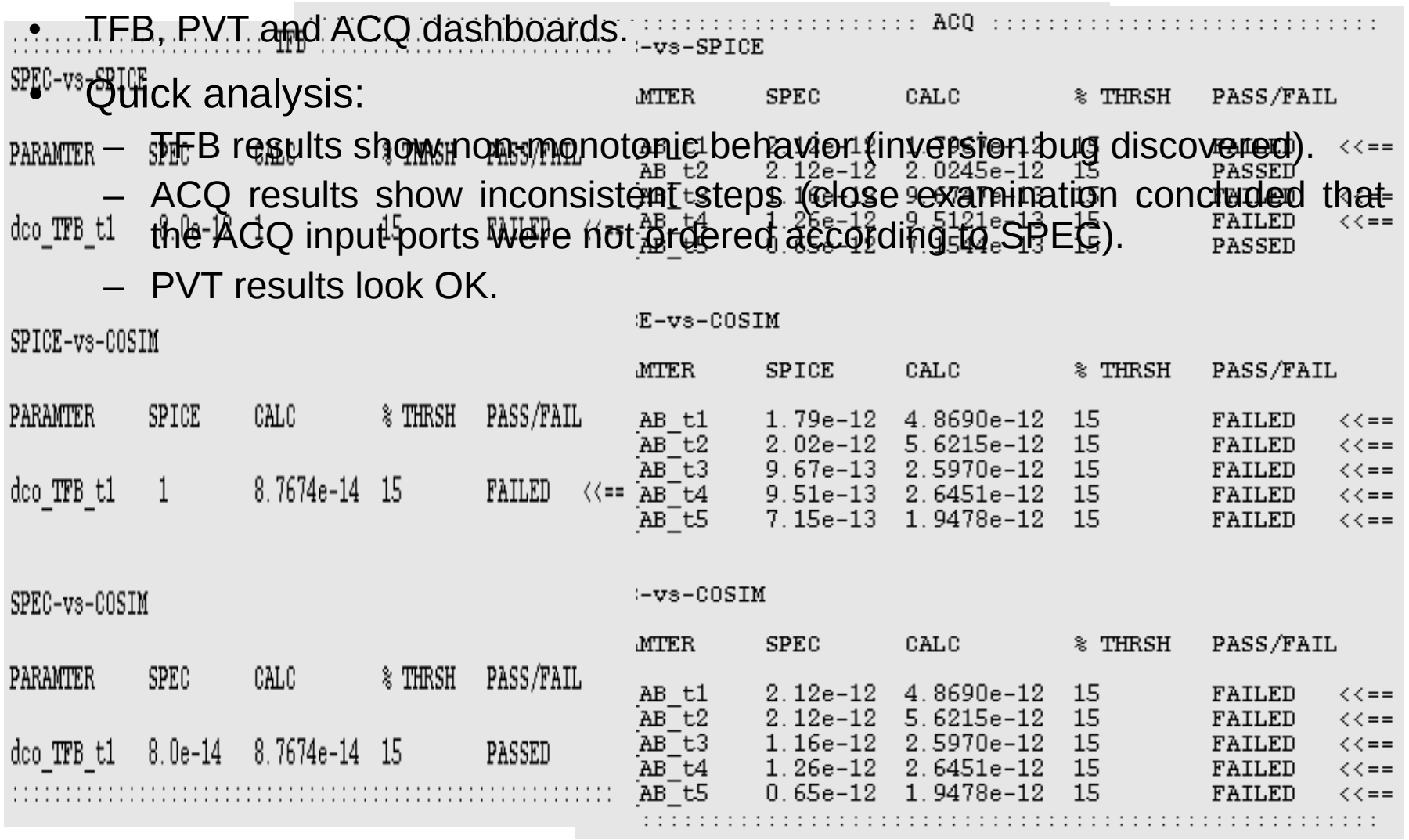
DCO case study - controls

!!!Incorrect Behavior!!!
DCO output is active When enable is low And vice versa



DCO case study – results

- TFB, PVT and ACQ dashboards.
- Quick analysis:
  - TFB results show non-monotonic behavior (inversion bug discovered).
  - ACQ results show inconsistent steps (close examination concluded that the ACQ input ports were not ordered according to SPEC).
  - PVT results look OK.



TFB

SPEC-vs-SPICE

PARAMTER	SPEC	CALC	% THRSH	PASS/FAIL	
dco_TFB_t1	8.0e-14	1	15	FAILED	<<==

SPICE-vs-COSIM

PARAMTER	SPICE	CALC	% THRSH	PASS/FAIL	
dco_TFB_t1	1	8.7674e-14	15	FAILED	<<==

SPEC-vs-COSIM

PARAMTER	SPEC	CALC	% THRSH	PASS/FAIL
dco_TFB_t1	8.0e-14	8.7674e-14	15	PASSED

ACQ

-vs-SPICE

MTER	SPEC	CALC	% THRSH	PASS/FAIL	
AB_t1	2.12e-12	4.8690e-12	15	FAILED	<<==
AB_t2	2.12e-12	2.0245e-12	15	PASSED	
AB_t3	1.16e-12	2.5970e-12	15	FAILED	<<==
AB_t4	1.26e-12	9.5121e-13	15	FAILED	<<==
AB_t5	0.65e-12	1.9544e-13	15	PASSED	

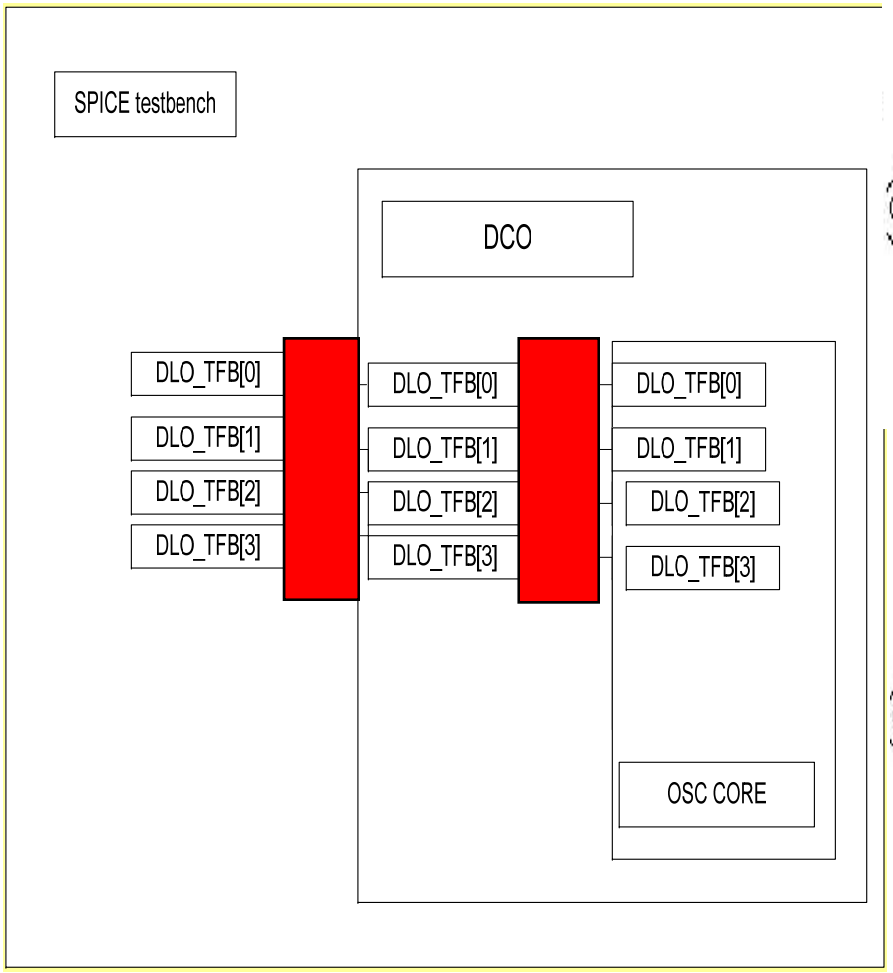
E-vs-COSIM

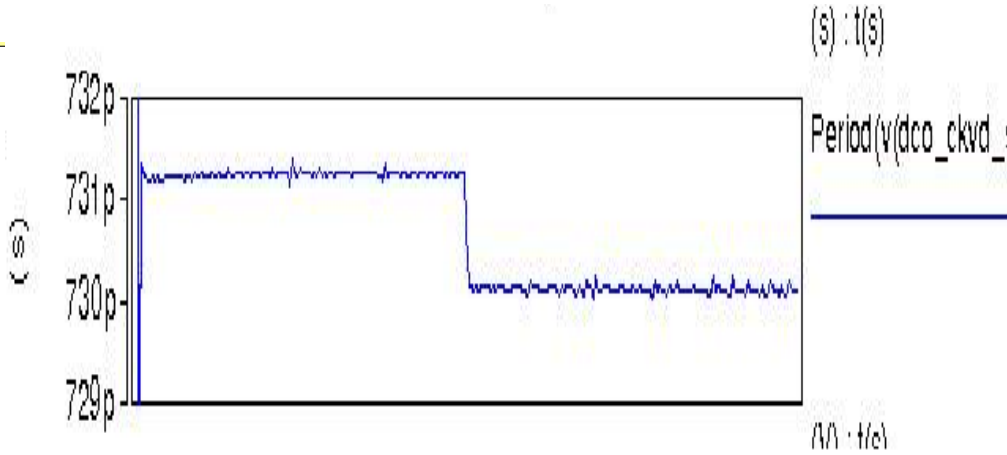
MTER	SPICE	CALC	% THRSH	PASS/FAIL	
AB_t1	1.79e-12	4.8690e-12	15	FAILED	<<==
AB_t2	2.02e-12	5.6215e-12	15	FAILED	<<==
AB_t3	9.67e-13	2.5970e-12	15	FAILED	<<==
AB_t4	9.51e-13	2.6451e-12	15	FAILED	<<==
AB_t5	7.15e-13	1.9478e-12	15	FAILED	<<==

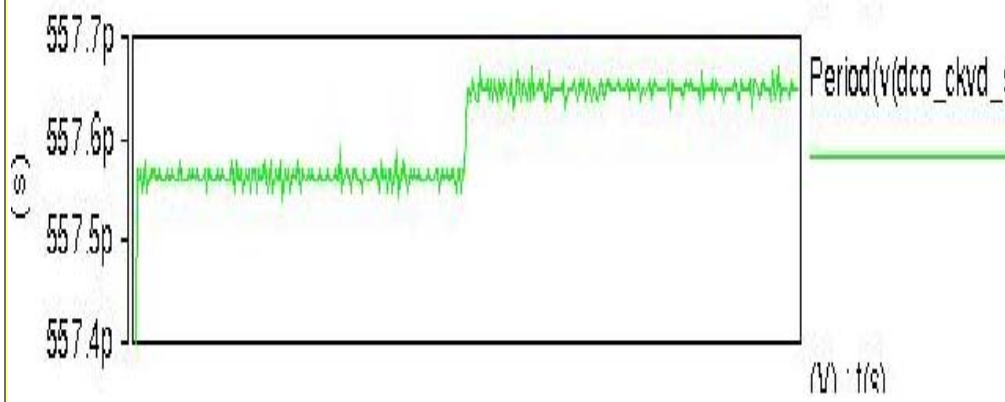
-vs-COSIM

MTER	SPEC	CALC	% THRSH	PASS/FAIL	
AB_t1	2.12e-12	4.8690e-12	15	FAILED	<<==
AB_t2	2.12e-12	5.6215e-12	15	FAILED	<<==
AB_t3	1.16e-12	2.5970e-12	15	FAILED	<<==
AB_t4	1.26e-12	2.6451e-12	15	FAILED	<<==
AB_t5	0.65e-12	1.9478e-12	15	FAILED	<<==

DCO case study – TFB inversion bug





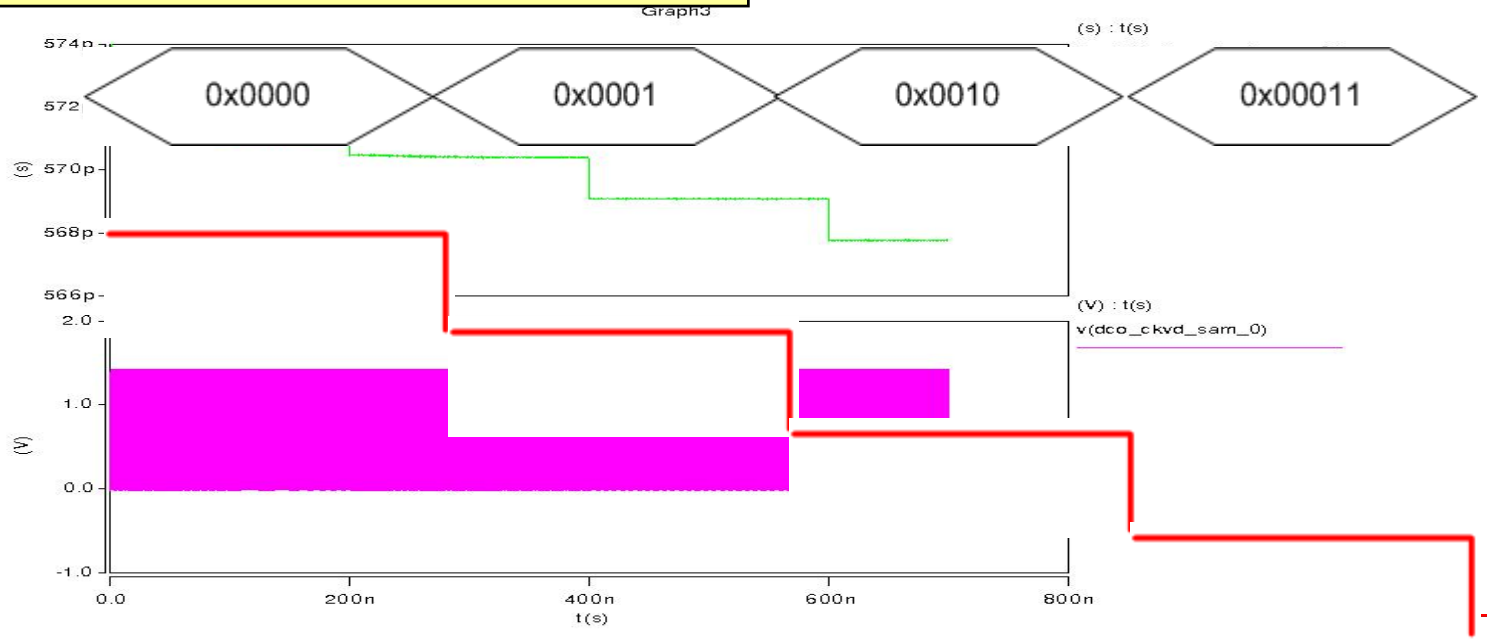


DCO case study – Spec incorrect

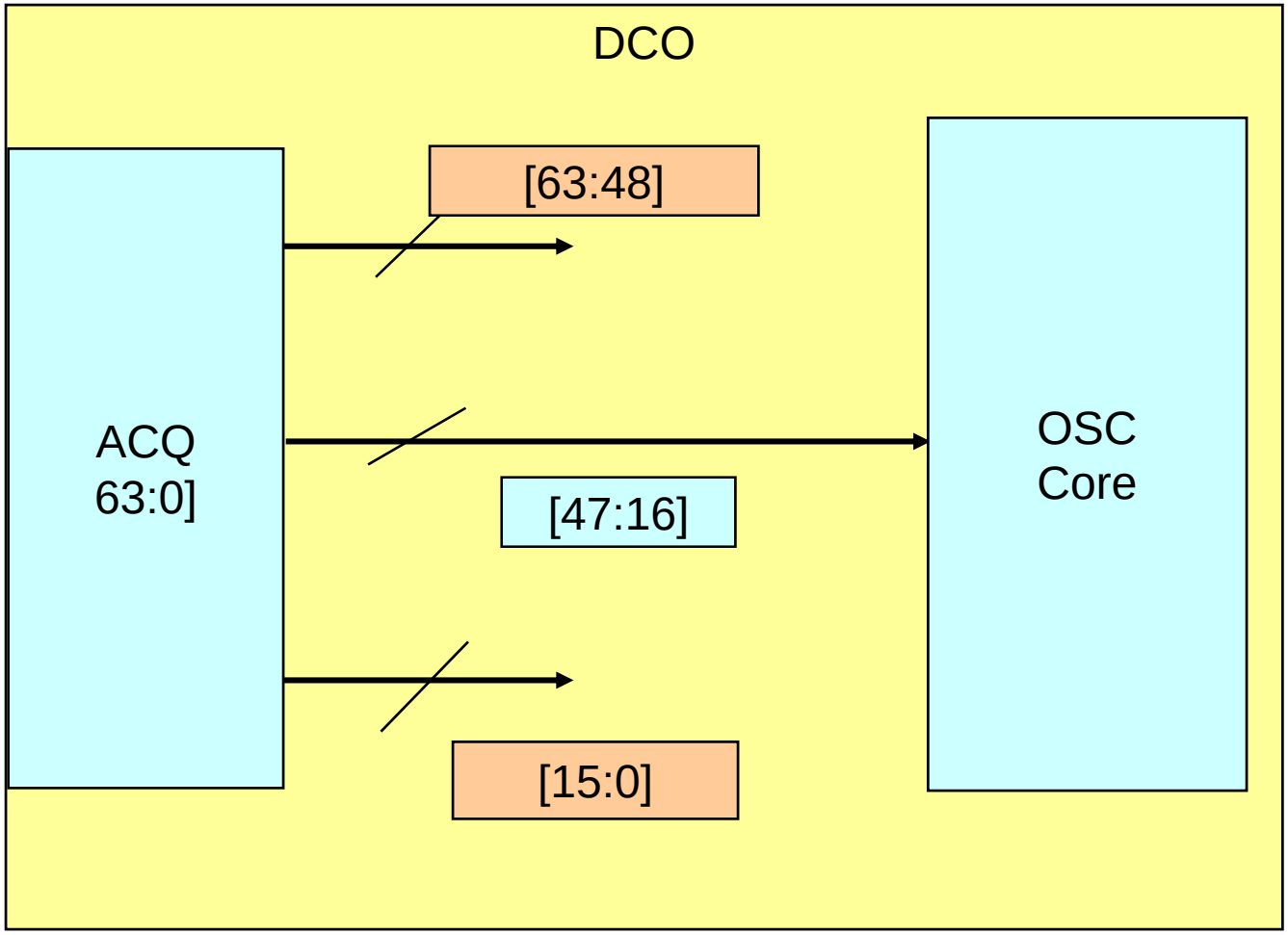
-
-
-

ACQ (medium tuning) has 64 bits that are **Unit weighted**

$$Freq = f\left(\sum acq[0..63]\right)$$



DCO Case study – ACQ spec incorrect



Applicability to other mixed signal circuits

- Circuit independent BMV flow
  - Not restricted to discrete circuits (for example DCO)
  - Independent of the type of circuitry
  - Design specific custom checkers make this possible

- CTA (continuous time amplifier) case study highlights
  - Careabouts: gain variation, process corners, bias control and test modes
  - Results
    - Good correlation across all process corners at low gain values
    - Bias current was not modeled

Conclusion

- Functional mismatch can lead to silicon bugs
- Performance mismatch can lead to inaccurate prediction of the system behavior

- Benefits offered by BMV:
  - Models verified against the SPEC
  - Models verified against the circuit
  - Helps in debugging functional issues early on in the project cycle
  - Ensures all specification details are addressed in the model

Last Page Intentionally Left Blank