Behavioural Modelling for Stability of CMOS SRAM Cells Subject to Random Discrete Doping

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***Abstract*—Channel random discrete doping (RDD), one of the main sources of MOSFET intrinsic parameter fluctuations, significantly affects the stability of CMOS SRAM. This paper describes a behavioural model for 35nm CMOS technology SRAM cells with random discrete dopants using VHDL-AMS (Analogue and Mixed Signal). The static transfer characteristic (STC) is described in the VHDL-AMS model. Monte Carlo simulation results of the behavioural model are close to those at SPICE level. The VHDL-AMS model can predict the worst case STC behaviour for SRAM induced by RDD but also improves the simulation speed by five times compared to SPICE.**

***Index Terms*—Behavioural modelling, MOSFET, random discrete doping, SPICE, SRAM, static transfer characteristics, VHDL-AMS.**

I. INTRODUCTION

The continuous scaling down of transistor dimensions has resulted in challenges at both technology and device levels [1]–[4]. One of these challenges is the increase in device variability which can be either intrinsic or extrinsic [2]–[3], with both having a strong influence on delay as well as on the power consumptions of devices, circuits and chips [4]. Although researchers are trying to improve CMOS technology and introduce new device architecture, variability is likely to be one of the serious problems for the next several CMOS generations [4]–[7].

The sources of intrinsic fluctuations in MOSFET characteristics include random discrete doping (RDD), line-edge roughness (LER) and atomic scale oxide thickness roughness (OTR) [8]–[10]. The microscopic variations in the number and location of dopant atoms in the channel induce device variations in deep sub-100nm technology [10]–[12], which may be mismatch of threshold voltages (Vth) or fluctuations of the drive current (and also mobility or transconductance). These intrinsic fluctuations are pronounced in minimum-geometry transistors which are often used in area constrained circuits such as SRAM cells [13]–[15].

The SRAM cell is one of the most important components in modern microprocessors and SOCs, and it is always considered as the benchmark circuit for development of CMOS technology. Large static noise margin (SNM) variations in SRAM caused by random doping have been observed [13]–[15]. SNM affects SRAM stability and determines the ability of the cell to maintain stable data under parasitic noise and device mismatches, and SNM can be characterized by static transfer characteristics curves [13]–[15].

For studying SRAM static transfer characteristics (STC) variations because of RDD, transistor level simulations such as SPICE are time consuming because repetitive simulations are needed with varying model parameters. Therefore, CAD tools which allow high-level behavioral simulation for micro-systems were developed. VHDL-AMS (Analogue and Mixed Signal) is one of the leading behavioural modelling languages with analogue extensions, and has been used by some researchers in different areas [16]–[19]. VHDL-AMS simulations based on behavioural model are computationally efficient compared to SPICE.

In this paper, a VHDL-AMS behavioural model for SRAM cells subject to RDD is developed. The STC variations because of RDD are predicted by the model with a reduction of simulation time. By using the behavioural model, one can get a general idea of the SRAM stability resulting from RDD without doing transistor-level simulations. In section II, the effects of RDD on STC curves (STCs) are investigated, Section III describes development of the behavioural model, and the simulation results of SPICE and the VHDL-AMS model are compared in section IV. In section V, the conclusions are given.

II. EFFECTS OF RDD ON THE STATIC TRANSFER CHARACTERISTICS OF CMOS SRAM

RDD induces potential variations within a device. The spread in the device transfer characteristics has been simulated by comprehensive 3-D atomistic simulations [14], [20]. A set of statistical parameters for describing RDD were extracted into the BSIM4 models [14] for 35nm technology MOSFETs.

Seven key BSIM4 model parameters (MPs) were chosen to characterize RDD effects at device level. Lpe0 is lateral non-uniform doping parameter at zero body bias (Vbs) which can affect the Vth of the model. Dsub is the DIBL coefficient exponent in the subthreshold region. Voff describes the difference in Vth between subthreshold and strong inversion regions, which significantly affects the subthreshold drain current. a1 and a2 are the first and second non-saturation factors, respectively. Rdswmin is the LDD resistance per unit width at high gate voltage and zero Vbs for internal Rds. Nfactor is called the subthreshold swing factor which relates to depletion capacitance fluctuations.

Fig. 1 shows the statistical distributions of Lpe0 and Dsub, which were extracted from 200 discrete devices. The approximate normal distributions are shown, and the other 5 MPs also have normal distributions (not shown). In the following, the fitting distribution parameters will be used in predefined functions for SPICE Monte Carlo (MC) simulations.

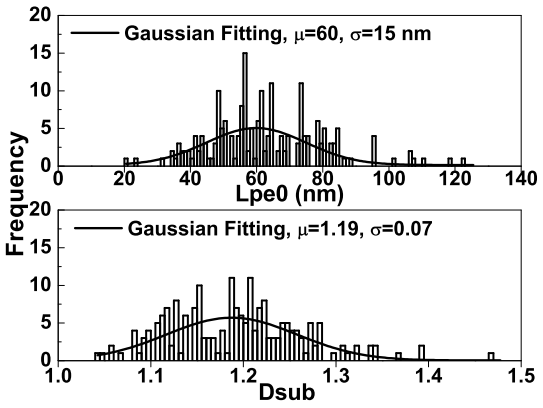

Fig. 1. Statistical distributions of Lpe0 and Dsub for characterizing RDD in BSIM4 models. The parameters are extracted from 200 devices, with the Gaussian fittings shown.

The effects of RDD at circuit level are studied by taking the SRAM cell as an example. Fig. 2(a) shows the circuit schematics, with two driving MOSFETs, M2 and M4 (M21 and M41 are designed as redundant devices), as well as two access (M5, M6) n-MOSFETs, and two load (M1, M3) p-MOSFETs. The SRAM is sensitive to noise at the start of its operation and attention is paid to its static noise margin (SNM) stability [13]–[15]. Fig. 2(b) illustrates that the SNM is defined as the smaller area formed by the two STCs. The variations of STCs directly result in the change of the SNM, and this work concentrates on the fluctuations of STCs caused by RDD to develop SRAM behavioural model.

The electrical characteristics of the 8 transistors are not the same for different SRAM cell instances because of RDD. Therefore, the performance of SRAM cells varies. Fig. 3 shows 2000 MC simulation results from SPICE. Parameter values are given by normal distributions. In Fig. 3(a), 5 MPs, other than Lpe0 and Dsub, are varied. We do not find huge STCs variations in the 2000 SRAM cells, which means these parameters are not crucial for SRAM stability. However, significant variations in STC are observed when Lpe0 and Dsub vary, as shown in Fig. 3(b). During these simulations, the ratio of the driver transistors width/length (W/L) to the access transistors W/L is set to 2 to improve the SRAM stability as well as to reduce the influence of RDD [14], [21]. For a symmetric SRAM structure, the STCs are almost the same by sweeping either V_{SL} or V_{SR}.

To some extent, STCs variations can be regarded as a reflection of the Vth variation which affects the inflexion points of inverters. In the complete Vth model of BSIM4 [22],

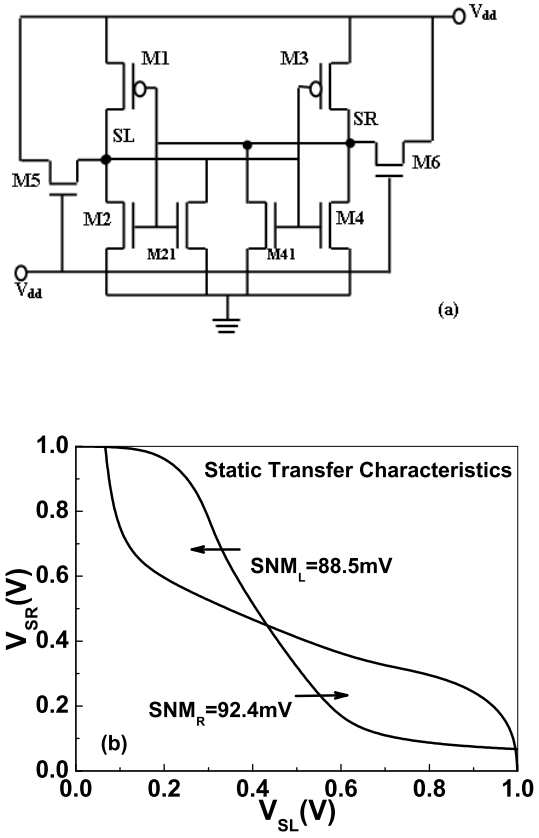

Fig. 2. The circuit schematics and bias configuration for SNM (a), and static transfer characteristics as well as SNM definition (b) of CMOS SRAM cell.

Lpe0 and Dsub have direct contributions to Vth but the other five parameters have not. Therefore, the stability of SRAM cells with respect RDD should be affected mainly by Lpe0 and Dsub. In section III, STCs will be analysed to develop the behavioural model.

In the extreme cases of SRAM STCs, SNM decreases to about 16% of its mean value, so the SRAM performance is affected significantly and the systems may behave abnormally. For the worst cases of Fig. 3(a), although there are some variations, all SRAM cells work almost properly when 5 MPs fluctuate. However, in Fig. 4 the very small SNM of some SRAM cells with 7 MPs changing may result in systems failure and designers must take this into account. Therefore, the behavioural model should reflect the extreme curves as well as the small-scale variability.

III. VHDL-AMS BEHAVIOURAL MODEL DEVELOPMENT

A behavioural model describes the functions of a circuit block by mathematical equations, which give the relationship between input and output. Behavioural modelling has been used to speed up analogue simulation and analogue fault simulation [17], but little work has been done on digital cells.

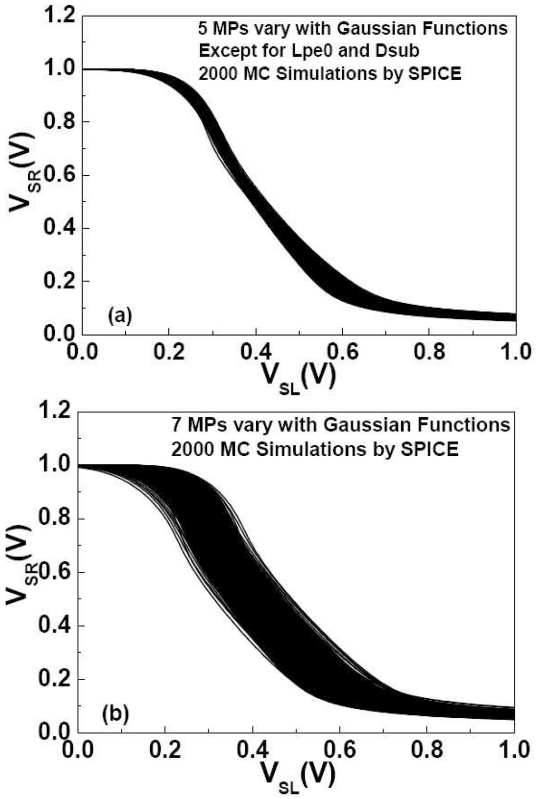

Fig. 3. STCs variations induced by device model parameters fluctuations. (a) shows 5 MPs varying, and in (b) 7 MPs fluctuate. STCs are obtained by 2000 Monte Carlo SPICE simulations.

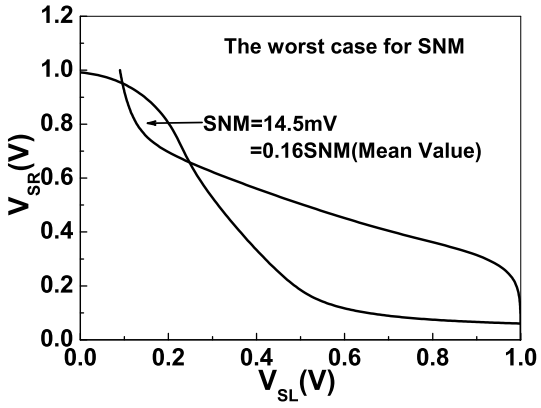

Fig. 4. The worst cases of the STCs for 2000 MC simulations with 7 MPs varying. SNM reduces significantly which may result in failure of an SRAM cell.

In the following, SRAM is used as an example to show the behavioural modelling process.

In general, HDLs are used for behavioural modelling for both digital and analogue electrical systems [23]. Among of them, VHDL and Verilog are often used in digital designs, while analogue HDLs such as SpectreHDL [24] and Verilog-A [25] are usually used for analogue circuits. More than 10 years ago, VHDL and Verilog were extended to analogue and mixed-signal design: VHDL-AMS [26] and Verilog-AMS [25]. In this paper, VHDL-AMS is used to develop the behavioural model.

A large range of STCs in Fig. 3(b) are analysed to extract the relationship between V_{SL} and V_{SR}. STCs have inverter-like transfer behaviour but with smaller slopes and a few humps, which are difficult to describe with the Sigmoidal (S) curves. We used a two-level Sigmoidal function to fit:

$$V_{SR} = P_a + \frac{1-P_a}{2\times[1+e^{(V_{SL}-P_b)/P_c}]} + \frac{1-P_a}{2\times[1+e^{(V_{SL}-P_d)/P_e}]} \quad (1)$$

where Pa, Pb, Pc, Pd and Pe are fitting parameters (FPs).

Fig. 5 shows comparisons between SPICE simulation and Eq.(1). Several different cases are shown including the worst case transfer curves. The two agree for the whole range of STCs fluctuations, and all STCs can be fitted to the equation.

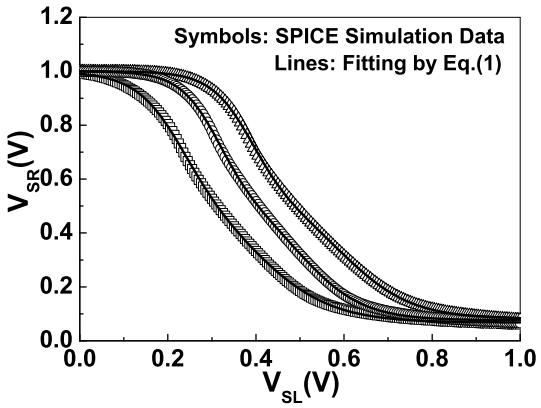

Fig. 5. The nonlinear fitting of SRAM STCs to Eq. (1). The figure shows all STCs can be fitted to the equation.

The VHDL-AMS behavioural model has the normal electrical input and output terminals, as well as five inputs which relate to the five FPs. There should be a definite relationships between FPs and device MPs. As 7 MPs vary simultaneously for each SPICE simulation, it is very difficult to extract the relationships between FPs and MPs. However, not all FPs are independent in a specific SRAM cell. One can develop a behavioural model by finding the potential relationships between the FPs.

Fig. 6 shows the relationship between FPs. The curve-fitting covers the whole range of STCs to give the real range of FPs. It is found the simulated STCs follow Gaussian distributions which means FPs should have normal distributions, and one can extract the means and standard deviations of FPs from the STCs. In Fig. 6, Pb is taken as the independent variable, and we try to find functional relations between other FPs and Pb. If all FPs are given by normal functions independently, some extreme but unrealistic combinations would be produced. The functions in Fig. 6 are used in the VHDL-AMS model.

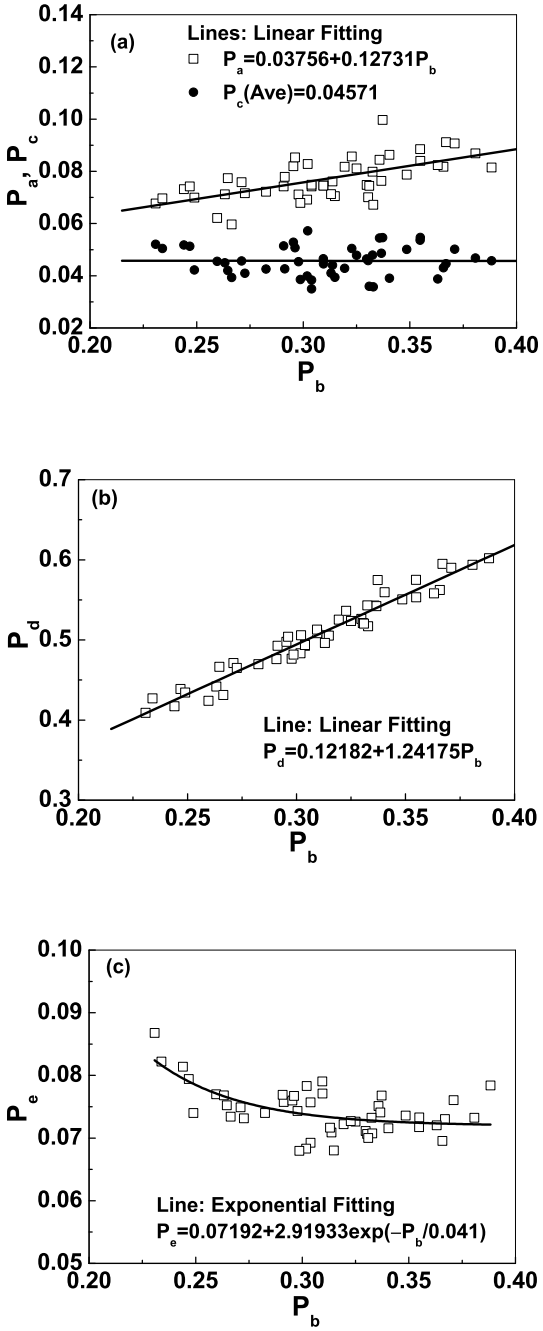

Fig. 6. Relationships between Pb and Pa, Pc (a), Pd (b) and Pe (c), extracted by fitting STCs. The linear and exponential relations are used in the VHDL-AMS behavioural model.

The VHDL-AMS model is comprised of the main entity and architecture implementation, input voltage signal generation, test-bench file and command file, Table I Part I gives terminals and input signals definitions as well as the electrical behaviour of the system, described by Eq.(1). Pb is generated by an independent Gaussian source which is implemented by the Box-Muller method [27]. The other fitting parameters are calculated as shown in Fig. 6. Part II is a linear voltage source applied to SL. The test-bench in part III combines the first two parts for simulation and the command lines of part IV set simulation periods and sampling intervals.

IV. BEHAVIOURAL MODEL SIMULATION RESULTS AND COMPARISON WITH SPICE

The VHDL-AMS model is simulated using a commercial simulator. The behavioural model corresponds to the 8 devices in the SRAM having different MPs, which are set by the normal distributions extracted from real device characteristics. As shown in Fig. 7, the transfer characteristics simulated by SPICE and VHDL-AMS are almost the same both in shapes and in range. The errors result from the approximate fitting of FPs in Fig. 6, as well as the problem of combining dependent FPs in the VHDL-AMS model. The worst cases of SNM extracted from both simulations are shown in Fig. 8, where (a) and (b) correspond to 200 and 2000 MC simulations, respectively. Both figures show that the minimum SNMs are almost the same for SPICE and the behavioural model. Therefore, the behavioural model describes the variability for SRAM with respect RDD.

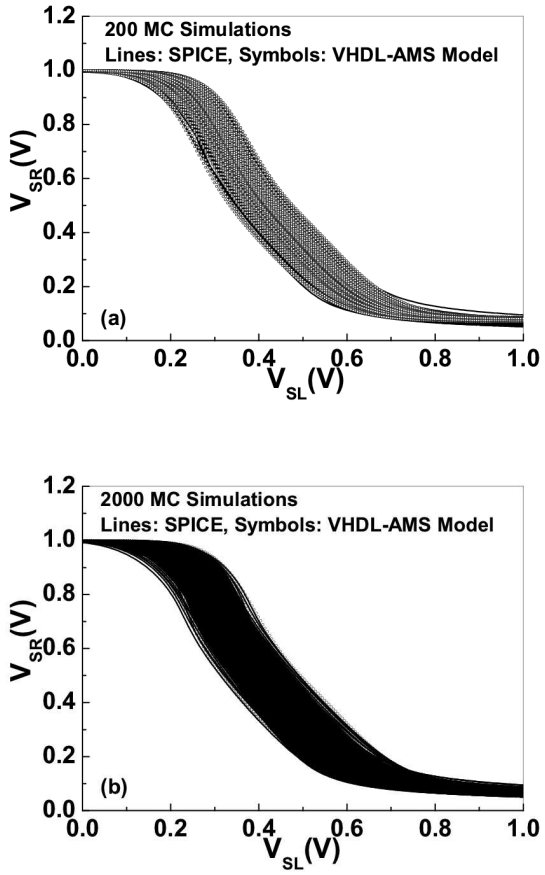

Fig. 7. Comparisons of STCs between SPICE and VHDL-AMS simulations. (a) and (b) show 200 and 2000 times MC simulations, respectively.

TABLE I
THE VHDL-AMS BEHAVIOURAL MODEL DESCRIPTIONS

Part I Main part

```
entity SRAM is
port(terminal SL,SR:electrical);
end entity SRAM;

architecture Behavioural of SRAM is
quantity Vin across SL;
quantity Vout across Iout through SR;
signal Vs1,Vs2:real:=0.0;
signal Pa,Pb,Pc,Pd,Pe:real:=0.0;
begin
p0:process is

variable s1: positive; variable s2: positive;
variable x1,x2 : real; – – Uniform random variables
begin
Uniform(s1,s2,x1); Uniform(s1,s2,x2);
Vs1<=sqrt(–2.0*log(x1))*cos(2.0*math_pi*x2);
– –Box-Muller Method
Vs2<=0.305+Vs1*0.021;
pa<=0.03756+0.12731*Vs2 ;
pb<=Vs2;
pc<=0.04571;
pd<=0.12182+1.24175*Vs2;
pe<=0.07192+2.91933*exp(–Vs2/0.041);

end process p0;

Vout==Pa+(0.5–0.5*Pa)/(1.0+exp((Vin–Pb)/Pc))
+(0.5–0.5*Pa)/(1.0+exp((Vin–Pd)/Pe));
break on Pa; break on Pb; break on Pc;
break on Pd; break on Pe;
end architecture Behavioural;
```

Part II Input Voltage

```
entity Vinput is
generic(vhi,vlo:voltage;thi,tlo:real);
port(terminal SL, SR: electrical);
end entity Vinput;

architecture Behaviour of Vinput is
quantity V across I through SL;
signal pulse:voltage:=0.0;
begin
v==pulse'ramp(1.0E–9, 0.0);
pulse_proc: process
begin
pulse<=vlo; wait for tlo;
pulse<=vhi; wait for thi;
pulse<=vlo; wait for 0 ms;
end process;
end architecture Behaviour;
```

Part III Testbench

```
entity test_sram is
end entity test_sram;
architecture test of test_sram is
terminal SL,SR: electrical;
alias ground is ELECTRICAL_REF;
begin
Vin0: entity Vinput generic map (1.0,0.0,1.0E–9,0.0) port map (SL,ground);
Sram0: entity SRAM port map (SL,SR);

end architecture;
```

Part IV Command

```
* tran.cmd
.tran 1ns 2us 1ns 5ps
.end
```

The behavioural modelling approach has the advantage that the simulations run considerably faster than at transistor-level. Compared to SPICE, the behavioural model improves the simulation times significantly [16]–[18]. Table II shows CPU times for up to 20,000 MC simulations, and an average of five times improvement is found.

TABLE II
COMPARISON OF CPU TIMES FOR TRANSISTOR LEVEL SPICE AND VHDL-AMS BEHAVIORAL LEVEL SIMULATIONS

Simulation cycles	200	2000	20000
SPICE	7.3s	70.95s	893.93s
VHDL-AMS	2.0s	15.0s	145.0s

V. CONCLUSIONS

Random discrete doping (RDD) in the channel increases the variability of the static noise margin of SRAM. This work focuses on behavioural modelling for SRAM with RDD. An SRAM behavioural model was developed using VHDL-AMS. The accuracy of the behavioural model is demonstrated by comparison with SPICE Monte Carlo simulation, and moreover the model speeds up simulation by several times. By using this kind of behavioural model with standard cell libraries, one can get useful design insights without knowing about device-level variability.

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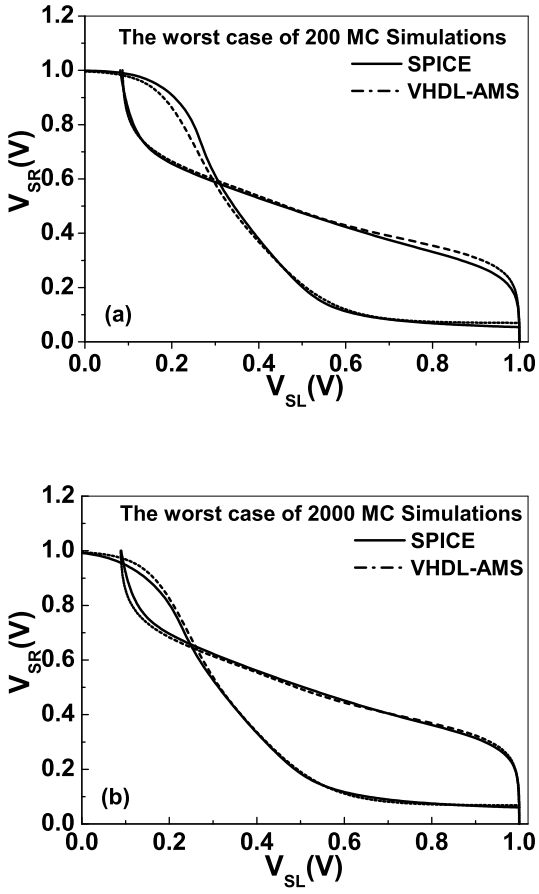

Fig. 8. Comparison of the worst cases of STCs for 200 (a) and 2000 (b) MC simulations between SPICE and the behavioural model.

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