System Level Modeling of Smart Power Switches using SystemC-AMS for Digital Protection Concept Verification

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ABSTRACT
This paper presents a method for the compact modeling, simulation and experimental verification of digital protection functions of smart power switches consisting of a digital controller and a power MOSFET with analog driving circuitry. We focus on short circuit events in an automotive environment where high power dissipation and thermal stress severely affect device reliability. For accurate temperature calculation, a non-linear thermal network including coupling between power transistor channels is used. A digital strategy for over current limitation, short circuit detection and over-temperature shutdown is modeled using SystemC-AMS and verified experimentally using a hardware-in-the-loop system.

1. INTRODUCTION
Smart power switches are used for low-voltage automotive and industrial applications with medium and high current loads. In modern industrial implementations, protection functions are implemented as analog circuits utilizing pn-junction based temperature sensors for over temperature shutdown, current measurement with a shunt resistor and op-amps for the over current limitation as well as a Zener diode clamp circuit protecting the power MOSFET against over-voltages. Over the last decades, these protection concepts of smart power devices have become state of the art. However, the critical parameters involved in these protection strategies are optimized for certain worst-case operating points and cannot be dynamically adjusted to match individual load conditions.

Advanced protection concepts based on non-linear digital control strategies may be applied to address this issue. The overall goal of the presented work is to develop a method to successfully verify such digital control concepts on a system level rather than with a low level mixed-signal simulation. Model development is mainly focused on overload conditions such as shorted loads and transient over-voltage events caused by switching inductive loads. Power MOSFET test structures with integrated temperature sensors are used to validate the models using a custom designed hardware-in-the-loop test bench.

2. MODELING APPROACH
System-C AMS [2] is used to model the behavior of specified loading conditions, digital control concepts and electro-thermal characteristics of power MOSFET transistors. A SystemC-AMS test bench was created to support the simulation of a shorted load.

The block diagram is illustrated in Figure 1. On the analog side an ideal voltage source VBAT represents the battery voltage. The load of the power transistor is modeled using idealized R_{load} and L_{load} elements which represent the line impedance in case of a short circuit. The elements which constitute the MOSFET model are a controlled current source and three capacitances (C_{GS}, C_{DG}, C_{DS}). These elements are connected to form a linear electrical network using primitives of the SystemC-AMS extension library.

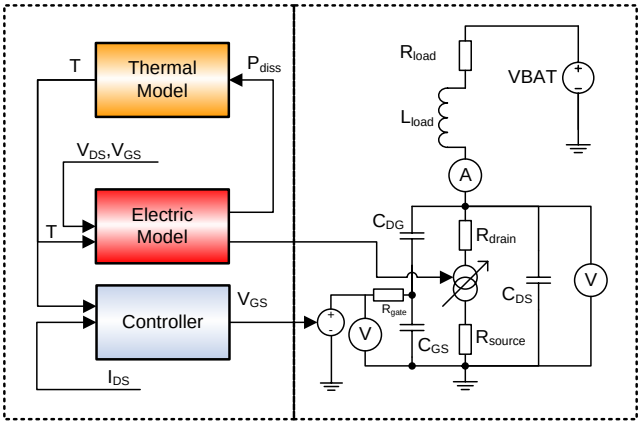

Figure 1 Model of a typical short circuit scenario

On the digital side, the thermal model yields the power MOSFET temperature using as input parameters the power dissipation in the activated power transistor and its ambient temperature. The electrical MOSFET model is used to determine the drain current and drain-source voltage, delivering the instantaneous power dissipation as an input for the thermal model. The controller provides switching and protective functions by regulating the gate-source voltage V_{GS}.

2.1 Electric MOSFET Model
The electric MOSFET model used is derived from well known SPICE transistor model equations. Initially the Schichman-Hodges model or a LEVEL 1 MOSFET model was considered as a simple behavioral model of the power MOSFET. However, this model is generally not regarded as accurate; it may also lead to oscillations in the numerical solution.

Therefore another more accurate model, the so-called “Grove-Frohman” model is used in this work. The Grove-Frohman model as stated in equation 1 results in increased accuracy and better

simulation performance. Moreover, it eliminates abrupt changes in the I/V characteristics of the LEVEL 1 model mainly between linear and saturation region. Further information on both models may be found in [1].

ON region $V_{gs} > V_{th}(T)$

$$I_{drain} = \beta(T, V_{gs}) \begin{Bmatrix} \left(V_{gs} - V_{bi} - \frac{\eta V_{de}}{2} \right) V_{de} \\ -\frac{2}{3}\lambda \begin{bmatrix} (PHI + V_{de} + V_{sb})^{3/2} \\ -(PHI + V_{sb}) \end{bmatrix} \end{Bmatrix} \quad (1)$$

CUTOFF region: $V_{gs} \leq V_{th}(T)$

$$I_{drain} = 0$$

For an accurate transient behavior of the power transistor, proper absolute values of the capacitors C_{DG}, C_{GS} and C_{DS} have to be chosen. In this work, the Meyer [1] capacitance model is used.

In case of a short circuit, the chip temperature increases rapidly within a few hundred microseconds to a maximum of 170°C. This temperature excursion has a significant impact on gain (β) and threshold voltage (V_{th}) [2]. Therefore the temperature dependence of these parameters has to be taken into account.

2.2 Thermal MOSFET Model

It is assumed that heat accumulation and removal from the junction significantly influence the electrical behavior of the power transistor. As stated in equation 2, heat conduction in the simplified one-dimensional case may be modeled in equivalence to an electrical transmission line without transverse conductance and inductance:

$$\frac{\partial^2 T}{\partial x^2} = \frac{c\,\rho}{\lambda_{th}} \frac{\partial T}{\partial t} \Leftrightarrow \frac{\partial^2 U}{\partial x^2} = C'R' \frac{\partial U}{\partial t} \quad (2)$$

where T describes the temperature, x the position in x-direction, λ_{th} the heat conductivity, c the specific heat capacitance and ρ the density of the material. In the electrical case, where the temperature T is substituted by the Voltage U, C' stands for the equivalent electrical capacitance and R' the resistance.

As a consequence of equation (2), heat conduction may be modeled with R-C elements as depicted in Figure 2. The current represents the heat flow and the nodal voltages the temperatures. The coefficients for this so called "Cauer" network [3] can be directly derived from the physical structure.

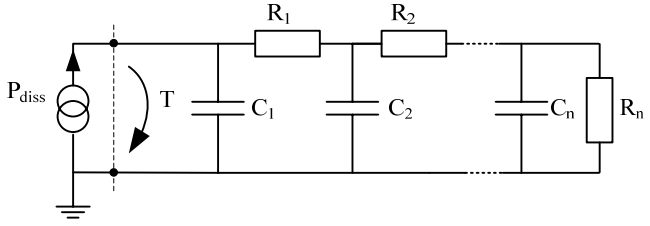

Figure 2 Thermal Cauer network

An alternative approach is the use of FEM (finite element method). This way the thermal step response of thermal systems can be derived directly by transient thermal simulation. As known from system theory, the step response represents the full thermal transient behavior of a linear system. However, it may also serve as a first approximation of the real non-linear system. In case of thermal short at the output (i.e. an ideally cooled backside) the Cauer network can be substituted with a "Foster" network [3] which is shown in Figure 3.

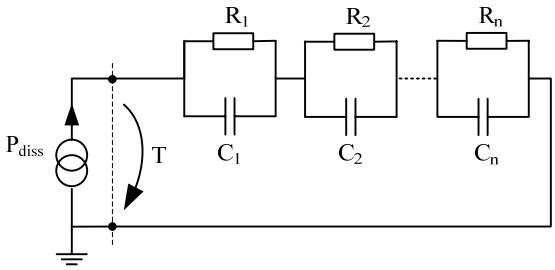

Figure 3 Thermal Foster network

The simple formal structure of a Foster network leads to a compact mathematical description. The normalized current step response (Z_{th} curve) of an *n*-th order Foster network takes the following form:

$$Z_{th}(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-\frac{t}{R_i C_i}} \right) \quad (3)$$

where R_i and C_i are *i*-th thermal resistance and capacitance, respectively. Knowing the Z_{th} curve the RC parameters can be obtained by curve fitting with equation 3. It has to be noted, that in case of the Foster network, the R-C coefficients are not directly related to any physical structure.

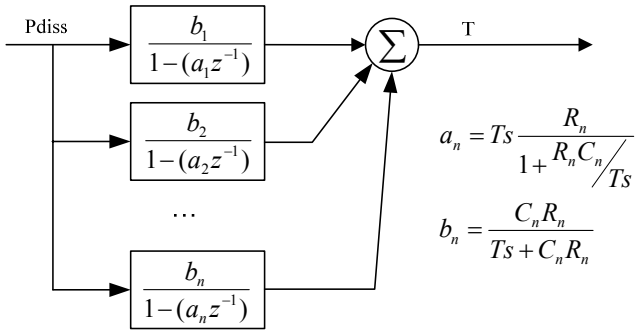

Figure 4 Block diagram of a foster network represented by discrete transfer functions in the z-domain

For digital computing of temperature based on thermal networks, it is useful to express the analog thermal network in its digital (i.e. discretized) representation. The transformation of an *n*-th order analog Forster network into a discrete Forster network transfer function in the z-domain is shown in Figure 4. Again, R_i and C_i represent thermal resistances and capacitances and *Ts* is the discrete sampling period. The filter coefficients a_n and b_n can be calculated from R_n, C_n and *Ts* as shown.

So far the model is considered to be linear and thus temperature independent, usually such an approach is applied if power dissipation density and temperature rise are low. For large temperature deviations the nonlinear and temperature dependent material properties play a significant role [4]. Therefore it is reasonable to implement temperature or power dissipation dependent RC coefficients.

Our approach is to state a dependence between RC coefficients and simulated power dissipation. Introducing these dependence in digital filter coefficients a_n and b_n results in equation 4. During simulation the instantaneous power dissipation in the power MOSFET (I_{drain} times V_{ds}) is used to modify the digital filter coefficients.

$$a_n = Ts \cdot \frac{f_{Rn}(P)}{1 + f_{Rn}(P) \cdot f_{Cn}(P) \Big/ Ts}$$
$$b_n = \frac{f_{Rn}(P) \cdot f_{Cn}(P)}{Ts + f_{Rn}(P) \cdot f_{Cn}(P)} \qquad (4)$$

2.3 Controller Model

In addition to its switching function, smart power switches implement analog protective functions to provide protection for the entire load circuit. In our controller model, a digital current limitation and over-temperature shutdown with automatic restart on cooling is used as a protection strategy.

The current limitation is realized using a P controller sensing the drain current, the over temperature protection using a relay with thermal hysteresis measuring the device temperature. The block diagram of the controller model is shown in Figure 5. The block denoted as PLANT contains the power MOSFET, supply voltage, load and the thermal system. The parameter u_{Temp} represents the over temperature threshold, e_{Temp} is the difference between the measured temperature y_{Temp_sense} and u_{Temp}. u_{ids} is the current limit, e_{ids} the control error and r_{ids} the actuating variable. The brackets indicate sampled signals where H and S represent hold and sample elements. A code snippet of the SystemC code of the controller is shown in Listing 1.

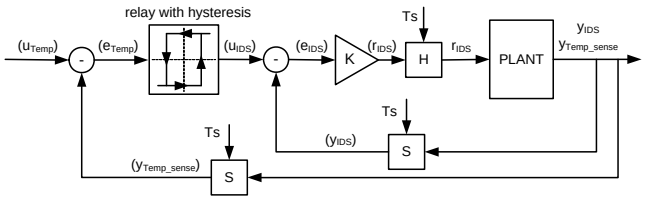

Figure 5 Current limitation and over-temperature shutdown with automatic restart on cooling

Listing 1

```
terror=TLIM-(tamb.read()+tmax.read());
if(terror<=tlimit){    //hysteresis
        currentSet=0; tlimit=TLIMH;}
else{ currentSet=ilim;tlimit=TLIML; }
error=currentSet-imos.read();
vgsset=vgs_prev+k*error;  //p-controller
vgs_prev=vgsset
```

3. TEST CHIP

3.1 Description

The schematic of the test chip is depicted in Figure 6. The test chip consists of eleven temperature sensors and two vertical DMOS power transistors which are different in area. The first power transistor depicted as DMOS1 has a split gate electrode as shown in the schematic. The layout of the test chip is shown in Figure 7. The area of the chip is 2.7 x 4 mm^2 and the thickness is 0.38 mm.

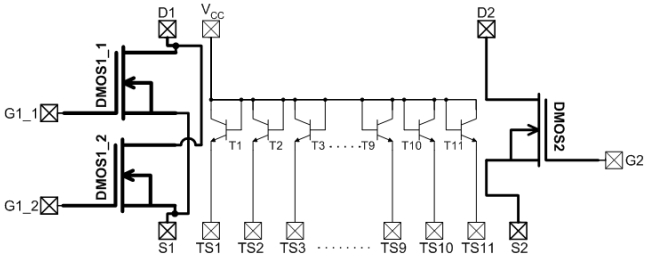

Figure 6 Schematic of the test chip (T1-T11 are bipolar transistors used as temperature sensors) [10]

All integrated devices on the test chip are designed in an advanced smart power technology (SPT) [6]. This technology allows us to integrate bipolar, CMOS and DMOS devices on one chip [7]. Thereby it is possible to integrate accurate temperature sensors using bipolar devices.

In order to connect all input and output signals, the test chip is assembled in a standard P-DSO-28 plastic package (Figure 8). The electrical connections between pins (leads) and particular structures on the test chip are created by gold wires having diameter of 50 µm. The drain, source and gate contacts are created on the laterally extruded parts of the power metallization of the power transistors.

3.2 Temperature sensors

A cut out in the geometrical middle of the active area of both power transistors is made for placement of temperature sensors. The temperature sensors are regularly distributed on a virtual line connecting both power transistors (Figure 7). The distance d between neighbouring sensors is 300 µm.

The temperature sensors are based on the forward voltage drop of p-n junction with increasing temperature [8]. The temperature sensors are created by npn-bipolar transistors where the base is shorted with the collector. Forcing the transistor emitter with constant current, this concept allows temperature measurements with high accuracy up to 300 °C [9].

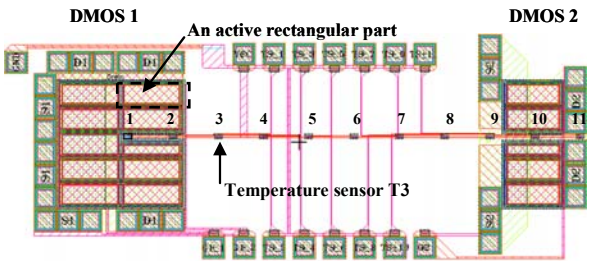

Figure 7 Layout of the test chip [10]

Figure 8 View on the test device. The test chip is encapsulated in the plastic package P-DSO-28 (molding compound partially removed above the test chip) [11]

To be able to calculate the temperature at the integrated temperature sensors from the measured electrical signals, a calibration has been performed. The ambient temperature was controlled by the thermo-stream in the range from −40 °C up to 150 °C. At every temperature step, the electrical signals of the temperature sensors were monitored in real time. If the signal had stabilized at a certain level, this value was taken for the calibration. A sufficient number of temperature steps in the calibration range were chosen to be able to extrapolate the calibration curves to higher temperatures. The calibration points were fitted with a polynomial function of second order for every sensor separately. This approximation is in accordance with the theory of p-n junction thermo-electric behaviour [8].

4. MEASUREMENT SETUP

A hardware-in-the-loop (HIL) system has been developed to investigate digital control and protection concepts and additionally to verify SystemC models. As controlling unit a PCI-FPGA device hosted by a standard workstation is used. This reconfigurable measurement and control device drives the electrical and digital input/output signals of the measurement setup as shown in Figure 9 and can serve as prototype target for controller providing arbitrary protection functions.

The gate of the transistor is controlled by a voltage-controlled voltage source and the integrated temperature sensors are measured by the FPGA device. Variable R_{load} and L_{load} define the short circuit conditions and a GPIB controlled power supply emulates the battery voltage. V_{GS}, V_{DS}, I_{DS} and four temperature sensors are sampled simultaneously and collected by the host PC. In case of a device failure, mainly a drain-source short, the battery voltage is disconnected in less than 2 µsec to prevent any further physical damage.

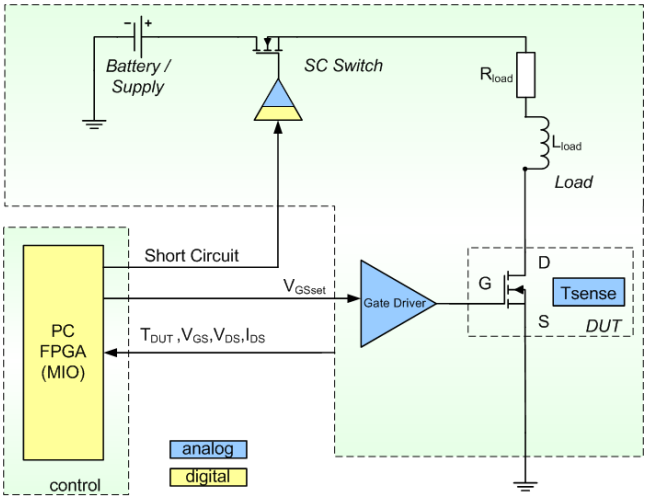

Figure 9 System architecture of hardware-in-the-loop (HIL) test bench

5. RESULTS

5.1 Zth Curves Extraction

Zth curves were obtained using transient thermal FEM simulations. The FEM model of the test chip was built in the FEM simulator FlexPDE. The model is shown in Figure 10. To obtain realistic values the analytical description of the thermal material properties of bulk crystalline silicon was used for the silicon die [12].

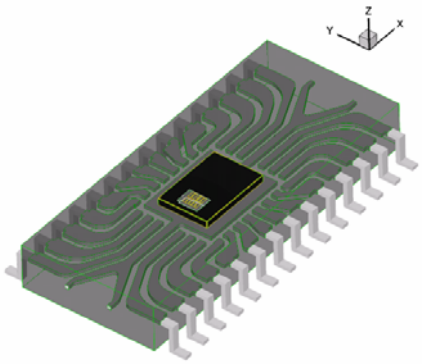

Figure 10 Geometrical model of the test device [11]

The Z_{th} curves were simulated for different power dissipation pulses. This way the power dissipation dependence rather than temperature one could be taken into account. The Z_{th} curves were approximated using exponential functions describing input impedance of Foster networks as shown before. The used network is of third order whereas the optimal order is determined in observing the convergence error during the fitting procedure. The power dissipation dependent thermal resistances and capacitances are shown Figure 11. An enormous dependence of RC coefficients on power dissipation was observed.

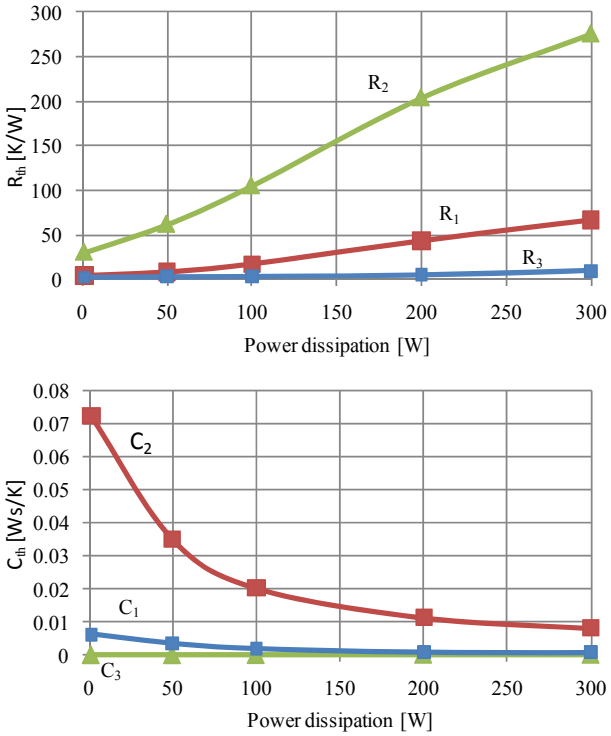

Figure 11 Non-linear thermal RC coefficients of Foster network.

5.2 Comparison Simulation - Measurements

In the first approach a controller with current limitation and over-temperature shutdown with automatic restart and cooling was modeled in SystemC and programmed on the FPGA device. The load is modeled as short circuit with corresponding R=20 mΩ and L=1e-7 H. The test settings are listed in Table 1. The thermal model is implemented as a linear transfer function, supported by the SystemC-AMS extension. The simulation and experiment results are shown in Figure 12. The solid lines are simulated and the dashed lines are measured parameters.

Table 1 Test settings

Vbat [V]	R[Ω]/L[H]	ton [s]	T_lim [°C]	I_lim [A]
10	1e-2/1e-7	1.5E-3	55(+5/-5)	5

At time of 500 µs the controller activates the power MOSFET in short circuit and limits the current to 5 Amps. Under this condition, large power dissipation is generated and rapid self heating occurs. If the temperature exceeds the upper temperature threshold the controller turns off the power MOSFET. The transistor cools down and the controller will restart the device if the temperature falls below the lower temperature threshold. At time of 2 ms the device remains in off state and starts to cool down.

In the cooling phase the simulated temperature starts to deviate upwards from the respective measurements. Therefore the simulated restart is significantly delayed compared to the measured restart. The maximum relative deviation is as large as 20 %.

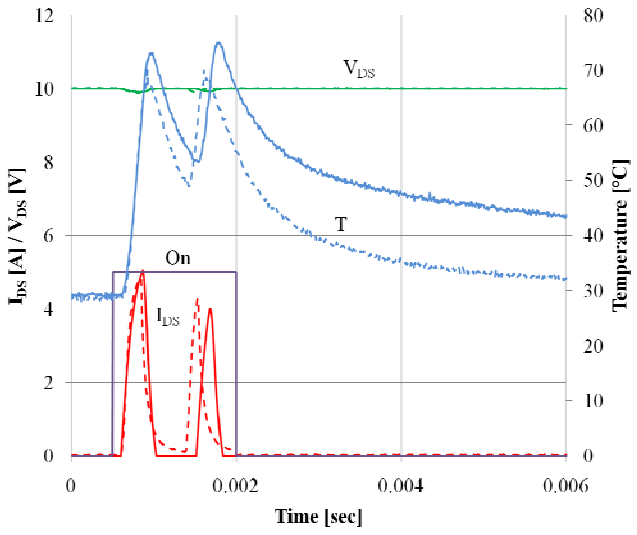

Figure 12 Simulated (solid line) and measured (dashed line) current limitation and over-temperature shutdown with automatic restart on cooling using a linear thermal network.

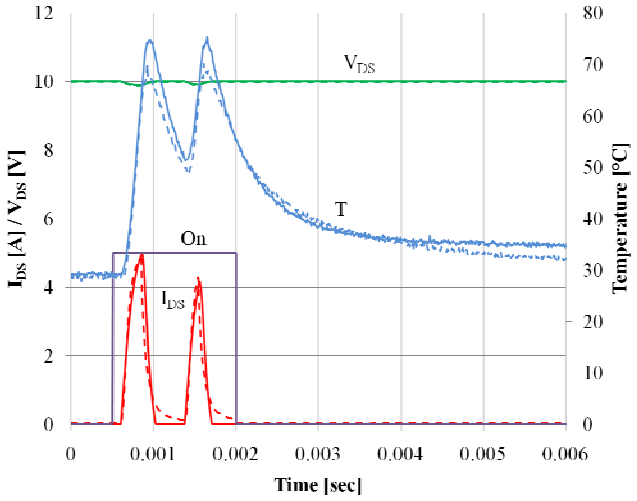

Figure 13 Simulated (solid line) and measured (dashed line) current limitation and over-temperature shutdown with automatic restart on cooling using the proposed nonlinear thermal network.

In the second approach the non-linear thermal network in form of digital filter was used for temperature calculation. The simulation was performed for the same experimental case. Results are shown in Figure 13. Compared to the first approach the simulated behavior agrees very well with the measured one. A maximum relative deviation of about 5 % was observed, which is a great improvement in comparison to the first approach.

6. Conclusion

The presented behavioral modeling approach can be used to develop and optimize digital control and protection concepts of smart power devices under applicative conditions with reasonable accuracy while significantly reducing the simulation effort due to compact models. A virtual smart power switch using a digital controller model, an electro-thermal power MOSFET and a load model were co-simulated. The models were verified using a HIL test bench together with a special test chip. Further we introduced a non-linear thermal network which yields to a significantly increased accuracy while preserving short simulation runtimes.

7. ACKNOWLEDGMENTS

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