An Enhanced Macromodeling Approach for Differential Output Drivers

Ting Zhu, Paul D Franzon
Dept. of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695
Email: {tzhu, paulf}@ncsu.edu

ABSTRACT
This paper presents an approach for building new compact macromodels of differential output drivers. Composed of enhanced physical-based elements, the new models are capable of capturing the important intrinsic nonlinear and dynamic characteristics of the drivers. We demonstrate the approach with two typical digital drivers, low-voltage differential signaling (LVDS) driver and pre-emphasis driver. The obtained macromodels achieve excellent accuracy in capturing behaviors at various input patterns, loading conditions and supply voltages.

1. INTRODUCTION
Good macromodels of output drivers are essential for fast timing, signal-integrity, and power-integrity analysis in high-speed digital systems. A well-known modeling standard is Input/output Buffer Information Specification (IBIS) [1] which is behavioral data taken from actual devices. The IBIS models consist of look-up tables used to characterize I/V output curves, rising/falling transition waveforms and package parasitic information. Despite their commercial success, IBIS models have limitations on timing and noise analysis. Their accuracy is degraded at varying loadings and unstable power supply [2]. They also have difficulty supporting advanced features such as fully differential buffers, pre/de-emphasis and adaptive decision feedback equalizer (DFE). Some refinements are needed to enhance the IBIS models [3],[4].

Another developed approach is parametric macromodeling which exploits mathematical description of current and voltage evolution at the circuit ports [5], [6]. Those methods treat the circuit as a black-box and expose the dynamics by carefully selected input stimulus. Then the obtained data are fitted in model expressions, either Radial Basis Functions (RBF) or splines. Those models are shown capable of capturing effects like crosstalk, SSN, etc. However, they largely depend on the input stimulus and various curve fitting techniques. Also they don’t have a definite physical circuit representation and thus they are difficult to be understood and modified by the users.

In this study, we present an enhanced macromodeling approach for output drivers. The approach is physical-based and all the components of the models can be obtained from port responses by transistor-level simulations. With newly proposed capacitive components, the macromodels are capable of capturing sensitive nonlinear and dynamic behaviors. By charactering the power and ground ports, the impacts of supply and ground variations can be captured by the macromodels. The obtained macromodels are implemented in VHDL-AMS [7] which is very expressive in the mix-signal modeling.

The paper is organized as follows. In Section 2, the proposed macromodeling approach including model structure, characterization steps and VHDL-AMS implementation are presented. All the details are demonstrated with a LVDS driver example. In Section 3, macromodeling of a pre-emphasis driver is discussed. The experiment results are presented in Section 4 and conclusion is addressed in Section 5.

2. MACROMODELING APPROACH

In this section, we present macromodeling of a Low voltage differential signaling (LVDS) driver as an example. LVDS is a dominant differential signaling interface in high-speed digital design [8]. The simple termination, low power, and low noise generation properties generally make this technology the choice for data rates from tens of Mbps up to 3.125 Gbps. A LVDS interface and the simplified schematic of the modeled driver circuit are shown in Figures 1. The circuit is designed in 0.18 μm CMOS process with supply voltage of 2.5 V and operating frequency of 1GHz.

2.1 Macromodel structure
As shown in Figure 2(a), the driver circuit is equivalent to two pull-up (PU) and two pull-down (PD) networks. Data inputs \( D, \overline{D} \) are separated to four input ports \( IN_{PU1}, IN_{PU2}, IN_{PD1}, IN_{PD2} \) that can be controlled individually in modeling. Structure for the proposed macromodel is presented in Figure 2(b).
Current sources $I_u$ and $I_d$ describe nonlinear static output currents which are generally controlled by $V_{in}$ and $V_{out}$. In order to capture the impacts from supply and ground variations, like SSN, behaviors controlled by $V_{s}$ and $V_{g}$ are also modeled.

$C_{ip}$ and $C_{in}$ describe the equivalent capacitive effects between input ports and power/ground, while $C_{op}$ and $C_{on}$ represent those effects at the output. Those components are important to analyze timing and power delivery network.

Different from previous work, we also propose $C_{mp}$ and $C_{mn}$ that are used to capture the coupling capacitive effects between input and output. As the overshoot and undershoot at the output of driver are caused by the intrinsic input-to-output coupling capacitance (for example, due to the gate-to-drain capacitances of the transistors). Therefore, modeling those effects is essential to obtain good dynamic accuracy.

### 2.2 Parameters extraction procedures

#### 2.2.1 Nonlinear DC current

The flow of DC current sources extraction is shown in [Figure 3](#). The first step extracts output voltage regulation effect. Normal supply voltage is used (in this case, $V_s = V_{dd} = 2.5V$). The inputs are set to turn on $PD1$, $PU2$ and off $PU1$, $PD2$. While the voltage source $V_1$ at $V_{op}$ is sweeping from 0 to $V_{dd}$ at a slow slew rate ($1V/100ns$), the current $i_{o1}$ into the port is recorded. Since it’s a differential driver, characteristics of the two outputs are dependent upon each other. Thus, a voltage source $V_2$ at $V_{on}$ is sweeping simultaneously but from $V_{dd}$ to 0. The recorded $i_{o1}, i_{o2}$ are shown in [Figure 4(a)](#). We use piecewise linear approximation for representing the output currents characteristics. The important points are read from the simulation results.

In order to predict the impacts of the supply voltage variations, macmodeling is extended to the power port. In the second step, we set output $V_{on}$ and $V_{op}$ at $V_s/2$ (medium value of power supply). When the DC voltage of $V_s$ is sweeping from 0 to $2V_{dd}$ ($5V$) (to characterize in a large voltage range), the recorded current $i_{o1}$ and $i_{o2}$ are shown in [Figure 4(b)](#).

#### 2.2.2 Equivalent capacitive parameters

The flow of equivalent capacitance extraction is shown in [Figure 4](#). The values are extracted under the typical working condition. In the first step, we set $V_s$, $V_{g}$, $V_{op}$ and $V_{on}$ at 0V. As [Figure 4(a)](#) shows, when sweeping the voltage source at $IN_{PU1}$ from $-V_{dd}/2$ to $V_{dd}/2$ at a fast slew rate ($1V/100ns$), the current $i_o$ at output $V_{op}$ and current $i_s$ at supply port $V_s$ are recorded. The equivalent capacitance $C_{ip}$ and $C_{mp}$ are derived from equation (1),(2).

\[
C_{ip} = \frac{i_o}{dv/dt} \quad (1)
\]

\[
C_{mp} = \frac{i_s}{dv/dt} \quad (2)
\]

By the similar method, by sweeping the voltage source at $IN_{PD1}$ from $-V_{dd}/2$ to $V_{dd}/2$ and recording $i_o$ and $i_s$, the equivalent capacitance $C_{in}$ and $C_{mn}$ are obtained.

\[
C_{in} = \frac{i_o}{dv/dt} \quad (3)
\]

\[
C_{mn} = \frac{i_s}{dv/dt} \quad (4)
\]
In the second step, we turn off all the current sources and set \( V_s \) to \( V_{dd} \). By sweeping the output \( V_{on} \) from 0 to \( V_{dd} \) fast (slew rate \(-1V/10ps\)), the current at \( V_s \) and current \( V_g \) are recorded. The output equivalent capacitance \( C_{op} \) and \( C_{on} \) are decided by (5), (6)

\[
\frac{C_{op}}{dv/dt} = \frac{i_o}{dv/dt} \tag{5}
\]

\[
\frac{C_{on}}{dv/dt} = \frac{i_o}{dv/dt} \tag{6}
\]

2.3 VHDL-AMS implementation

List 1. LVDS driver macromodel (partial) [7]

```vhdl
library IEEE;
use IEEE.std_logic_1164.all;
library IEEE_proposed;
use IEEE_proposed.electrical_systems.all;

entity lvds is
port(
  terminal out_pos: electrical;
  terminal out_neg: electrical;
  terminal data_p: electrical;
  terminal data_n: electrical;
  terminal vdd: electrical;
  terminal gnd: electrical
);
end lvds;

architecture ideal of lvds is
begin
  up_n_cc : entity work.current_source_p(ideal)
generic map(
    fall_dly => 0.0ps,
    rise_dly => 0.0ps,
    rise_time => 0.0e-12,
    fall_time => 0.0e-12,
    v 1 => v 1 , // Use extracted values for v0,v1,v2
    v 2 => v 2,
    v 0 => v 0,
    vg2=>vg2,
    // For Vgs scaling, use extracted values for
    vg1=>vg1,
    // vg0, vg1, vg2
    vg0=>vg0,
    i 0 => i 0,
    // use extracted values for i0,i1,i2
    i 1 => i 1,
    i 2 => i 2,
    ig2=>ig2, // For Vgs scaling, use extracted values for
    ig1=>ig1, // ig0, ig1, ig2
    ig0=>ig0,
    r 1 => r 2,equal to slopes
    r 2 => r 2)
port map ( data => data_n,
  node_p => vdd,
  node_n => out_pos );
  up_p_cc : entity work.current_source_p(ideal)
  // Omit the entity body
  dn_n_cc : entity work.current_source_n(ideal)
  dn_p_cc : entity work.current_source_n(ideal)
  CAP_Cip1: entity work.capacitor(ideal)
  CAP_Cip2: entity work.capacitor(ideal)
  CAP_Cin1: entity work.capacitor(ideal)
  CAP_Cin2: entity work.capacitor(ideal)
  CAP_Cmp1: entity work.capacitor(ideal)
  CAP_Cmp2: entity work.capacitor(ideal)
  CAP_Cmn1: entity work.capacitor(ideal)
  CAP_Cmn2: entity work.capacitor(ideal)

  entity current_source_p is // Current source Iu, similar for Id
  generic (
    fall_dly, rise_dly: time;
    rise_time,fall_time: real;
    v1,v2,v0,vg2,vg1,vg0: voltage;
    i0,i1,i2,ig2,ig1,ig0: current;
    r1,r2: resistance
    )
  end current_source_p;
```

Figure 4. DC current extraction results

Figure 5. Flow of equivalent capacitance extraction
3. APPLICATION EXAMPLE

The approach described in Section 2 is applied to a pre-emphasis driver. Pre-emphasis is an advanced signal conditioning technique in I/O circuits. Pre-emphasis drivers are able to boost magnitudes of the high frequency spectral components, aiming to reduce Inter-Symbol Interference (ISI) caused by lossy channel [9]. The example circuit is shown in Figure 6 (a). It is designed in 0.18 µm CMOS process with supply voltage of 1.8 V and the operating frequency is 2GHz.

When extracting I/V behaviors, the impact from terminal resistors has to be eliminated. With the information of tap coefficient, the equivalent capacitance at main driver and boost driver stage are characterized. The developed macromodel topology is shown in Figure 6 (b) and it is also implemented in VHDL-AMS.

4. EXPERIMENT RESULTS

4.1 Different loading effects

Two cases are designed to validate accuracy of the LVDS driver macromodel. All the simulation is done in Mentor Graphics’ mix-signal simulation environment SystemVision Professional [10]. The test setup is shown in
The LVDS driver is connected to a differential lossy transmission line (RLGC model) terminated with load resistor. Capacitors represent the characteristic impedance of the package. Transistor-level circuit simulation results are used as references.

(a) Case A, length of TL = 0.75m, \( Z_0 = 50 \Omega \), \( C = 0.5 \text{pF} \), \( R = 100 \Omega \), input pattern “0101”, data rate = 1GHz

(b) Case B, length of TL = 1.5m, \( Z_0 = 50 \Omega \), \( C = 1 \text{pF} \), \( R = 100 \Omega \), input pattern “0101”, data rate = 1GHz

The differential voltage waveforms at the near-end and the far-end of the transmission line are shown in Figure 8.

The accuracy of the proposed macromodel is quantified by computing the maximum relative voltage error and the maximum relative delay error. The delay error is defined as the time difference between the reference and the macromodel response measured for the zero voltage crossing of the output differential voltage. The maximum relative voltage error is defined as the maximum error between the reference and macromodel voltage responses divided by the voltage swing.

As the results shown, in those validations, the maximum relative voltage error voltage is within 3.85% and the relative delay error is within 0.9%. It is seen that the LVDS driver macromodel is capable of capturing the different loading effects well.

The pre-emphasis driver macromodel is also verified for different loading effects. As the test fixture is shown in Figure 9.

(c) Case C, \( Z_0 = 50 \Omega \), \( C = 0.5 \text{pF} \), \( R = 50 \Omega \), random input pattern, data rate = 2GHz

(d) Case D, \( Z_0 = 50 \Omega \), \( C = 0.5 \text{pF} \), \( R = 75 \Omega \) (mismatched termination), random input pattern, data rate = 2GHz

When inputting 128×2 bit pseudorandom bit-signal with 2Gbps data rate, the differential voltage waveforms at the near-end and the far-end of the transmission line are presented in Figure 10. As the results show, the pre-emphasis driver macromodel is accurate in capturing different loading effects and reflections. The maximum relative voltage error is within 4.0% and the maximum relative delay error is within 3%.

4.2 Supply and ground variations

The LVDS macromodel is verified when there are variations at the supply and ground connections. As Figure 11 shows, the ideal power supply \( V_{dd} \) was connected to the power supply port \( V_s \) of the driver through \( L_s \) (1nH) and \( R_s \) (0.1Ω), which represent the parasitic of power and ground rail in real situation.

When the input pattern is “0101”, the testing results of output voltage waveforms are shown in Figure 12. The power and ground bounds are also shown in the Figure. It is seen from the results that when there is voltage
variation as large as 20% of the supply voltage, the maximum relative voltage error is within 4.0% and the maximum relative delay error is within 1%.

5. CONCLUSION

In this paper, we propose a new macromodeling approach for high-speed differential output drivers. Our approach extracts physical-based components which accurately capture nonlinear and dynamic behaviors. By charactering equivalent capacitive parameters at the input and output as well as coupling between them, the macromodel well adapt to different input-pattern and loading conditions. By modeling power and ground ports, the macromodel can capture interference effects when there are variations at the supply and ground connects. All the components are extracted from the port responses. The macromodel is implemented in VHDL-AMS. The approach is applied to two typical output drivers, LVDS and pre-emphasis drivers. The obtained macromodels are proved to be efficient and accurate in simulations.

6. REFERENCES