Fast and Waveform Independent Characterization of Current Source Models

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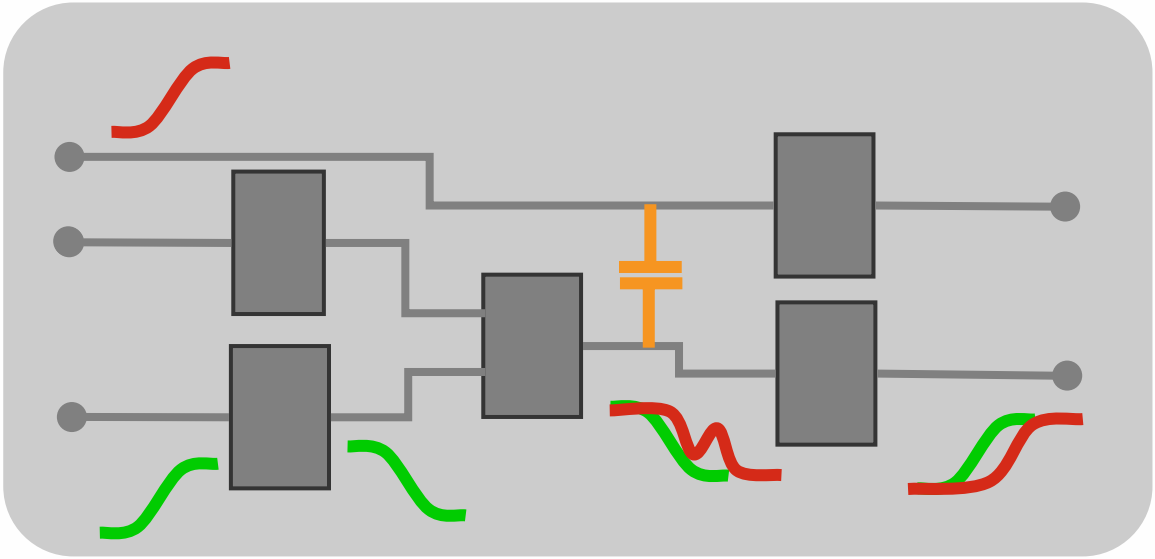
Outline

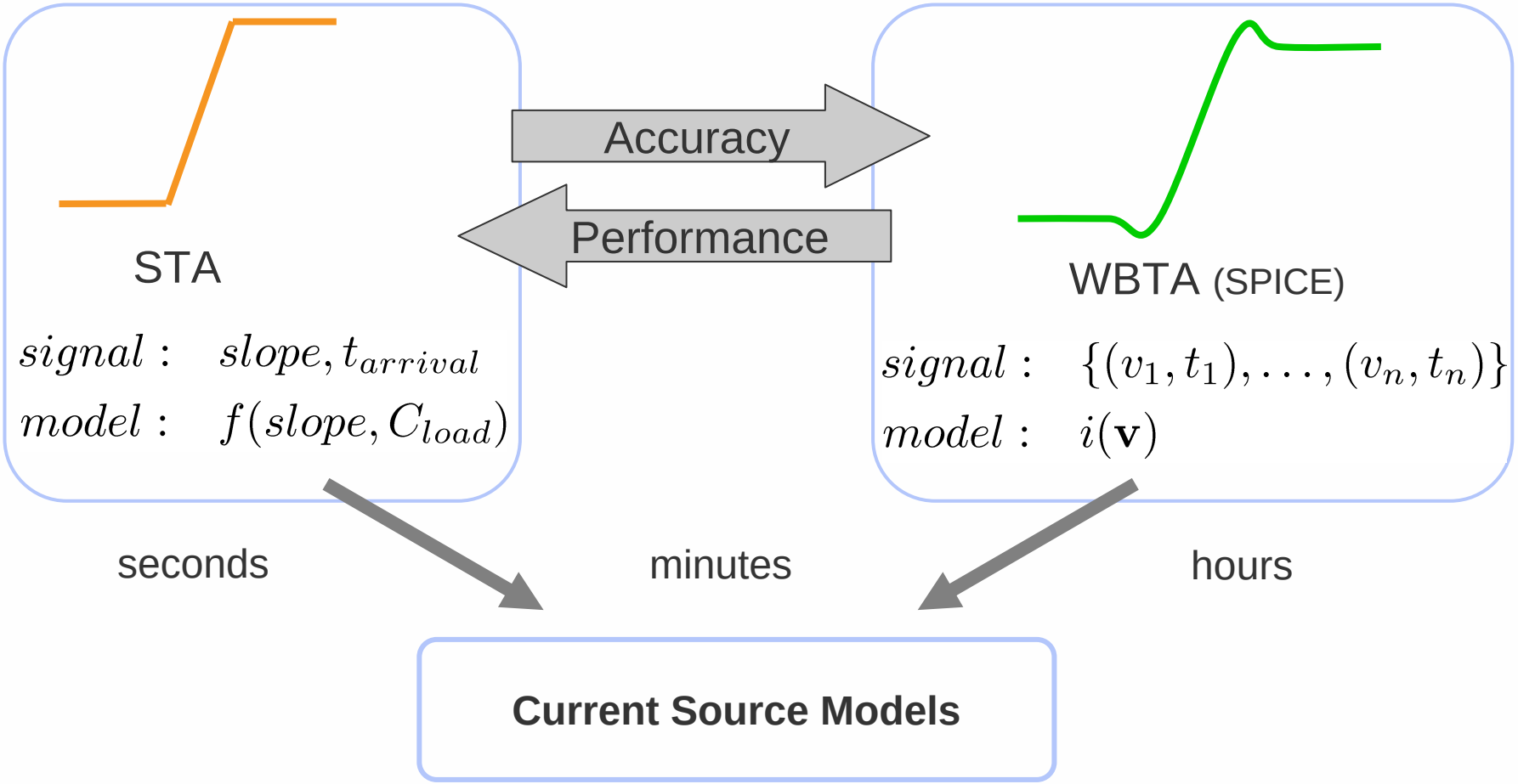
- Demand for more Accuracy
- Current Source Models
- Fast Characterization Method
- Results
- Summary

Actual waveform required for precise timing analysis



- long interconnects
- noise on delay effects
- non-monotonic signals

Comparison of STA and waveform-based timing analysis



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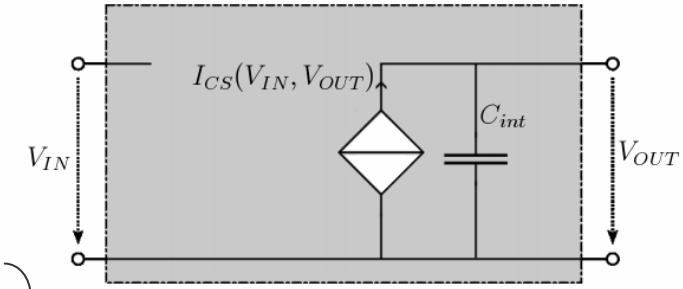
Short overview on existing current source models

- common structure:
  - VCCS for DC port currents
  - capacitances/charges for cell dynamics



- Croix and Wong, *Blade and razor: cell and interconnect delay analysis using current-based models*, DAC03
- Li et. al., *Characterizing Multistage Nonlinear Drivers and Variability for Accurate Timing and Noise Analysis,* 2007 Trans. on VLSI

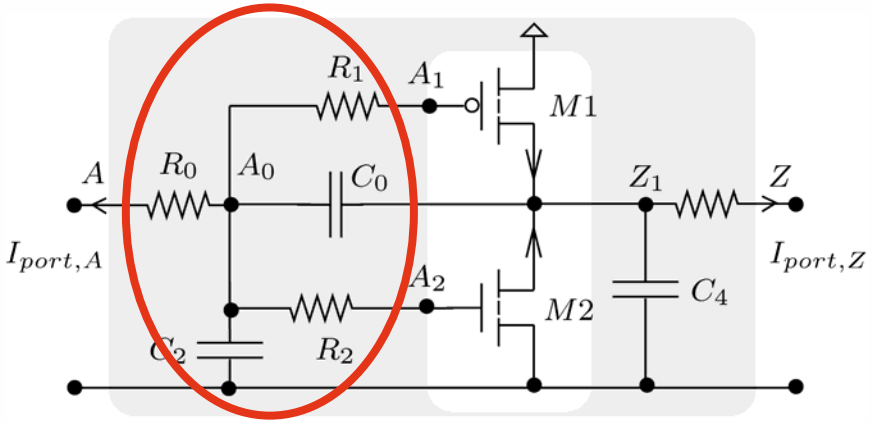
- black box models
- transient simulation
- waveform matching

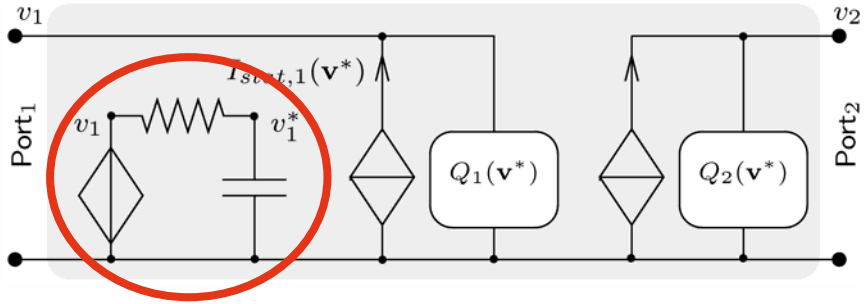
- Amin et.al., *A multi-port current source model for multiple-input switching effects in CMOS library cells*, DAC06
- Kashyap et. al., *A nonlinear cell macromodel for digital applications*, ICCAD07

- structure information needed
- transient / AC simulation

Proposed current source model for logic cell

parasitic delay





CSM

- DC port currents
- port charges
- lowpass filter
  (only large gates)

$$I_{dc,in} = f(v_1^*, v_2)$$
$$I_{dc,out} = g(v_1^*, v_2)$$
$$Q_{in} = h(v_1^*, v_2),\ I_{dyn,in} = \dot{Q}_{in}$$
$$Q_{out} = k(v_1^*, v_2),\ I_{dyn,out} = \dot{Q}_{out}$$

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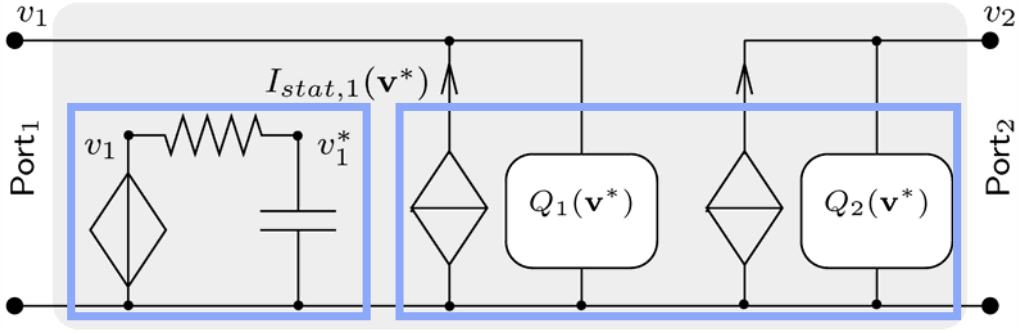
Waveform independent characterization

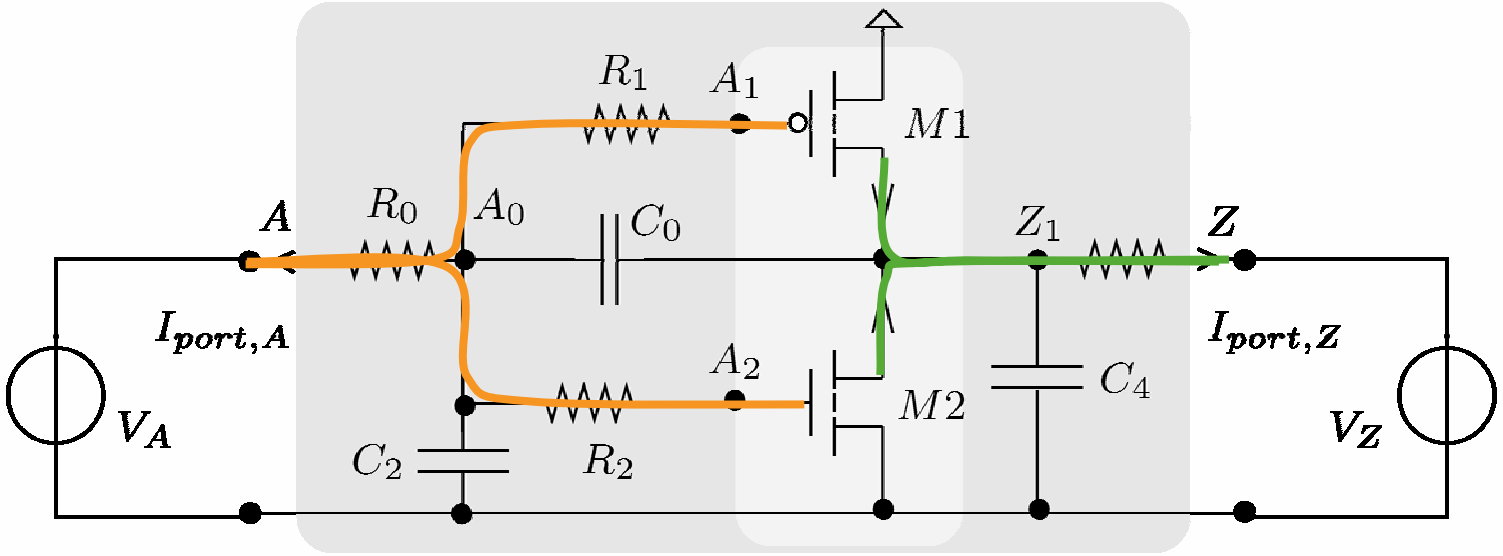


BSIM netlist → Topology analysis → DC sweeps → AC simulation → CSM subcircuit

- Topology analysis: • CCB • measure statements
- DC sweeps: • I(**v**) - LUT • Q(**v**) - LUT
- AC simulation: • lowpass filter

CCB: channel connected blocks, LUT: lookup table

Characterization – DC simulation for port currents

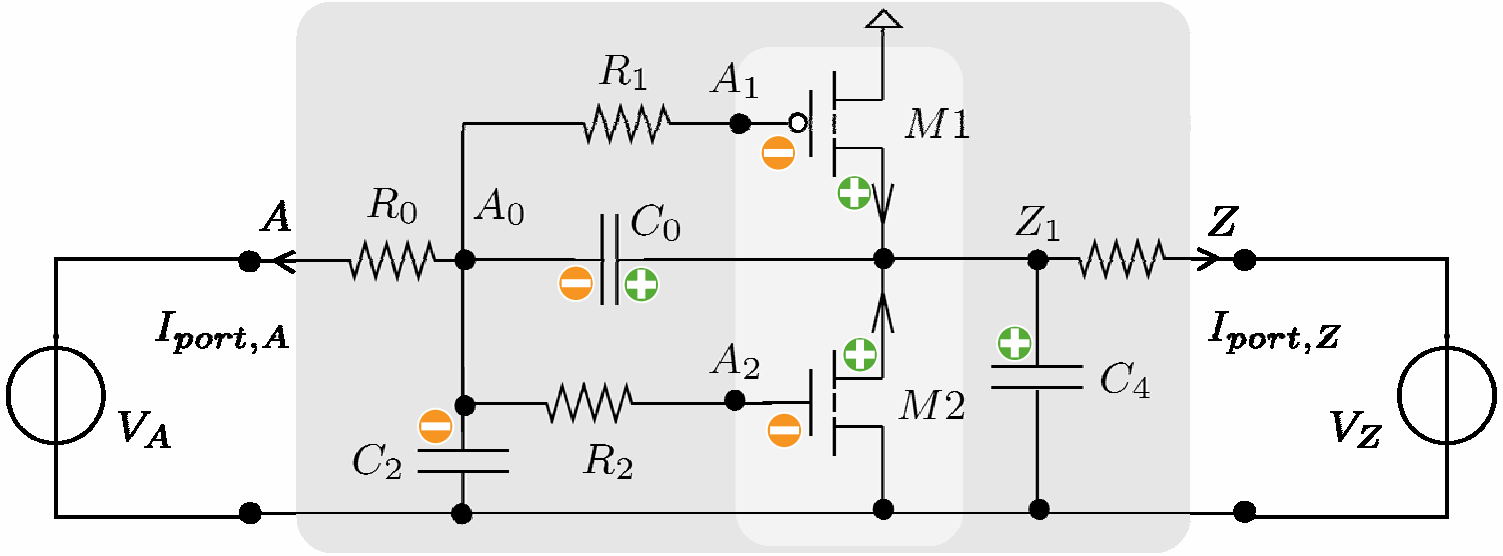


$$I_A = I_{g,M1} + I_{g,M2}$$

$$I_Z = I_{d,M1} + I_{d,M2}$$

Derived from netlist

Characterization – DC simulation for port charges

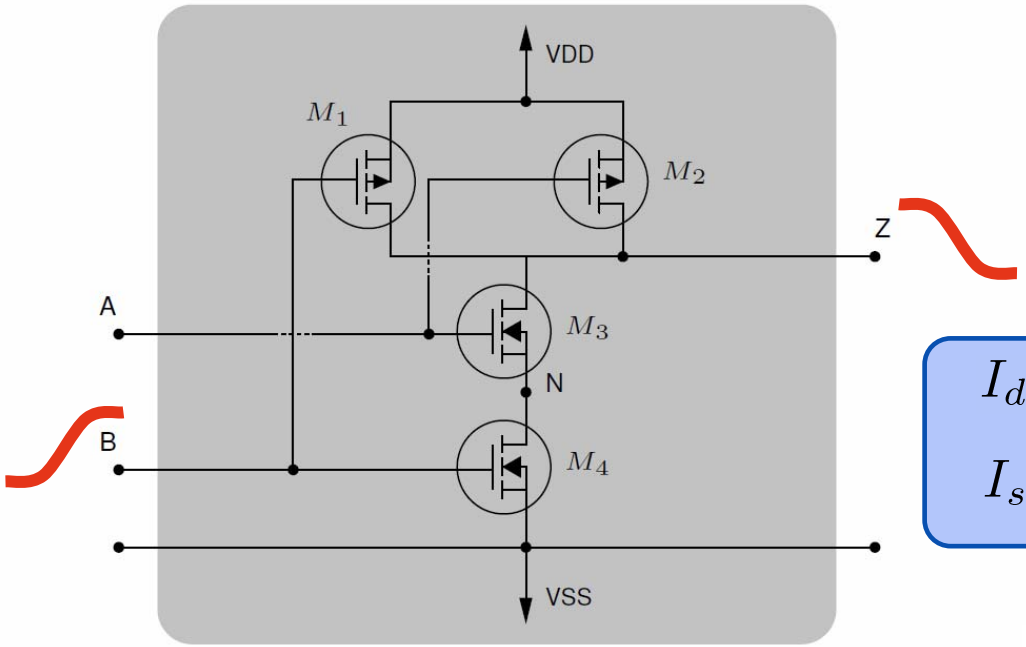


$$Q_A = Q_{g,M1} + Q_{g,M2} + Q_{C_2,A_0} + Q_{C_0,A_0}$$

$$Q_Z = Q_{d,M1} + Q_{d,M2} + Q_{C_1,Z_1} + Q_{C_0,Z_1}$$

Derived from netlist

Characterization - cells with stacked transistors



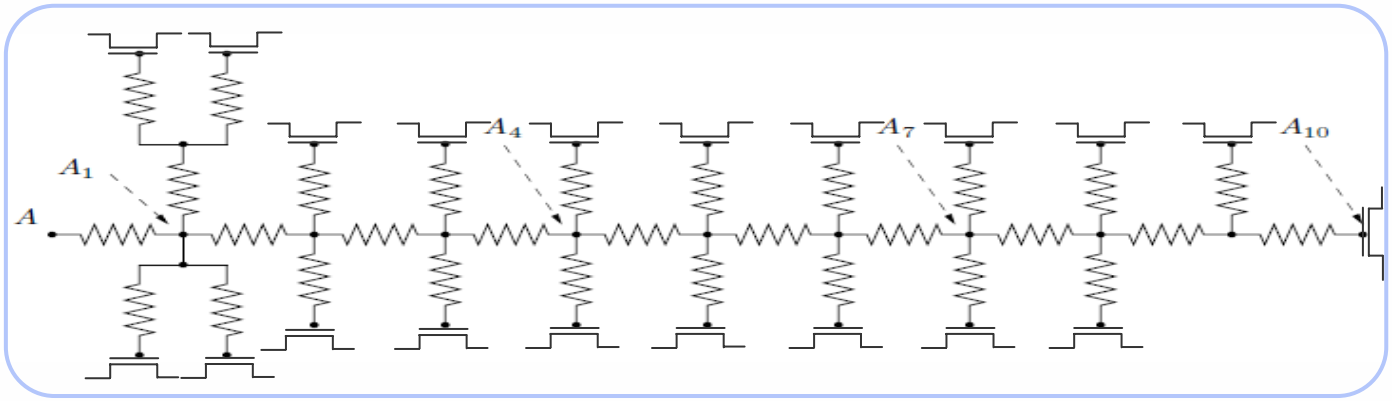
$$I_{d,M3} = -I_{s,M3}$$

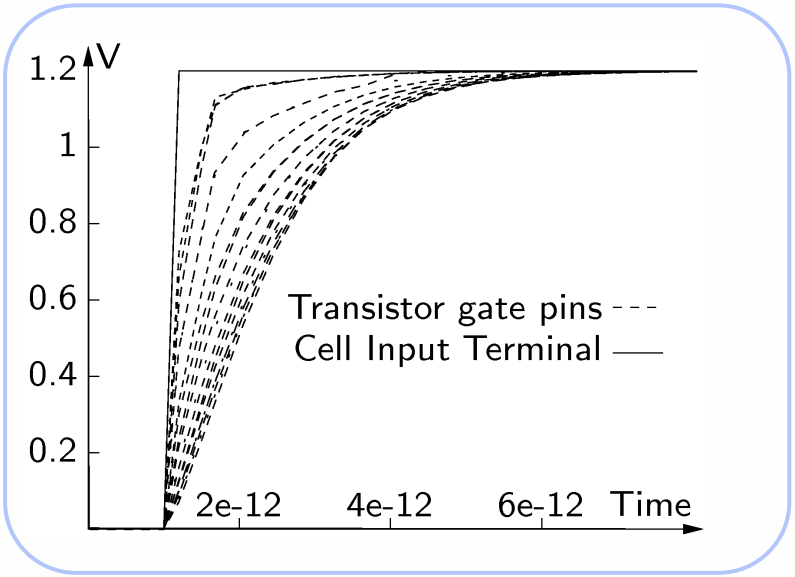
$$I_{s,M3} = -I_{d,M4} + \dot{Q}_{s,M3} + \dot{Q}_{d,M4}$$

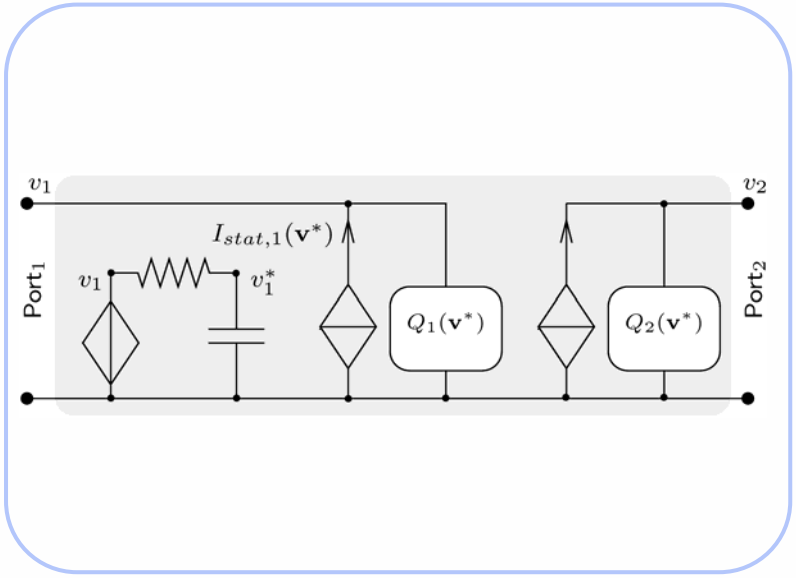
$$I_{\text{out}} = I_{d,M1} + I_{d,M2} + I_{d,M4}$$

$$Q_{\text{out}} = Q_{d,M1} + Q_{d,M2} + Q_{d,M3} + Q_{s,M3} + Q_{d,M4}$$

Voltage approximation error for large inverter (input)







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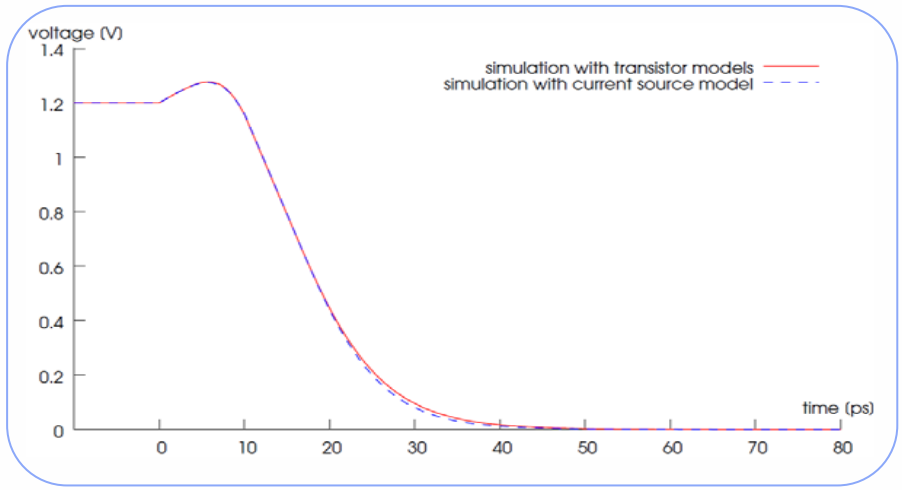
Typical characterization times

Cell	Inputs	FETs	Parasitics	Characterization	
				CSM	TRAN*
2T Inv.	1	2	33	14s	4m 27s
12T Inv.	1	12	136	20s	13m 28s
Buffer	1	60	859	940s	1h 30m
Nand	2	32	482	56s	1h 11m
And	2	24	326	1m 12s	1h 03m
And-Or	8	68	1091	7m 51s	8h 35m

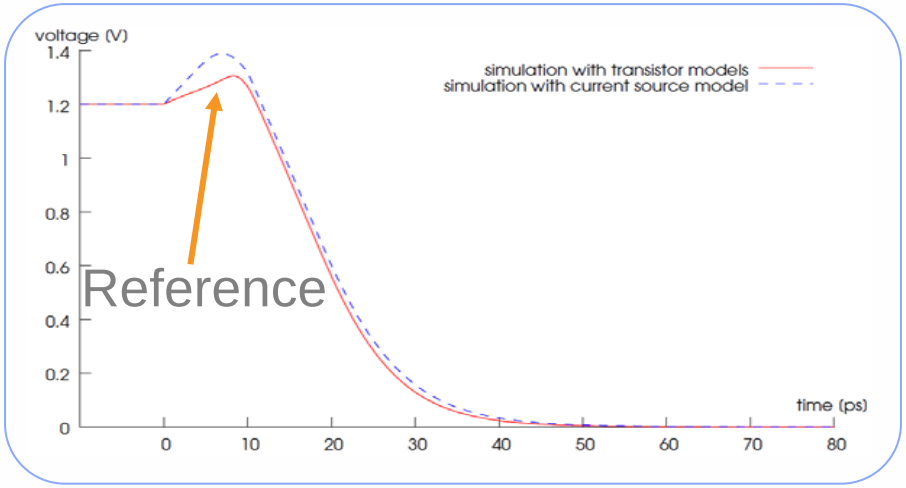
60X

*Amin et al, *A multi-port current source model for multiple-input switching effects in CMOS library cells,* DAC06

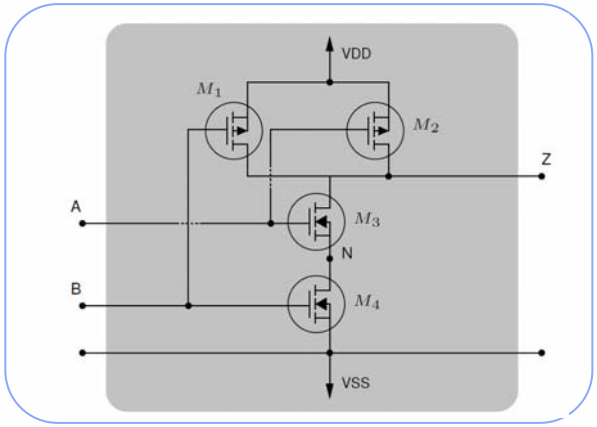
Output waveforms for step inputs (NAND cell)



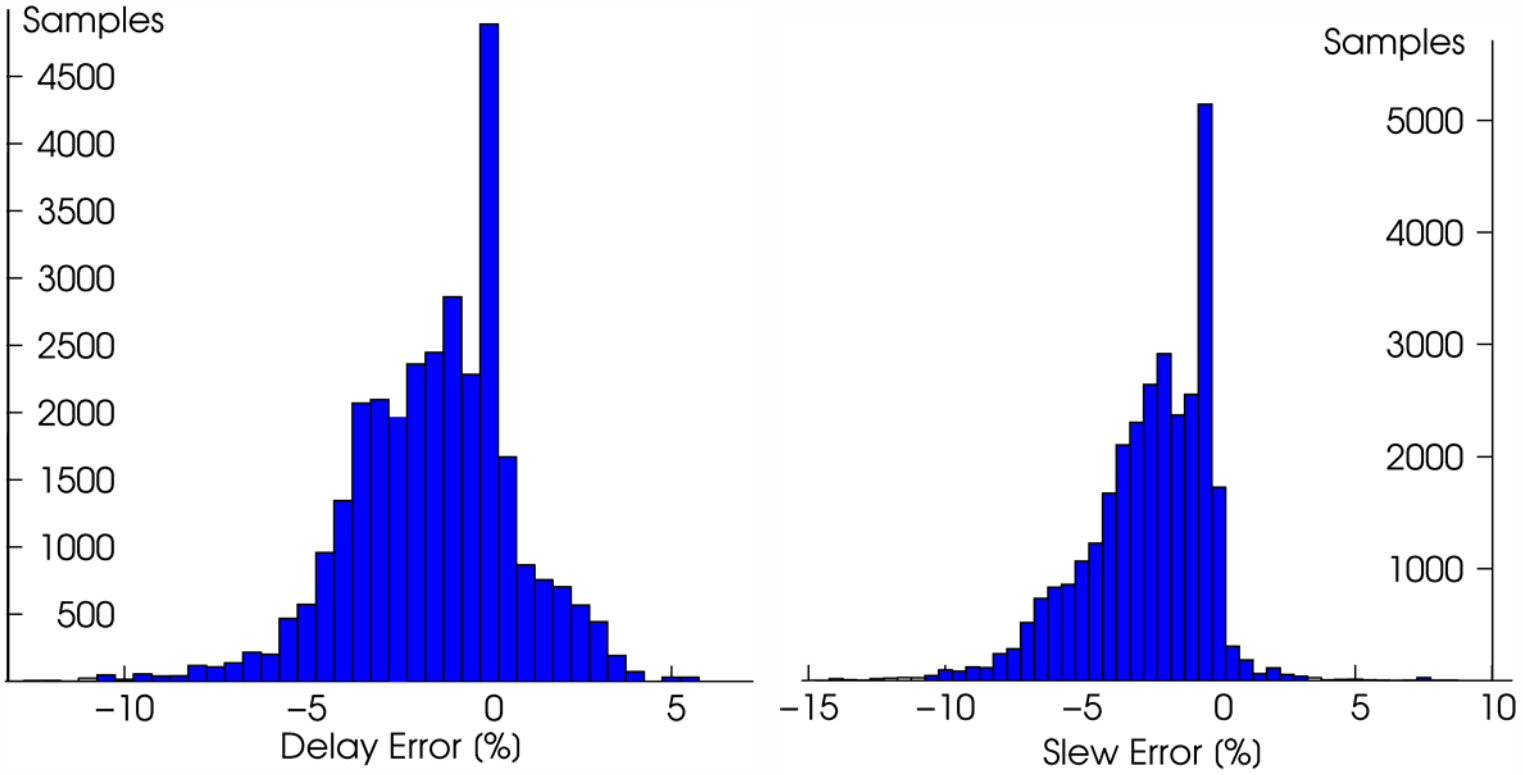
Pin A



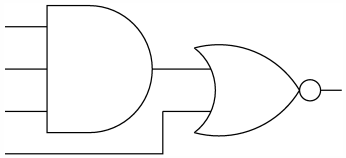
Pin B

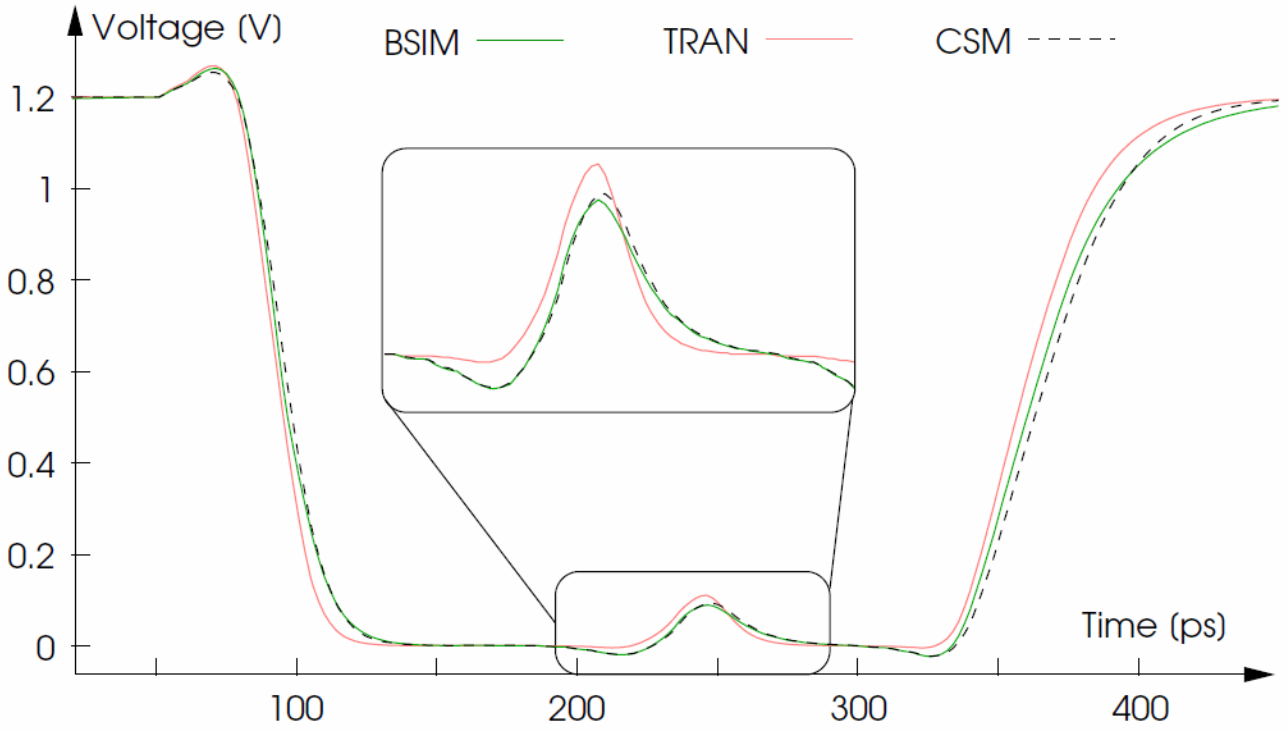


Relative errors for 80 gates, several slope-load combinations

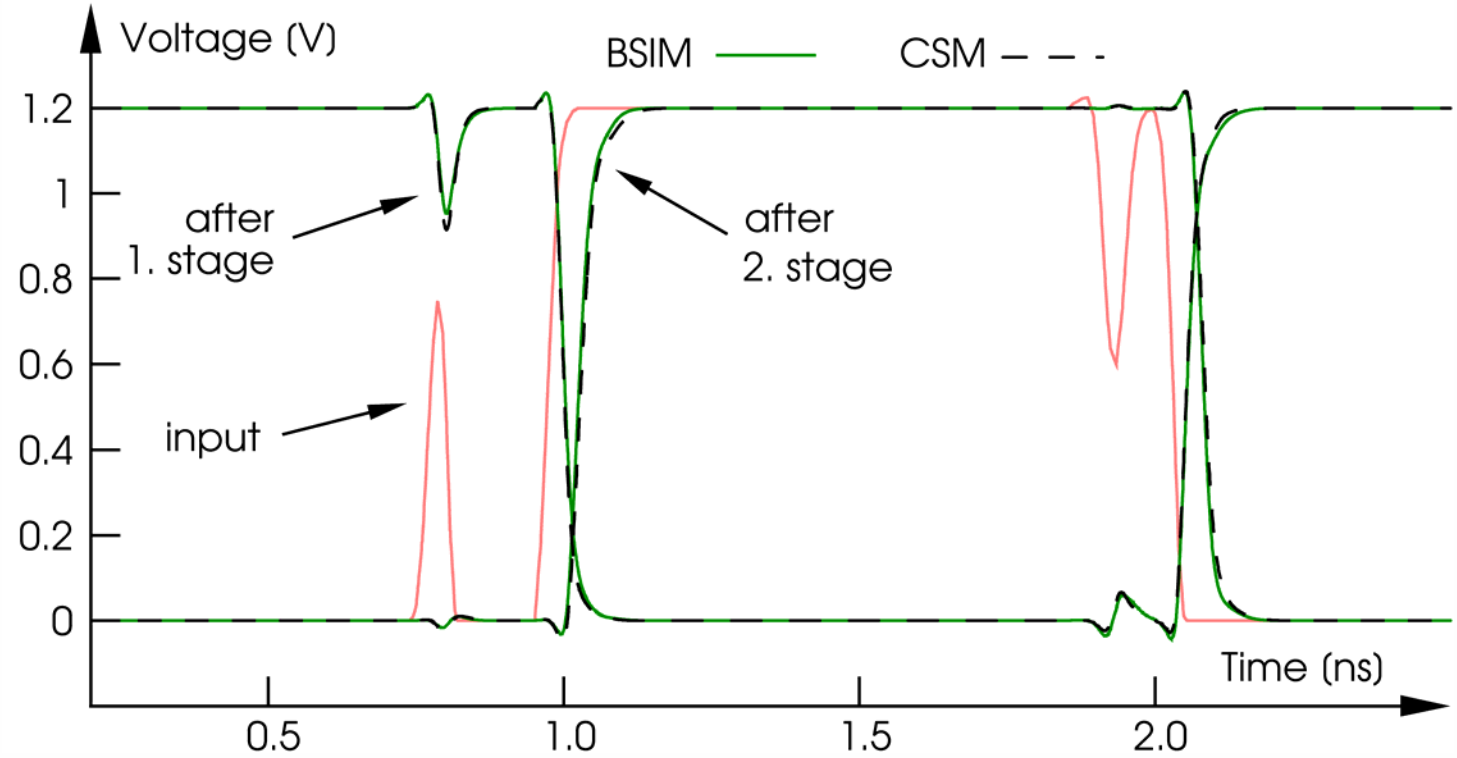


Output waveform for noise attacks





Noisy waveform of concatenated NAND gates



Path-based timing analysis

ISCAS'85 Circuit	Path Length	Delay Error (%)	Slope Error (%)	CPU Time BSIM	CPU Time CSM	Speedup
c1908	42	1.8	1.1	1m 26s	1s	70
c5315	49	2.2	5.1	2m 2s	2s	46
c6288	123	4.6	2.7	16m 16s	7s	107
c7552	42	2.3	6.6	1m 45s	2s	52

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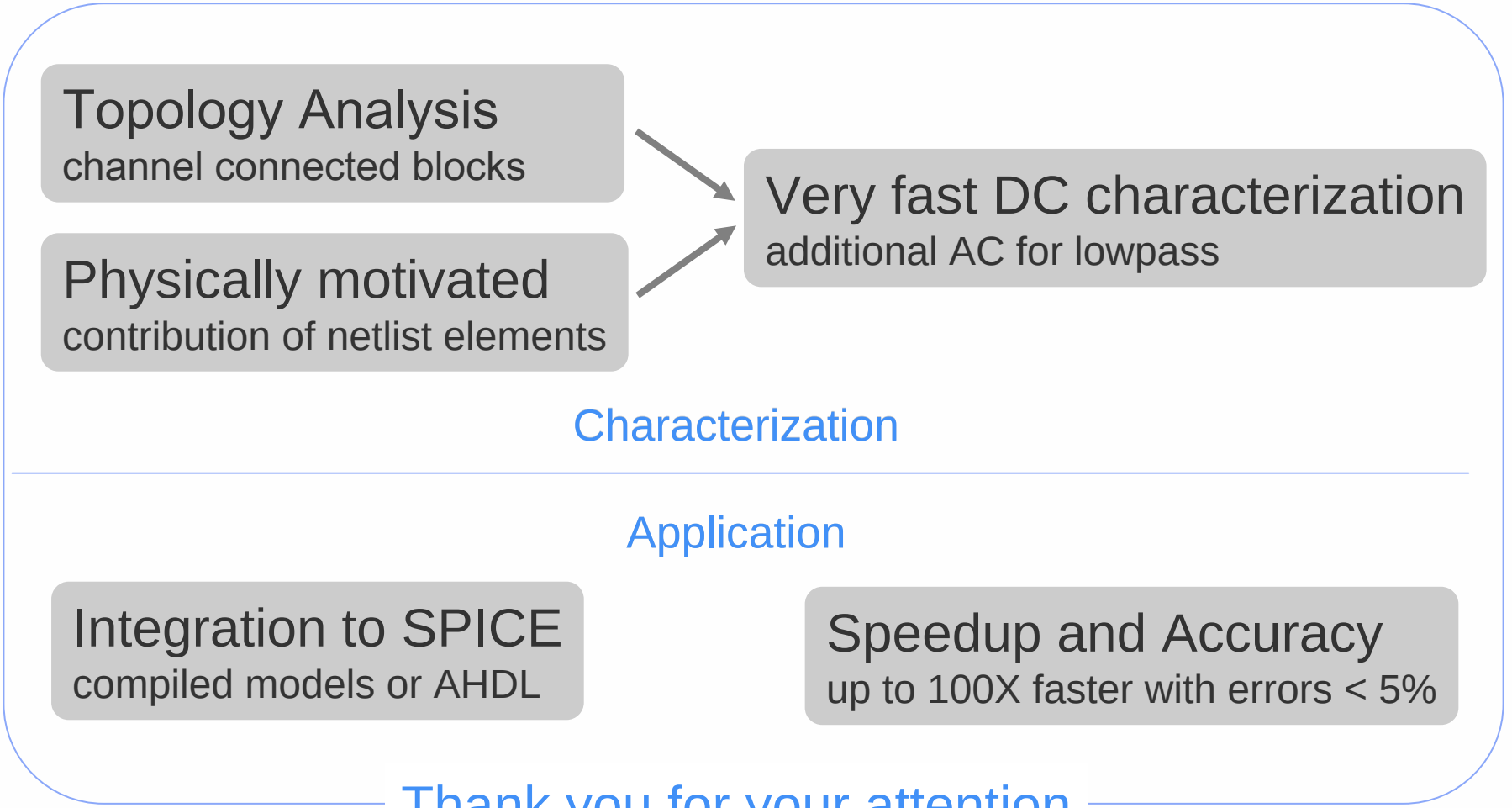
Fast and waveform independent CSM characterization



Thank you for your attention