System Verification of Flexray Communication Networks Through Behavioral Simulations

Candice Muller and Maurizio Valle
DIBE - Biophysical and Electronics Engineering Department
University of Genoa
Genoa, Italy
Email: [candice.muller, maurizio.valle]@unige.it

***Abstract*— Internal vehicle communication networks are becoming highly distributed systems. The increase of the internal vehicle electronic system complexity requires higher performance and reliability, and the necessity of ensuring enough bus signal integrity increases the design verification effort. In this paper we present a system verification methodology of Flexray communication networks through behavioral simulations as well as the analysis of important parameters which influence the communication. The paper presents the verification of different network topologies through mixed-mode behavioral simulations and the evaluation of the most critical aspects of the physical layer. Modifications in the original topologies have been performed, and their effects have been analyzed. Additionally, we give special attention to the computational effort required for the behavioral simulations. The different topologies have been simulated with two bus line models (a lossless and a lossy), and the results are evaluated in terms of CPU usage time and accuracy.**

I. Introduction

The amount of electronics used in vehicle systems is growing fast with the replacement of purely mechanical or hydraulic systems by electronic ones and with the implementation of new functionalities. Thus, the internal vehicle communication networks are becoming highly distributed systems. Unfortunately, the increase of the internal vehicle electronic system complexity requires higher performance and reliability and the necessity of ensuring enough bus signal integrity increases the design verification effort. The development of a network that can properly manage all the electronic control units (ECUs) has become a challenge for the automotive industry.

The automotive industry has recognized the central role of the internal vehicle communication network and, in this context, introduced a time-triggered communication protocol to succeed the event-triggered controller area network (CAN) [1], [2]. Flexray [3] is the communication protocol established by an industrial consortium of leading automotive and electronic manufacturers. This automotive standard hybrid protocol combines time-triggered and event-triggered messages, is fault-tolerant and supports high-speed data communication up to 10.0 Mbps. Moreover, it is very flexible with regard to the network topology: it allows point-to-point, passive linear bus, passive star, active star topologies or any combination of them. This flexibility allows the optimization of the network according to the needs of the application.

Flexray allows implementing more complex and safety critical applications, due to its deterministic approach. On the other hand, it requires higher effort during the design process and introduces numerous new configuration parameters [1]. The hardware components and the network topology have significant impact on the system signal integrity.

Both safety and the economic requirements (cost and time-to-market) dictate to the system tests and verification in the early stages of the design process. The use of prototypes to the design verification is expensive, time consuming and inflexible. Moreover, in most cases, there are no hardware prototypes available in the early stages of the design process.

On the other hand, design verifications can be effectively achieved through behavioral simulations. Different research regarding behavioral modeling of in-vehicle communication systems has been reported in literature. A virtual environment of a complete CAN network is presented in [4]; it also highlights the importance of simulations of in-vehicle networks at the early stages of the design process in order to reduce the number of prototypes and consequently, cost and time to market. The work presented in [5] focuses on the automated simulation-based methodology for the design flow of robust Flexray networks while the TEODACS research project [6] considers the Flexray communication network as a whole, analyzing the internal and external effects which influence the network in the different protocol layers.

In this paper we present a system verification methodology of Flexray communication networks through behavioral simulations as well as the analysis of important parameters which influences the communication, e.g. topology, cable lengths, termination, etc. The paper presents the verification of different network topologies (point-to-point, passive star and linear passive bus) through mixed-mode behavioral simulations and the evaluation the most critical aspects of the physical layer (e.g. propagation delay, asymmetric delay, etc.). Modifications in the original topologies have been performed and their effects have been analyzed. Additionally, we give special attention to the computational effort required for the behavioral simulations. The different topologies have been simulated with two bus line models (a lossless and a lossy), and the results are evaluated in terms of CPU usage time and accuracy.

II. Flexray Network Design Challenges

The main challenge of designing a Flexray communication network is ensuring sufficient signal integrity in the analog bus. The network topology, cable lengths, the presence of active and passive stars, and the node terminations can have significant impact on the signal integrity. Moreover, the parameter tolerances (due to manufacturing process, temperature variations, etc.) can cause undesired network behavior. The use of behavioral models for the whole network simulation allows for the early verification of Flexray physical layer network concepts [7].

During the design process, the transmitted and received analog bus waveforms need to be checked against the system specification in order to ensure safe transmissions. Problems on the electrical physical layer can impact the behavior of the entire communication system, compromising the system reliability.

The critical aspects of signal integrity on a Flexray network which must be evaluated during the network design are:

- **Propagation delay:** time between a binary data stream transmission by one node and the data stream reception by another node. The propagation delay depends mainly on the topology of the path. This parameter influences the performance of the Flexray system, and it is relevant to the synchronization precision. The protocol defines the constraints for the propagation delay between two nodes. The designer should minimize the maximum propagation delay in order to achieve an optimum efficiency of the dynamic part and short interslot gaps.
- **Asymmetric delay:** mismatching between negative and positive edge propagation delays. It can be caused by non-symmetric split terminations, non-balanced ESD protection elements, hysteresis of common mode chokes, asymmetric capacitance of single wires in cables, connectors, etc. The asymmetric delay is relevant for the signal decoding due to the limitations of the Flexray decoder module, and it should not exceed a certain level defined by the protocol.
- **Truncation:** the channel may truncate the transmission start sequence. The truncation is the difference of the duration of TSS at sender and duration of TSS at receiver. The truncation needs to be less than the maximum configurable value of the protocol parameter of TSS transmitter duration (gdTSSTrasmitter). The effect of truncation sums up of different portions, which are contributed by active stars and the activity detection in the receiving bus drivers. It depends on the number of active stars in the path from the transmitter node to the receiver node. The truncation is relevant for the bus transition from idle to active.
- **Bit deformation:** the incorrect or missing network termination can cause bit deformation. In certain cases it can degrade the signal to unacceptable levels.
- **Frame stretching:** due to ringing after last bit of the frame, which shifts the channel idle recognition point.

III. Network Components

It is necessary to have reliable behavioral models in order achieve reliable simulation results. For the analysis of a Flexray communication network through behavioral simulations, it is necessary to have the behavioral model of the network components, which are: transceiver (bus driver), termination, common mode choke, ESD protection elements and transmission line.

The behavioral models which compose the system are described in VHDL-AMS hardware description language [8], which is an industry standard modeling language and is widely supported by available mixed-mode circuit simulators. Furthermore, it provides features for modeling analog, digital and mixed-mode systems and it provides to use of multiple energy domains, such as electro-mechanical, electro-optical and thermal-electrical systems, thus allowing for the complete automotive embedded system modeling (including sensors and actuators).

A. Transceiver

The transceiver is a mixed-mode interface between the communication controller and the analog bus line. It is responsible for converting the digital controller instructions into analog signals on the bus lines and vice-versa, thus it is directly related to the bus signal integrity.

[9] describes in greater detail the mixed-mode behavioral model of the Flexray physical layer transceiver used in the simulations presented in this paper. The model is developed in VHDL-AMS hardware description language [8].

B. Termination

The termination is an important aspect to the analog bus signal integrity. It should match with the transmission line impedance, guaranteeing the maximum energy transfer and ensuring no signal is reflected in the end of the transmission line. In the case of impedance mismatching, this reflection decreases the signal integrity. Flexray does not prescribe a certain termination concept, but it gives some recommendations about termination for certain network topologies. In order to achieve better EMC performance, the specification recommends to use split termination in all ECUs [10].

C. Common mode chokes

A common mode choke may be used to improve the emission and immunity performance. The function of the common mode choke is to force the current in both signal wires to be of the same strength, but opposite direction. Therefore, the choke represents high impedance for common mode signals. The parasitic stray inductance should be as low as possible in order to keep oscillations on the bus low. The common mode choke should be placed between transceiver and split termination [10].

The CMC behavioral model is implemented through the transformator equations:

$$v_1 = L_1 \frac{diL_1(t)}{dt} + M \frac{diL_2(t)}{dt} + i_1 R \qquad (1)$$

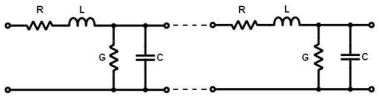

Fig. 1. RLGC transmission line model

$$v_2 = L_2 \frac{diL_2(t)}{dt} + M \frac{diL_1(t)}{dt} + i_2 R \tag{2}$$

where M is the mutual inductance:

$$M = k\sqrt{L_1 L_2} \tag{3}$$

k is the coupling coefficient.

D. ESD protection

To increase ESD protection capabilities of the ECU, additional capacitive loads can be applied between the bus line (BP/BM) and GND.

E. Transmission Line

The transmission line is one of the most critical components for the Flexray communication network simulations. It has a direct impact in the reliability of system parameters, e.g. propagation delay, bit deformation, etc.

A lossless behavioral model from Mentor Graphics Corporation is available in literature. The model is a two-port network which describes the line as characteristic impedance and a time delay. Moreover, it assumes that the signal propagates in the line with no energy loss.

In order to simulate lossy signal propagation, we have implemented the RLGC model. The RLGC model represents the transmission line as an infinite series of two-port elementary components, each one representing an infinitesimally short segment of the transmission line, as shown in Fig. 1.

IV. Transceiver Validation

Aiming to achieve realistic network simulations results, the generic mixed-mode behavioral model transceiver presented in [9] has been tuned in order to represent the NCV7381 device [11] and validated, comparing simulation results with measurements. Fig. 2 shows the DC output characteristics of BP and BM pins and simulation results for Data0 and Data1 representation while Fig. 3 presents the bus signal integrity validation for Data0 and Data1 transmissions. Results presented in Fig. 2 demonstrate that after tuning, the model DC output characteristics match with the real device, accurately representing the slopes and maximum output currents. From the results presented in Fig. 3 it is possible to see that the model accurately represent Data0 and Data1 in the analog bus, as well as the transmission delay from the transmit data input control pin (TxD) to the effective bus line (BP/BM) signal change and the delay from the bus line event detection to the received data output pin (RxD) change.

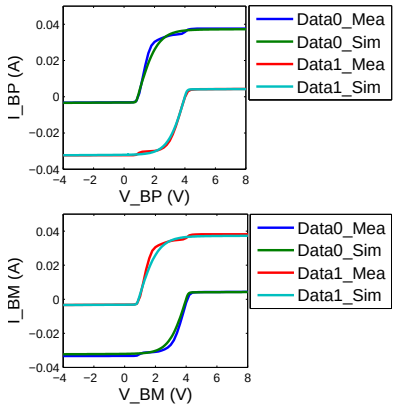

Fig. 2. BP and BM DC output characteristics

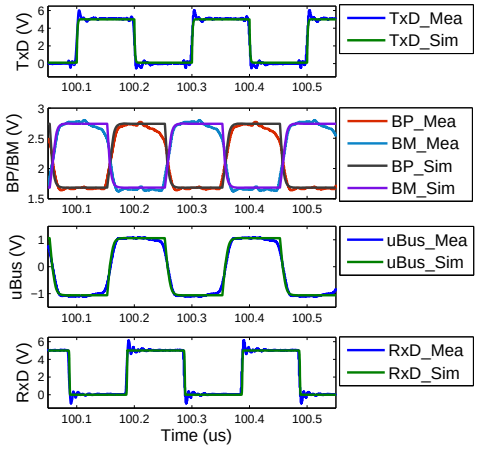

Fig. 3. BP and BM signal integrity analysis

V. Flexray System Verification

The models described in the previous section have been simulated using *Cadence* mixed-signal framework CAD environment (IUS v8.2). Nonetheless, the models fully match the VHDL-AMS standard and are completely portable to any other simulator that supports the language. The PC workstation used to perform the tests was an Intel Core2 Duo, 3.00GHz, 2GB RAM and Linux O.S.

The point-to-point (PTP), passive star (PS), and linear passive bus (BUS) topologies presented in Fig. 4(a), 4(b) and 4(c) respectively, have been verified through behavioral simulations. Each ECU is composed by a transceiver, split termination and ESD protection.

A. Point-to-point

The point-to-point topology has low impedance split termination in both ECUs (2x47Ω+4.7nF), as recommended in [10]. The line length used in the point-to-point topology is 9 meters long. The simulation period is 118.358 μseconds and one frame containing 16 data bytes (8 data words) is transmitted from ECU 1 to ECU 2.

Table I shows the TSS truncation, propagation delay and asymmetric delay parameters calculated from the simulation

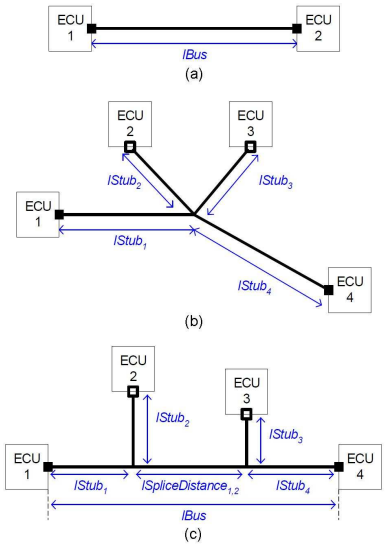

Fig. 4. PTP, PS and BUS topologies

TABLE I
PTP TOPOLOGY PARAMETERS

Parameter	RLGC	Lossless
Propagation delay [ns]	89	82
TSS truncation [ns]	166	168
Asymmetric delay [ns]	1	-1

results. The results presented in Table I show that all the critical aspects of signal integrity are in accordance with the specification, as expected.

B. Passive Star

The passive star topology has a low impedance split termination (2x47Ω+4.7nF) in the two ECUs that have the maximum electrical distance on the bus (ECU 1 and ECU 4) and high ohmic split termination (2x1300Ω+4.7nF) in the other ECUs, as recommended in [10]. The cable lengths used in the simulations are:

- $lStub_1$ = 2.5m;
- $lStub_2$ = 0.6m;
- $lStub_3$ = 1.7m;
- $lStub_4$ = 3.8m.

Passive star topologies tend to reflections at their low resistive center. A series resistance in parallel with an inductance, has been introduced in each branch wire, accordingly with [10].

A Round Robin communication has been performed. Each node transmits a small frame, composed by transmit start sequence (TSS), frame start sequence (FSS), byte start sequence (BSS), one data byte and frame end sequence (FES), which is enough for evaluating TSS truncation, asymmetric delay and propagation delay.

Fig. 5 presents the simulation results comparing the two transmission line models in the period in which ECU 4 acts

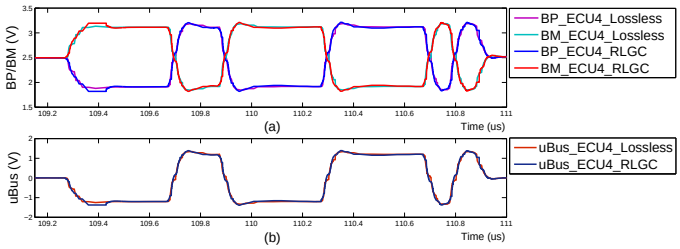

Fig. 5. PS simulation results

TABLE II
PS PROPAGATION DELAY

	ECU 1	ECU 2	ECU 3	ECU 4
ECU 1	33n 33n	62n 63n	63n 63n	89n 89n
ECU 2	69n 69n	33n 33n	56n 56n	77n 75n
ECU 3	67n 67n	54n 55n	31n 31n	75n 74n
ECU 4	89n 89n	69n 70n	70n 61n	33n 33n

as transmitter. Fig. 5(a) shows the comparison between the BP/BM bus line signals on ECU 1, while Fig. 5(b) shows the comparison of the differential voltage on bus (uBus). The uBus waveforms have a correlation coefficient of 0.9945.

Table II and Table III show the propagation delay and TSS truncation parameters, respectively, calculated from the simulation results. The tables show the parameters comparison using the two transmission line models: lossless and RLGC. Each table line represents the transmitter ECU, while each table column represents the receiver ECU. All the upper values of each cell refer to the simulation using the lossless transmission line model, while the down values refer to the simulation using the RLGC transmission line model. All the values are presented in seconds. It is possible to verify that the results obtained with the lossless transmission line are similar to the ones obtained with the RLGC model.

All the parameters are in accordance with the specification, as expected. Results presented in Table II show the propagation delay parameter dependency on the network topology path. As there is no active star in the network topology, the TSS

TABLE III
PS TSS TRUNCATION

	ECU 1	ECU 2	ECU 3	ECU 4
ECU 1	173n 173n	168n 169n	168n 169n	155n 157n
ECU 2	160n 162n	171n 171n	169n 168n	160n 162n
ECU 3	165n 165n	171n 171n	175n 175n	164n 165n
ECU 4	154n 157n	167n 167n	167n 167n	173n 173n

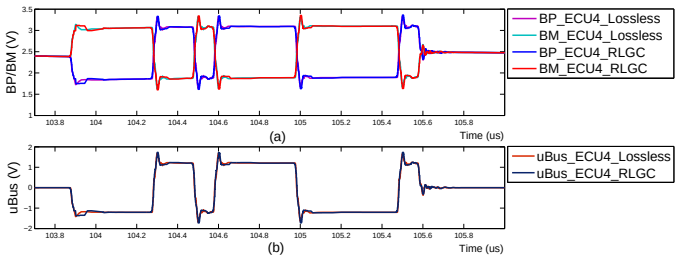

Fig. 6. BUS simulation results

truncation parameter depends only on the activity detection on the receiving ECU. This explain the small variation of the parameter (please refer to Table III).

ECU 1 and ECU 4 cable lengths have been increased, in order to test the transmission line models behavior with the maximum cable length between two ECUs recommended by the Flexray specification. $IStub_1$ has been set 16.2m and $IStub_2$ 7.8m; in this case the cable length between ECU 1 and 4 is 24m. Performing the Robin Round communication with both cable models and comparing the uBus simulation results in all four ECUs, the correlation coefficient of the uBus waveforms is:

- ECU 1 = 0.9985;
- ECU 2 = 0.9962;
- ECU 3 = 0.9950;
- ECU 4 = 0.9986.

This demonstrates an strong correlation between the cable models, even while considering the maximum cable length between two ECUs recommended by the specification.

C. Linear Passive Bus

The linear passive bus topology has a low impedance split termination (2x47Ω+4.7nF) in the two ECUs that have the maximum electrical distance on the bus (ECU 1 and ECU 4) and high ohmic split termination (2x1300Ω+4.7nF) in the other ECUs, as recommended in [10]. The cable lengths used in the simulations are:

- $IStub_1$ = 4.0m;
- $IStub_2$ = 0.6m;
- $IStub_3$ = 0.8m;
- $IStub_4$ = 3.5m;
- $ISpliceDistance_{1,2}$ = 1.0m.

A Round Robin communication has been performed for the linear passive bus topology.

Fig. 6 presents the simulation results comparing the two transmission line models in the period in which ECU 2 acts as transmitter Fig. 6(a) shows the comparison between the BP/BM bus line signals on ECU 4, while Fig. 6(b) shows the comparison of the differential voltage on bus (uBus). The correlation coefficient of the uBus waveforms is 0.9952.

Table IV and Table V show the propagation delay and TSS truncation parameters, respectively, calculated from the simulation results, comparing the lossless and RLGC bus line modes.

TABLE IV
BUS PROPAGATION DELAY

	ECU 1	ECU 2	ECU 3	ECU 4
ECU 1	33n 33n	58n 61n	68n 70n	88n 90n
ECU 2	62n 63n	33n 33n	49n 50n	70n 69n
ECU 3	71n 71n	48n 48n	31n 31n	59n 60n
ECU 4	90n 90n	66n 67n	59n 60n	33n 33n

TABLE V
BUS TSS TRUNCATION

	ECU 1	ECU 2	ECU 3	ECU 4
ECU 1	174n 173n	173n 171n	172n 170n	167n 167n
ECU 2	169n 168n	171n 170n	170n 169n	164n 165n
ECU 3	169n 169n	173n 172n	175n 175n	173n 171n
ECU 4	166n 166n	169n 169n	171n 170n	173n 173n

All the parameters are in accordance with the specification, as expected. A low impedance split termination has been inserted in ECU 2, in order to verify the effects of the DC bus load not in accordance with the Flexray electrical physical layer specification. The specification defines that the DC bus load should be between 40 and 55 ohms. Including low impedance in ECU 2, the linear bus DC load is:

$$R_{DCLoad} = \frac{1}{\frac{1}{97} + \frac{1}{97} + \frac{1}{2600} + \frac{1}{97}} = 31.94\Omega \qquad (4)$$

Fig. 7 shows the comparison of the simulation results with $R_{DCLoad} = 46.75\Omega$ (Sim1), in accordance with the specification, and $R_{DCLoad} = 31.94\Omega$ (Sim2), not in accordance with specification. The results show the decrease of the differential voltage on bus with the $R_{DCLoad} = 31.94\Omega$. The excess of on bus load can decrease the system reliability since the levels of the differential on bus voltage go to levels closer to the minimum requirements defined in the specification (eye diagram), reducing the bus signal integrity [7].

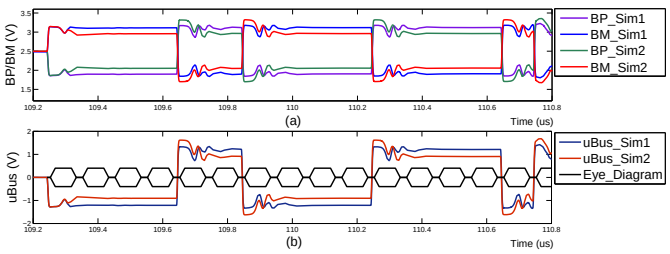

Fig. 7. Network R_{DCLoad} variation

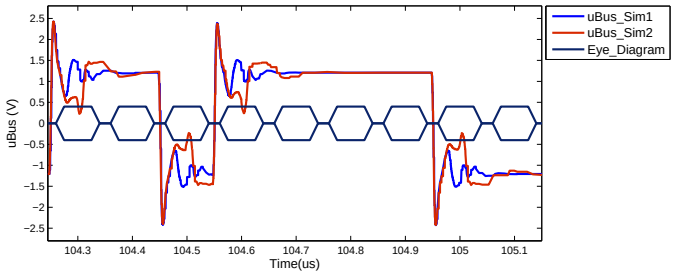

Fig. 8. Network termination changes comparison

TABLE VI
CPU USAGE TIME

Network Topology	RLGC Model	Lossless Model
Point-to-point	3246.6	21.8
Passive Star	3414.0	39.0
Linear Bus	4404.4	34.6

Another change on the network termination has been examined for the linear passive bus. Terminations from ECUs 3 and 4 were inverted, i.e. the ECU 3 termination has been changed to a low impedance split termination and the ECU 4 termination has been changed to a high ohmic split termination. Fig. 8 shows the comparison of uBus between the two simulations (termination compliant with specification (Sim_1) and termination not compliant with specification (Sim_2)) and the eye diagram.

From results presented in Fig. 8 it is possible to verify that the network termination not compliant with the specifications can degrade the analog signal on bus due to reflections. In critical cases, it can completely destroy the signal integrity.

D. Results Analysis

Table VI presents the CPU usage time for the simulation of the point-to-point, passive star and linear passive bus topologies, comparing the use of the lossless and RLGC transmission line models. Values are expressed in seconds.

From the results presented in Table VI it is possible to verify that the transmission line model has big impact in the CPU usage time. The CPU usage time significantly decrease with the use of the lossless transmission line model.

Through the simulation results presented in Fig. 5 and 6 it is possible to observe that the simulation results with the RLGC and with the lossless transmission line models are very similar. Moreover, the results presented in Tables I-V show that the TSS truncation, propagation delay and asymmetric delay has no significantly difference between the values obtained using the RLGC and the lossless models. Taking in account these two aspects, it is possible to say that the system verification of Flexray communication networks can be done using the lossless bus line model, which implies in a significant reduction of the CPU usage time. The advantage in terms of computational effort is still more evident when considering statistical analysis [12]. Although, the RLGC model can be used in the final step of the system verification, in order to guaranty a conservative analysis.

VI. CONCLUSIONS

The paper presents an approach for the system verification of Flexray communication networks through behavioral simulations. Aiming to achieve reliable simulation results, the generic mixed-mode behavioral model of Flexray physical layer transceiver has been tuned and validated (comparing simulation results with measurements) with a real device. The tuned transceiver model has been used for the verification of the critical aspects to be evaluated during the design of Flexray communication networks (TSS truncation, propagation delay, asymmetric delay and signal integrity), for different network topologies. Moreover, modifications in the original topologies have been done in order to evaluate the effects on the network behavior and robustness

Furthermore, the paper compares the two transmission line models (lossless and RLGC) in terms of accuracy and computational effort required (CPU usage time). The lossless model significantly reduces the CPU usage time, maintaining good level of accuracy since the in-vehicle cable lengths are quite short. The reduction in the CPU usage time can be still more relevant when performing statistical analysis. On the other hand, the RLGC model allows the signal access and observability in any point of the transmission line, which is not possible with the lossless model.

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