EMI Modeling of a 32-bit Microcontroller in Wait Mode

Jean-Pierre Leca [1, 2] Nicolas Froidevaux [1] Henri Braquet [2] Gilles Jacquemod [2]

[1] STMicroelectronics
ZI de Rousset, France

[2] LEAT, UMR CNRS-UNS 6071
Sophia Antipolis, France

Contact: jean-pierre.leca@st.com

ABSTRACT

In this paper, a predictive ElectroMagnetic Interference (EMI) model of a 32-bit microcontroller, running in a WFI (Wait For Interrupt) mode, will be presented. The simulated results give a good agreement with the TEM-Cell measurements. In the future, this model will be extended and will be able to simulate the microcontroller in others running modes (digital core running, Flash Memory reading or writing …). The model has been simulated with the help of the ELDO simulator whereas the measurements have been done on a 32-bit STMicroelectronics microcontroller, so-called STXX, following the IEC 61967-2 standard. The aim of this work is to be able to predict, during the design stage, the level of the electromagnetic emissions in order to establish some design or layout rules without simulating the whole product.

Keywords

ElectroMagnetic (EM) Compatibility, EM Interference, EM modeling, TEM-Cell measurements, Microcontrollers, CMOS integrated circuits.

1. INTRODUCTION

Nowadays, with the increasing complexity of products due to the shrink of the CMOS technologies, the EMI issues have become very hot topics, mainly for high-performances Integrated Circuits (ICs) like 32-bit microcontrollers. Indeed, those products generate more and more radiated emissions because of their higher switching current activity and faster signal rise times. Furthermore, higher operating frequencies allow the EM waves rich in harmonics to propagate further into the frequency domain. For markets as automotive, medical or GPS, where the safety is primordial, a low parasitic emission represents a significant marketing argument.

In a first time, in section 2, the EMI generation and propagation mechanisms are presented. Then, in section 3, the construction of the model is explained. Finally, the section 4 shows the simulated results, which have been analyzed and compared with the measurements done with the help of the TEM-Cell. This work is a first step before the building of a more advanced EMI predictive model.

2. BACKGROUND

2.1 Basic EMI mechanisms

2.1.1 Generation of the noise

Within an Integrated Circuit, each switching instance behaves as an EMI generator. Indeed, the origin of parasitic emissions is due to the switching currents which occur at each edge of the clock [1]. In high-performance microcontrollers, the number of switching digital gates is continually increasing, so the current peaks become more important. Indeed, the combination of several hundred thousands of gates synchronized to the clock leads to huge current glitches. In the same manner, with the shrinking of the technology, the switching currents rise time becomes faster. In conclusion, the factor di/dt can become very important.

2.1.2 Generation and propagation of the EMI

From those switching currents, how the electromagnetic field is created and then transmitted? First of all, the power and ground supply networks are forming closed current loops (closed by the external PCB capacitance) which create a magnetic field. Furthermore, as the bonding wires and internal rails are not perfect conductors (parasitic effects due to their equivalent inductances and resistances), those wires convert the transient currents into voltage drops on power and ground supplies. Those voltage drops create an electric field. This type of noise on the supplies is called "S*imultaneous Switching Noise (SSN)*" and can be expressed by the following formula [2] [3]:

$$\Delta V = L\frac{di}{dt} \quad (1)$$

2.1.3 Radiation and reception of the EMI

The electromagnetic field, created by current loops and voltage drops, is then transmitted to its environment by antennas. In ICs, the bonding interconnections and package lead frame both behave as miniature antennas. Indeed, they work like unintentional magnetic and electric dipoles. Finally, unintentional or intentional receivers are able to get the electromagnetic interferences created by the microcontroller.

2.2 EMI Measurements

2.2.1 Setup

A method to quantify the radiated emissions from a device is to use the IEC 61967-2 standard, which employs a TEM-Cell [4] as an EMI receptor [5]. The core of the TEM-Cell consists in a 50Ω adapted metal plate in a grounded chamber. The metal plate is called septum. The microcontroller Device Under Test (DUT) is mounted on the top of a dedicated PCB, designed following the IEC 61967-2 layout requirements, whereas all the connecting leads and passive components are weld on the bottom. The top side of the PCB (where the microcontroller is located) is then put inside the TEM-Cell aperture and is enabled in order to radiate EMI. The setup contains also a 30dB amplifier which is connected to the input of a spectrum analyser, as depicted in Figure 1. Finally, by using a spectrum analyzer, the frequency

spectrum is obtained from the RF voltage collected at the output of the TEM-Cell. The result obtained gives an evaluation of the IC radiated emissions [5][6].

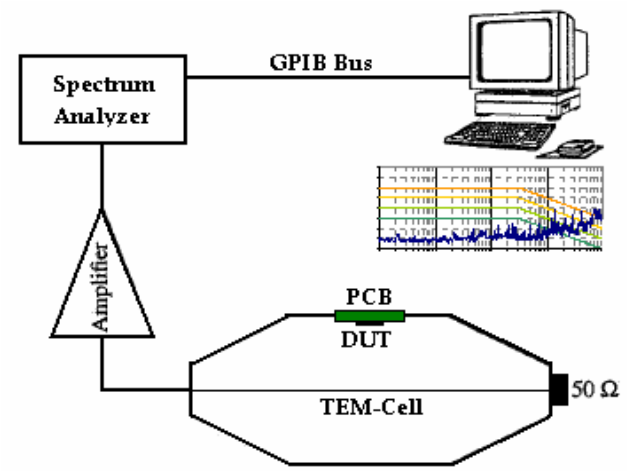
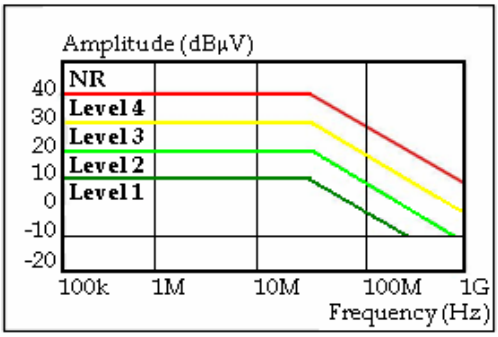


Figure 1. IEC 61967-2 setup

Within the STMicroelectronics Microcontroller Division, five categorization levels (cf. Figure 2), adapted from the IEC 61967-2 standard, are employed in order to qualify the electromagnetic emissions.



Level	Meaning
1	No EMI risk
2	Minor EMI risk
3	Moderate EMI risk
4	High EMI Risk
NR	Not Recommended

Figure 2. EMI categorization levels

2.2.2 Measurements results

The DUT is a microcontroller STXX encapsulated in LQFP 100 pins package. The chip is programmed to run in a low-power sleep mode (WFI). In this mode, the CPU clock is turned OFF but there is no effect on other clock sources. The peripherals clocks are also disabled by the program. In summary, a major part of the digital is disabled whereas the VDDIO33V clock domain is still active. Furthermore, the voltage regulator is ON.

Figure 3 presents the IEC 61967-2 measurement applied on this STXX, which is running in a WFI mode. The device is running at 24MHz.

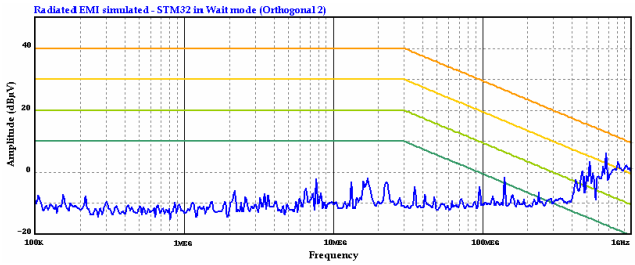


Figure 3. STXX SAE-J1752/3 measurement in WFI mode @ 24MHz (Orthogonal direction 2)

3. EMI MODELING

In this part, the goal is to build an accurate microcontroller emission model. The model should allow the designers to:

- Predict the EMI level during the product design stage.
- Test different design solutions in order to reduce the electromagnetic interferences.

The first approach could be to compute the EMI levels from the entire product back-annotated netlist. This approach, for complex ICs like 32-bit microcontrollers, is not suitable with a transistor-level simulator as ELDO. Indeed, because of the netlist sizes, the execution time and the memory space used by the simulator would be huge. So, the microcontroller behaviour has to be modelled with accuracy in order to reduce the simulation time.

3.1 A model based on the ICEM model

The proposed EMI model is based on the ICEM model (Integrated Circuits Electrical Model) described in the EMC standard 62014-3 [1]. An ICEM model is composed of a current generator, which describes the core internal activity (IA), and a passive distribution network (PDN), which symbolizes the on-chip and the package distribution networks (cf. Figure 4). The model describes the processes of EMI generation and propagation of an IC. The principle is the following: the core generates violent switching currents inside the logic block which propagates through the on-chip PDN, then through the package PDN and finally to the external PCB. So, the parasitic emissions created can be radiated to the external environment.

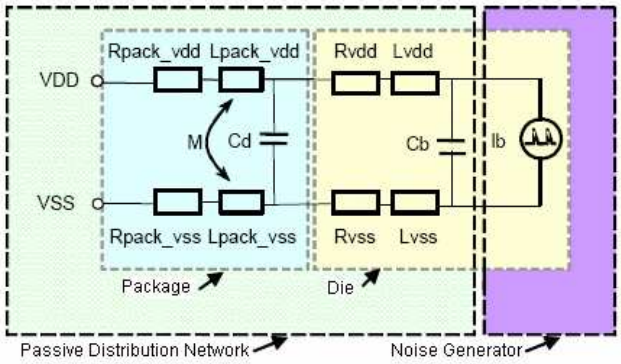


Figure 4. ICEM model of an Integrated Circuit

A majority of models built before, and based on the ICEM model, modelizes the chip current activity with the help of a PWL current source. As the internal current activity is the main parameter to evaluate the EMI, our model takes into account the actual shape of the current consumed by the product, even if it means that the simulation time will increase. The goal is to gain in accuracy. The microcontroller is then studied when running in a Wait mode in order to reduce the number of switching instances. So, only the main IPs (regulator, oscillator, PLL …), instead of being modelized, are totally integrated in the model.

3.2 The chip model

3.2.1 The internal regulator model

The microcontrollers STXX contain an internal regulator which transforms the 3.3V IO supply into a 1.8V core supply. The regulator doesn't have a great influence on the EMI because the current flowing through the IP, once the steady state reached, is a DC current. Though, this IP is integrated in the model in order to supply the others IPs.

3.2.2 The noise generator model

Each IP which provides transient switching currents generates EMI. So only the switching IPs are integrated in the noise generator model. The IPs involved, when the product is running in Wait mode, are the 8MHz Oscillator (OSC) and the Phase Locked Loop (PLL). They are integrated in the model by using their full post-layout spice netlists in order to model the noise generator with a high accuracy.

3.2.3 The internal power distribution network model

The power network distribution of the die plays also an important part in the EMI study. Indeed, each long wire can be considered as an inductance with its serial resistance. Those parameters can be determined by a full product layout (gds2 file) study. The equivalent inductance and resistance for a wire can be computed from its geometry (see Figure 5), by using the formula (2) and (3) [7]. Up to 1GHz, the skin-effect hasn't been considered because of the conductor widths, thicknesses and conductivities [7] [8]. Furthermore, the mutual inductance is not included in this model.

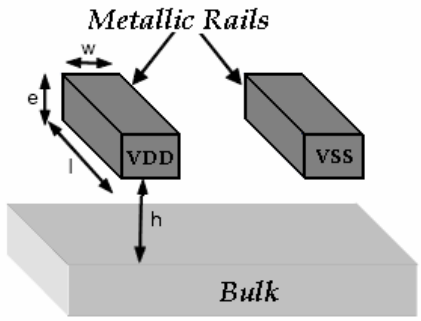


Figure 5. Supply rails geometry representation

$$R_{RAIL} = R_{\square} \frac{l}{w} \quad (2)$$

$$L_{RAIL} = l \frac{\mu_0 \mu_r}{2\pi} \ln\left(\frac{4h}{w} + 1\right) \quad (3)$$

Finally, the capacitances between the power supplies and the die ground have to be considered. The values can be estimated by running AC simulations on the IPs supplied by the different alimentations.

The Figure 6 shows the equivalent RLC network obtained using this extraction method. The grey square symbolizes an IO pad.

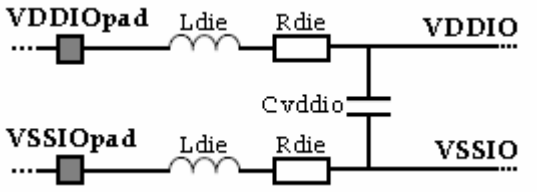


Figure 6. Die power rails RLC model

3.3 The package model

The STXX studied is encapsulated in a LQFP100 package. For this line of high-performance 32-bits products, the number of IOs is still increasing, because of the addition of new functionalities (RTC, USB, Ethernet, CEC…), so the package size is also increasing. Though, in the same time, the size of the chip is shrinking with the evolution of the CMOS technologies. This particularity leads to connect long bonding wires (in addition to the lead frames) between die pads and package pins (see Figure 7). For this reason, package is a huge contributor to the EM radiated emissions because of the inductive coupling. Indeed, the equation (1) shows that the noise amplitude rises with this inductance value.

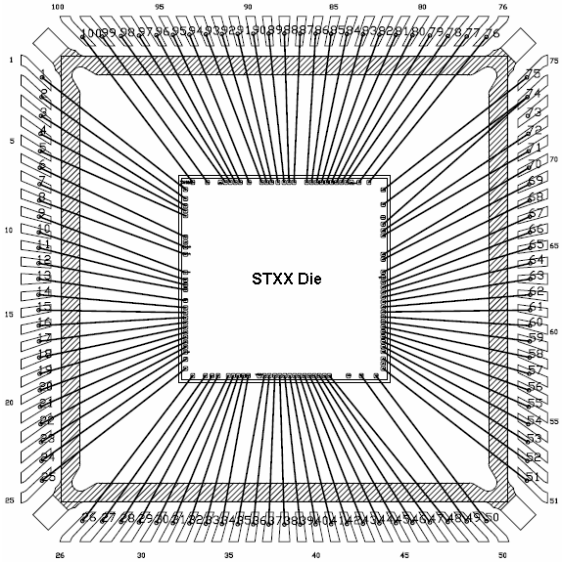


Figure 7. STXX TQFP100 bonding diagram

The package model has been extracted by using the software Ansoft Q3D. This extraction method is very often used as in [9] [10] [11]. This 3D extraction tool solves the Maxwell's equations by using the Finite Elements Method (FEM) or by the Method of Moments (MoM). With the help of a 3D package iterative meshing, this tool can compute the electromagnetic fields in order to extract the package S-parameters. Finally, from the S-parameters, a RLC spice model can be extracted. This model describes each package pin interaction with all the other pins. This model is valid up to 1GHz. The Figure 9 shows an example

of the interactions, for this STXX, between the adjacent supply pins 10 and 11.

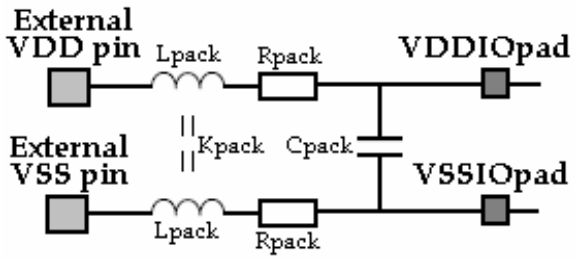


Figure 8. Example of the RLC model of the package

3.4 The TEM-Cell model

The TEM-Cell modeling constitutes the last part of the model. This part symbolizes the intentional receptor behavior. Indeed, the electromagnetic emissions created and radiated by the microcontroller are coupled with the TEM-Cell septum. So, the TEM-Cell has to be integrated in the final model in order to be able to correlate the simulations with the measurements. In [10], a model of the TEM-Cell has been obtained by using an electromagnetic solver which has taken into account the interactions between the septum and the product leads (with the help of a FEM method). This model determines the equivalent self inductance of the metal parts (lead, septum …) as well as the different inductive and capacitive coupling between the TEM-Cell and the microcontroller (see Figure 9):

- A capacitor symbolizes the electrical coupling between the TEM-Cell and the product.
- Mutual inductances (between the package and the TEM inductances) symbolizes the magnetic coupling the TEM-Cell and the product.

Those two last parameters allow us to take in consideration the position of the microcontroller when it is placed in the TEM-Cell. Indeed, whatever the product position in the TEM, the electrical field received by the septum is the same. However, the magnetic field changes with the position of the DUT. On one hand, the mutual inductance is negligible if the leads are orthogonal to the direction of propagation. On the other hand, the mutual inductance is no longer negligible if the leads are collinear to the direction of propagation [10].

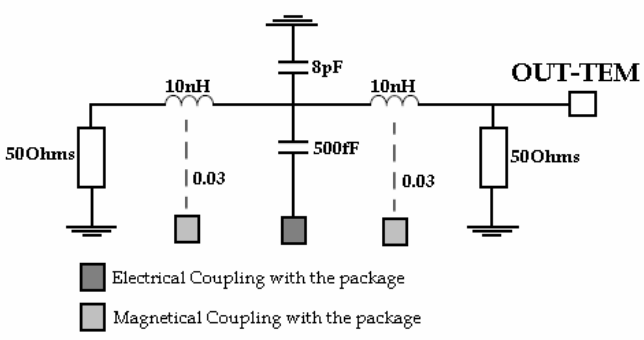


Figure 9. TEM-Cell RLC model

3.5 Final assembled model

Once the noise generator, the die and package PDN and the TEM-Cell have been modeled, the final model, valid up to 1GHz, can be assembled (see Figure 10). It symbolizes the behavior only when the chip is running in Wait. The main difference with this model compared with others models built before, is the noise generator accuracy. Indeed it takes into account the real current shape consumed by the product, even if it means that the simulation time will increase.

This model focuses mainly on the clock generation. Other activities (as the clock tree or digital core activity) are not taken in account in this "Wait Mode" model.

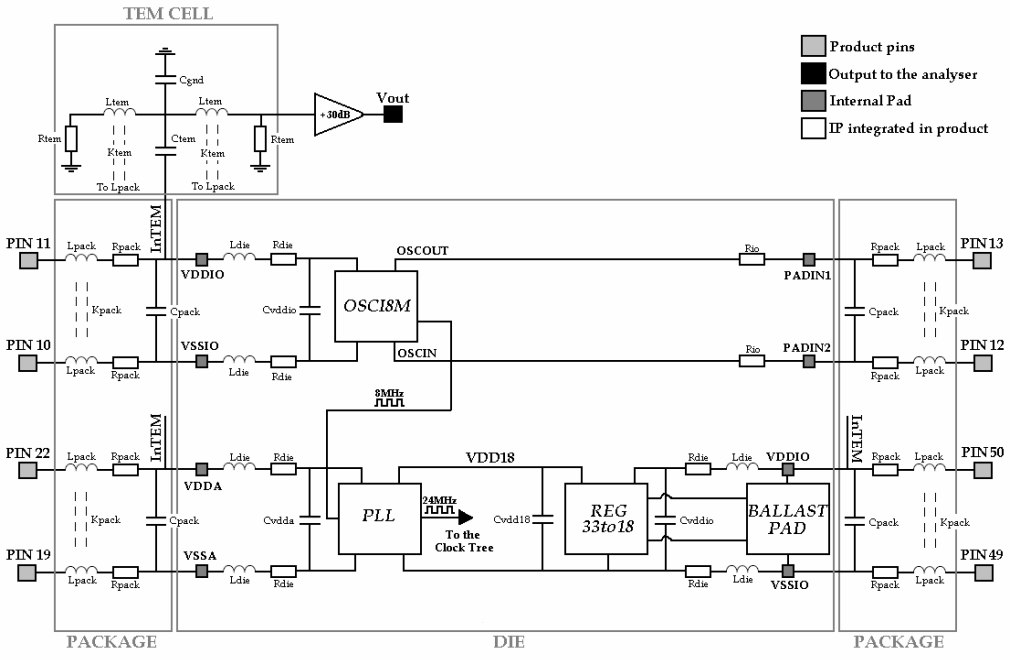


Figure 10. Final Wait Mode EMI model

4. RESULTS AND CORRELATION

The simulations have been done on a STXX with the help of the Eldo simulator. The model is running at 24MHz. An 8MHz clock is created by the oscillator (with the help of external 8MHz quartz) and then multiplied by three by the PLL. At each edge of the clock current glitches are created. Because of the package and die PDN, those switching currents create voltage bounces on the supply and ground as predicted by the formula (1). Finally the supply voltage variations are collected by the TEM-Cell, where the frequency spectrum is computed on its output. The figures 11 and 12 show the result of the FFT applied on the output of the 30dB amplifier. They also establish the comparison between simulations and measurements.

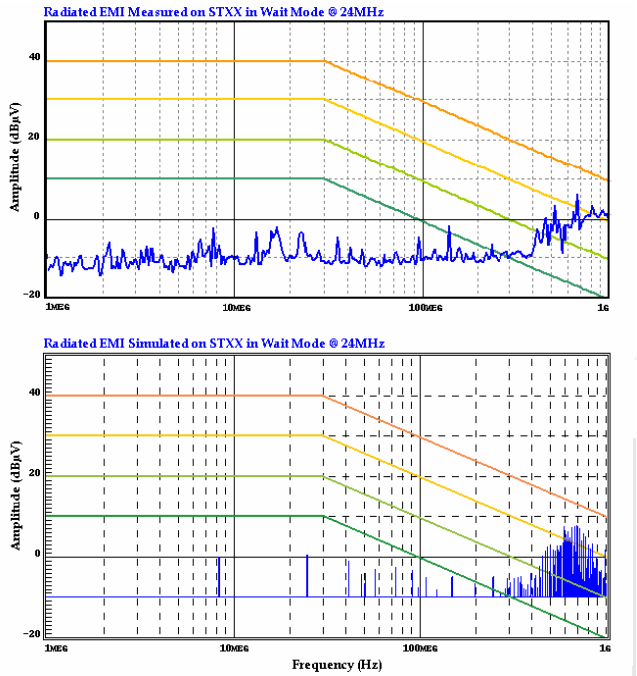


Figure 11. Comparison between Measurement (Up) and Simulation (Down)

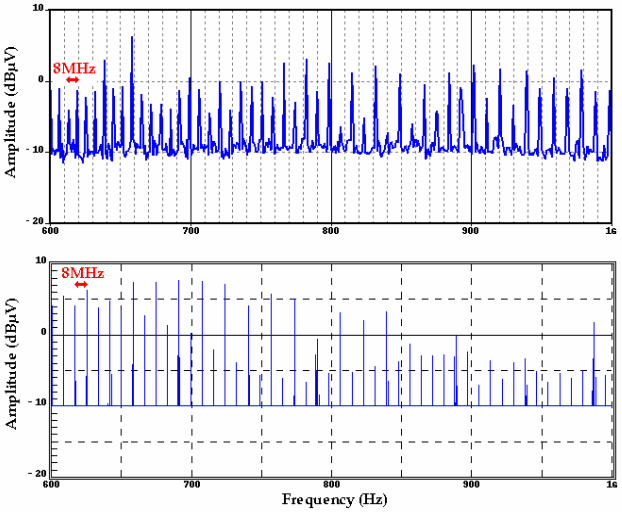


Figure 12. Zoom between 600MHz and 1GHz

The simulations seem to give a good representation of the phenomena observed in measurements. Indeed, the simulation fits well with the measurement regarding the amplitude and the frequency of the different components of the spectrum. First, the main harmonics (8MHz, 24MHz, 144MHz …) are all represented, except the 16MHz. Furthermore, their amplitudes match well with the measurements. Then, the decrease of the EMI between 144MHz and 400MHz is also visible. Finally, the resonance phenomenon in high-frequencies is also well represented. This resonance near 700MHz is due to the RLC filter constituted by the package inductance, the die resistance and the internal equivalent capacitance between the supplies.

5. CONCLUSION

This model gives a quite good EMI prediction prior to the product process. Indeed, an EMI level of 4, when the microcontroller is running in Wait mode (best case for the EMI), could be predicted during the design stage. Actually this model shows some inaccurate harmonics but the main goal is to be able to predict a global behaviour of the chip.

This model contains also others limitations. The most important is that this model only applies to the Wait mode. So it can be improved by adding an extracted clock tree but it is impossible to take in account the memory and digital core activities. Indeed, this limitation is caused by the simulator used, a transistor-level simulator, which requires too memory space and execution time when the netlists are huge.

This limitation can be avoided by using the Apache CAD tool suite like the RedHawk-CPM simulator. Those tools will allow including the digital core activity and the memories in the future models.

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