BER and Power Consumption Estimation Based on Hierarchical Modeling of a 2.4 GHz Power Amplifier

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IEEE Behavioral Modeling and Simulation Conference
September 23rd and 24th, 2010 - Session 2.2, 1:30 - 2:30 PM

Outline

- Introduction
- Power estimation framework
- Hierarchical modeling
- Conclusions

Introduction

- **Power consumption** remains as one of the major issues in micro and nanoelectronics industry

- **Integration** leads to the **increase in system complexity**
  - SoC can include several processing units, DSP, memories, sensors, RF transceivers, MEMS, etc
  - Providing energy for all these blocks becomes difficult

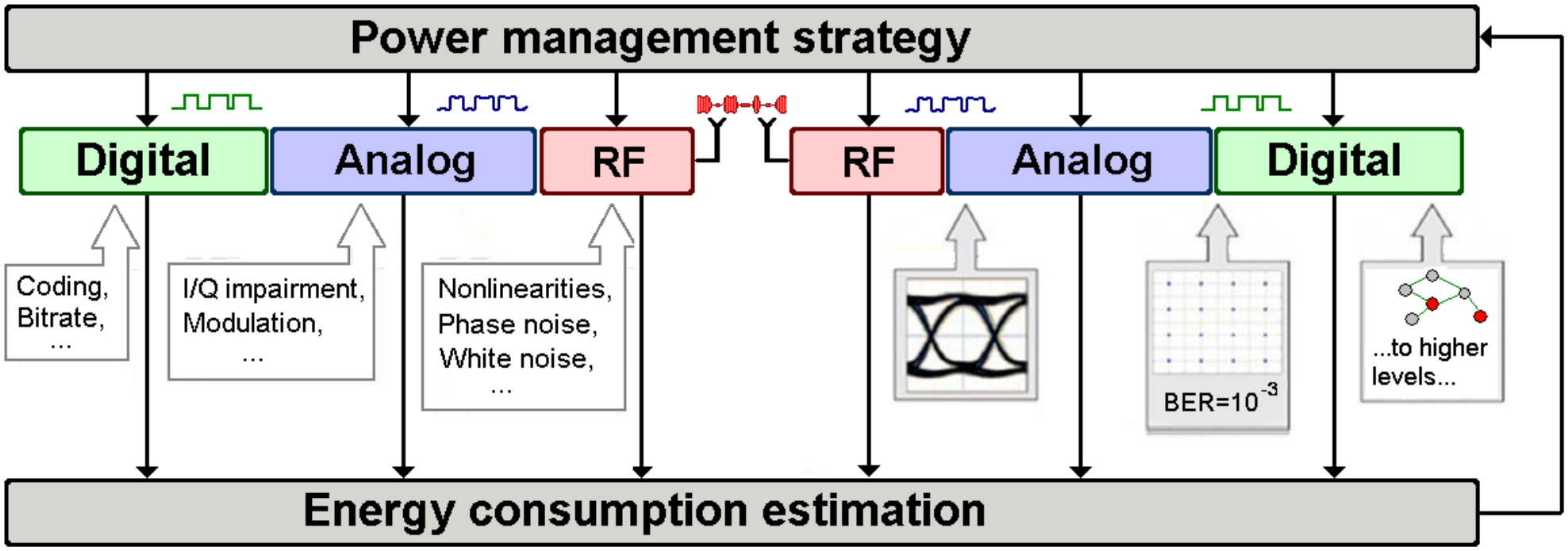
Introduction (2)

- **Mobile communication devices'** issues are critical
  - Wireless SoC are as complex as cited
  - But the power supply is limited by the battery lifetime

- **Demands for low-power and low-cost** products are harder to achieve
  - Downscaling energy x integration
    ⇨ Analog section and RF front-end
  - Time-to-market x system complexity
    ⇨ Improved design and high-level modeling effort

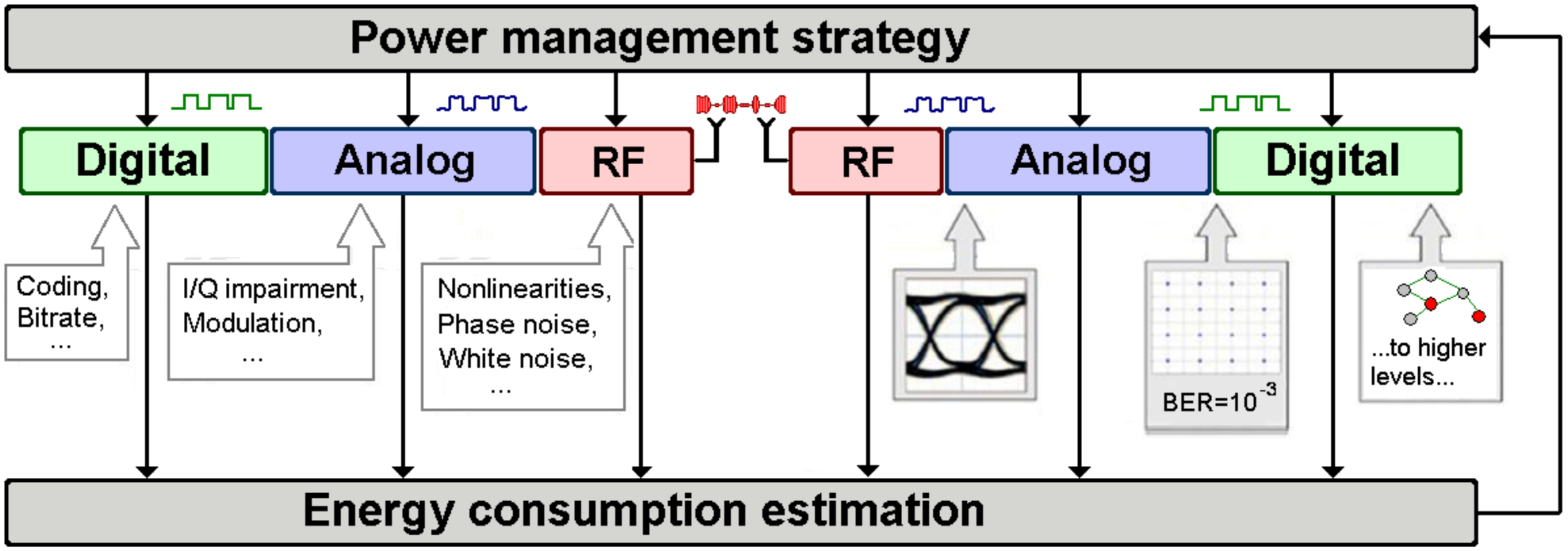
Introduction (4)

What strategy for power management?



Introduction (5)

What strategy for power management?

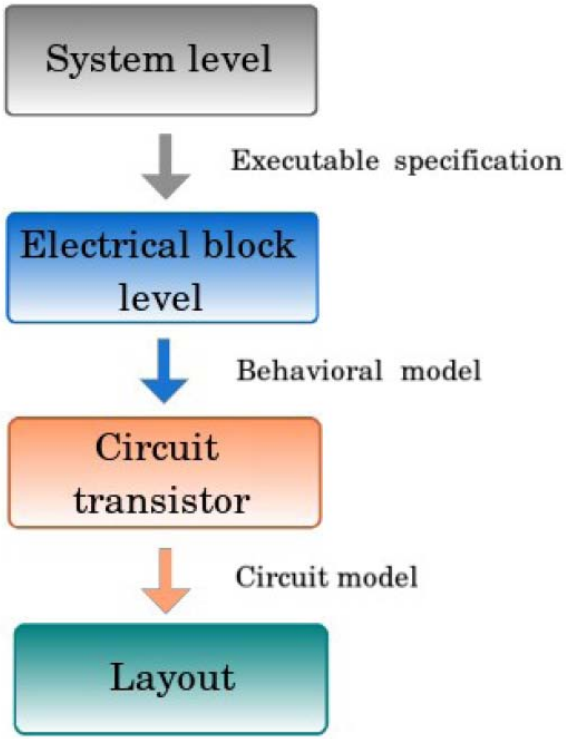


How much energy is consumed by the whole system?

Introduction (6)

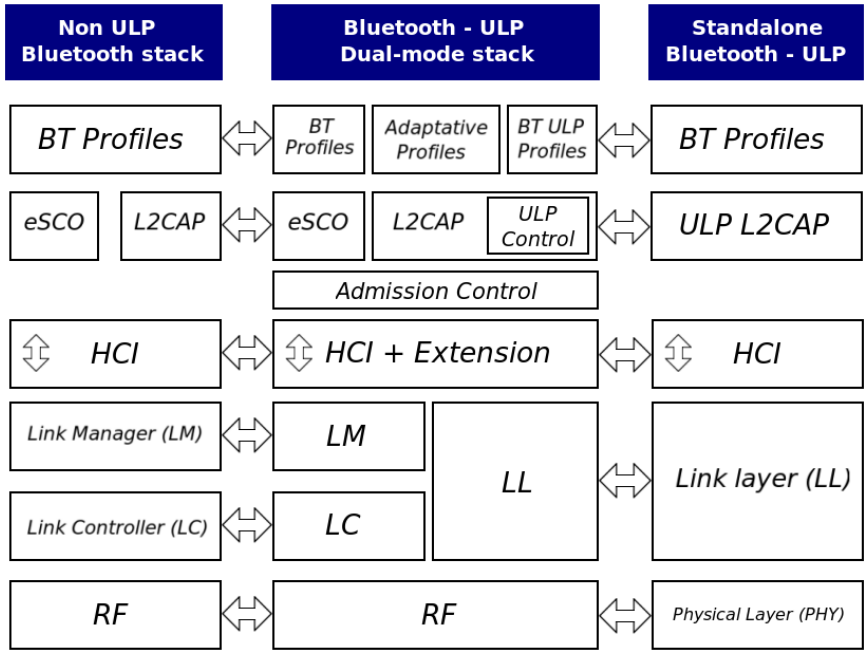
- **RF power amplifier**
  - Converts low-power into larger RF signal
  - Power gain must be efficiently achieved
  - Must present good linearity and input/output return loss

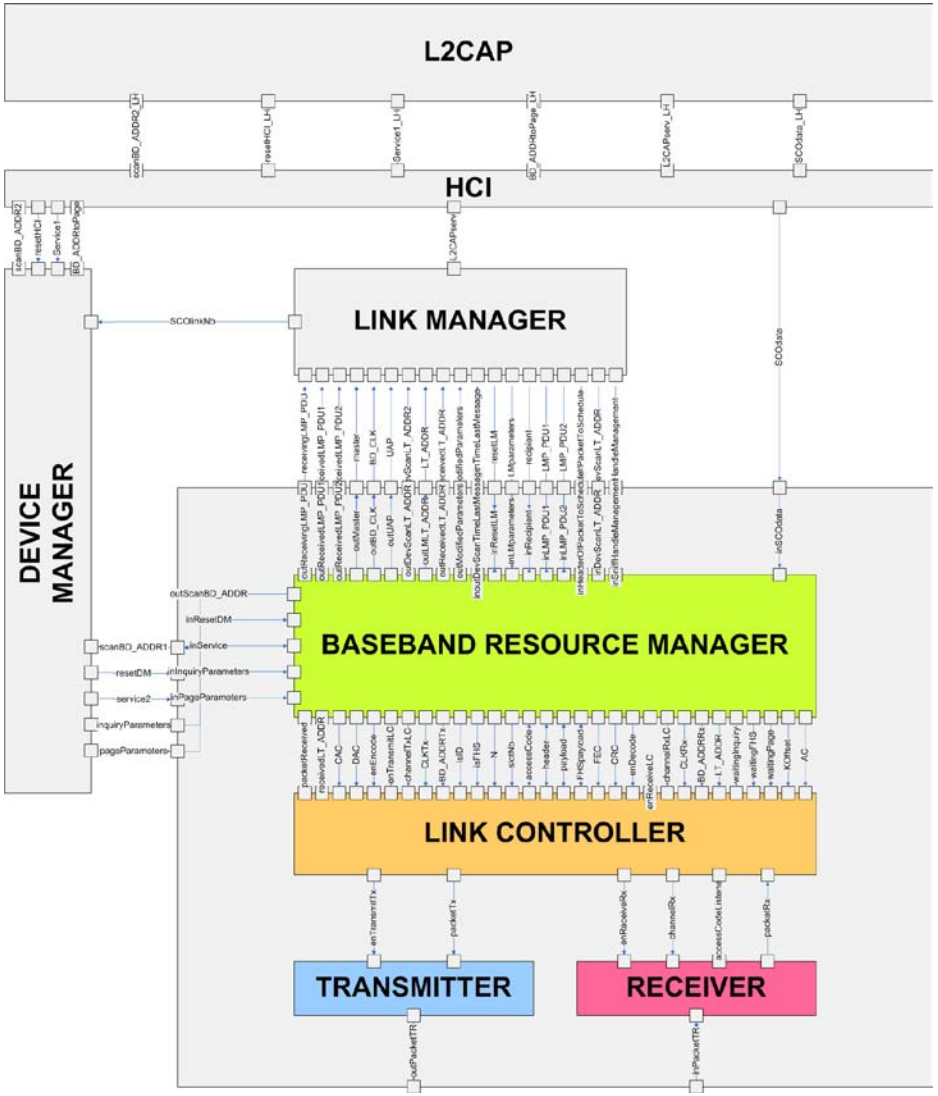
- One of most **power-consuming** block of the transmitter
  - Its deeper analysis may be interesting…
  - Hierarchical modeling
    - System-Level
    - Architectural-level
    - Circuit-level
    - Layout



Power estimation framework

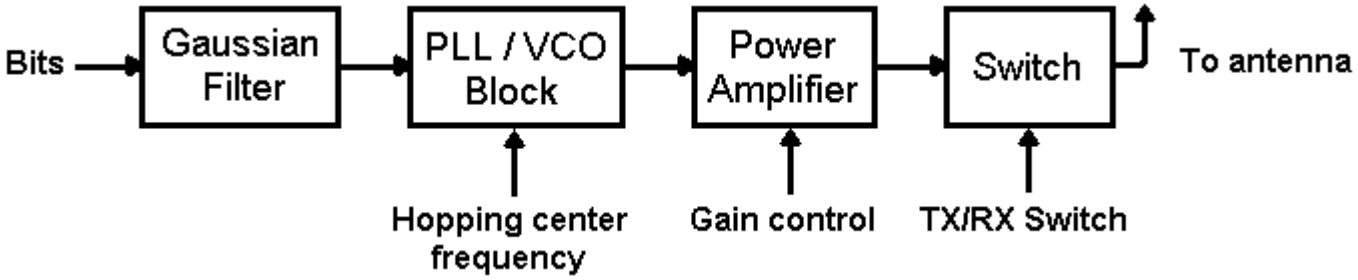
- **Bluetooth LE** system
  - Low power – Low cost applications
  - BT backwards compatibility
- **SystemC high-level model**
  - L2CAP to bit generation
  - Interface to network layer



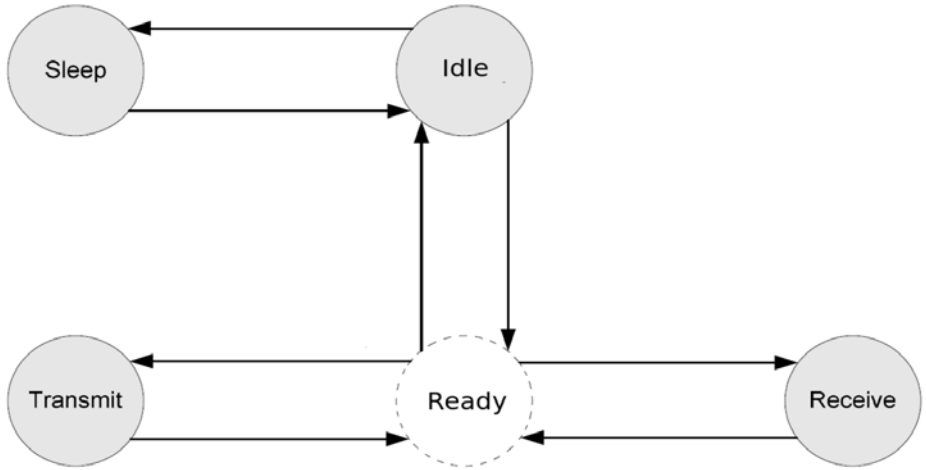


Power estimation framework (2)

- **RF transmitter**
  - Direct conversion
  - Blocks' characteristics extracted from standard specification
  - Refined Commlib RF models

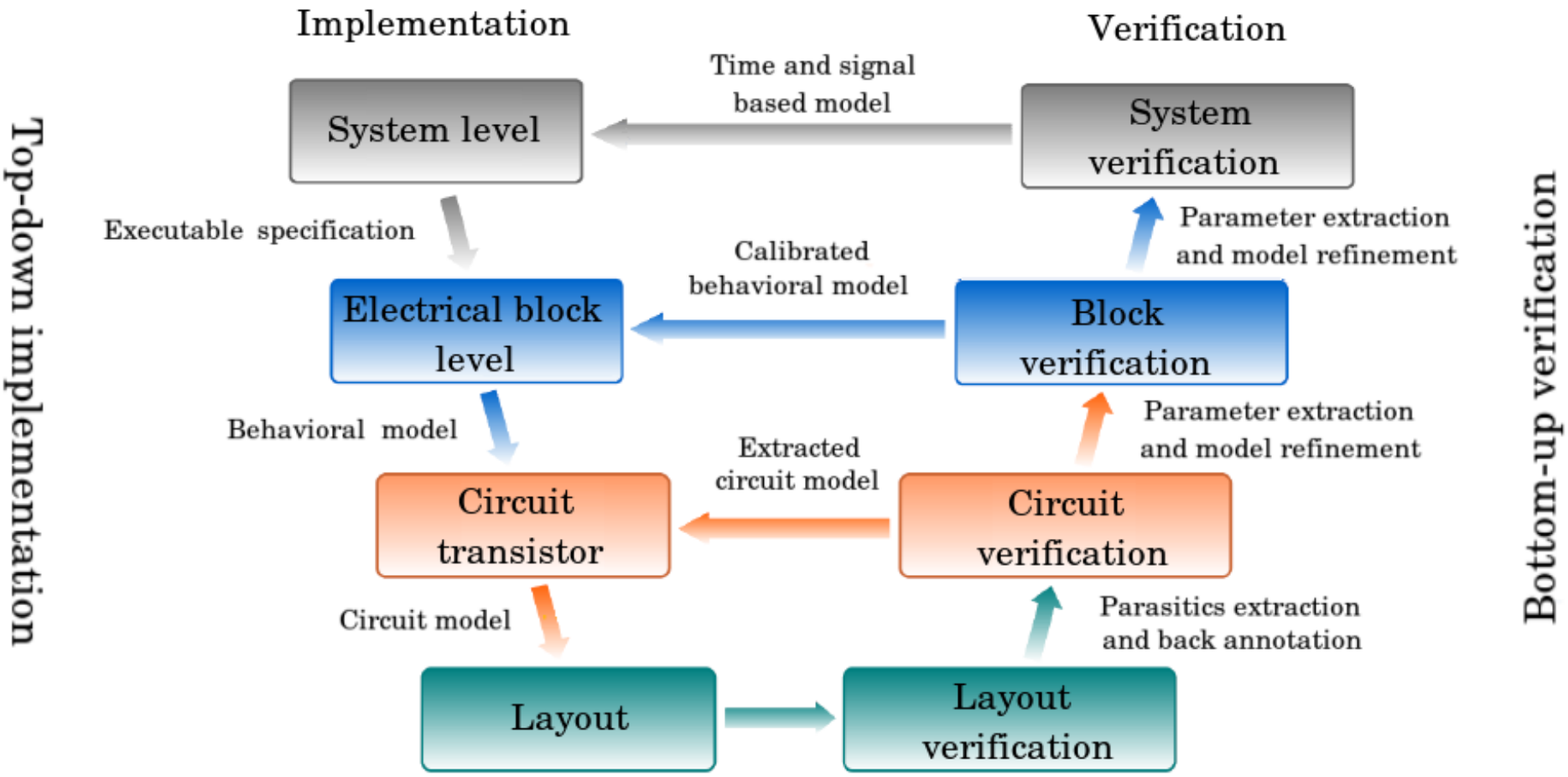


- **BT LE state-machine**
  - Blocks are not always active
  - On/Off switching can be implemented
    - Supply network must allow it
  - First idea on power consumption during time



Hierarchical modeling

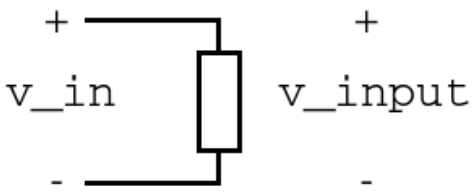
- Mixed signal **top-down design methodology**
  - System specification -> detailed design
  - Multi-level modeling and simulation compatibility
    - Mentor Graphics AdvanceMS environment



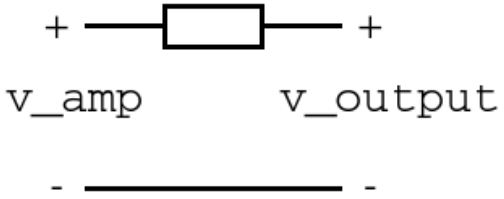
Hierarchical modeling (2)

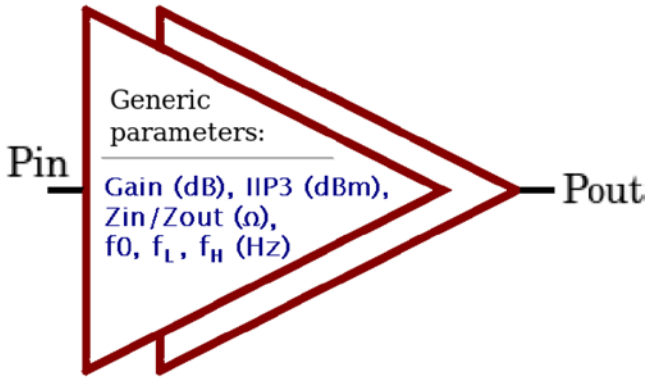
- Conservative **behavioral model** (VHDL-AMS)
  - Commlib_RF model (Mentor Graphics)

Input impedance

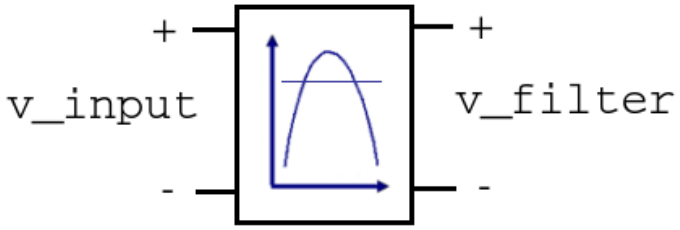


Output impedance



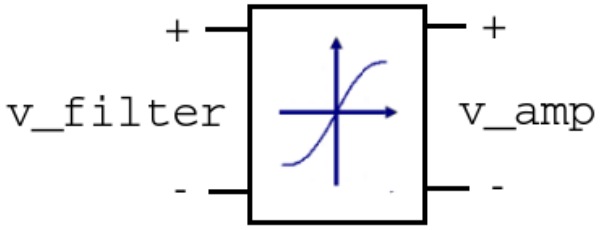


Frequency response



$$H_{frequency\,response} = \frac{1.0}{1 + j * (\frac{\omega}{\omega_1} - \frac{\omega_2}{\omega})}$$

Nonlinear response



$$G_{v_{3^{rd}\,order\,coeff}} = \frac{4}{3} * \frac{G_{v_{1^{st}\,order\,coeff}}}{IIP3^2_{voltage}} \qquad IIP3_{voltage} = \sqrt{\frac{2}{R_{input}} * 10^{\frac{IP3_{dbm} - 30}{10}}}$$

$$V_{input\,max} = \sqrt{\frac{G_{v_{1^{st}\,order\,coeff}}}{3 * G_{v_{3^{rd}\,order}}}} \qquad V_{output\,max} = \frac{2 * G_{v_{1^{st}\,order\,coeff}}}{3} * V_{input\,max}$$

Hierarchical modeling (3)

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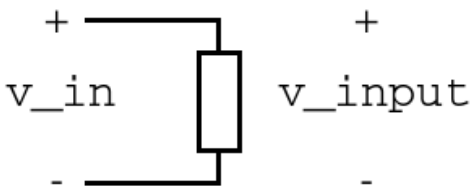
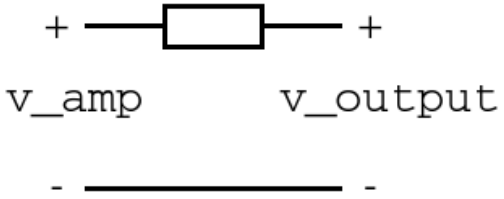
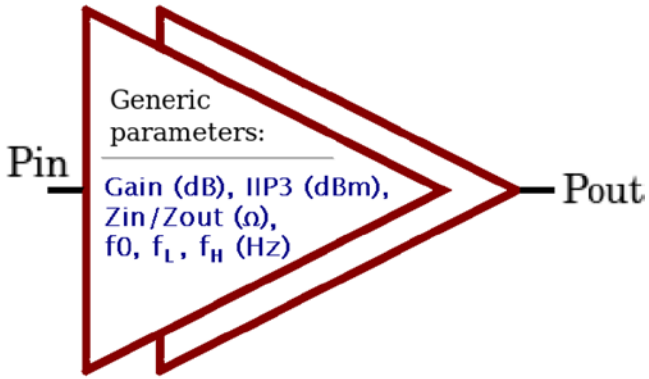


Output impedance





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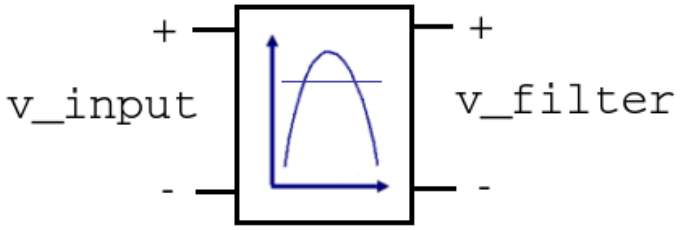

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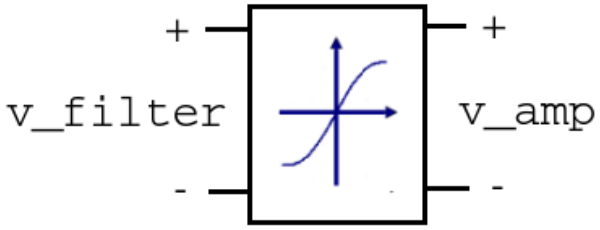

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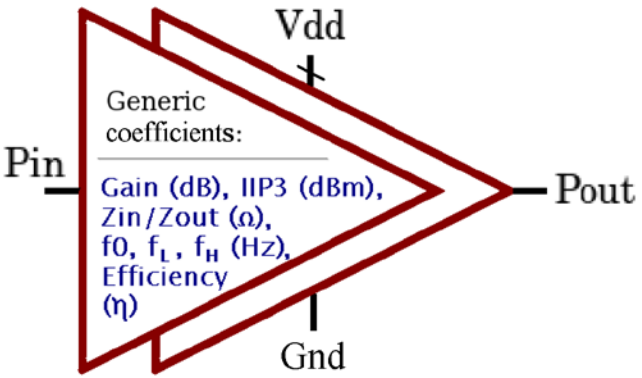
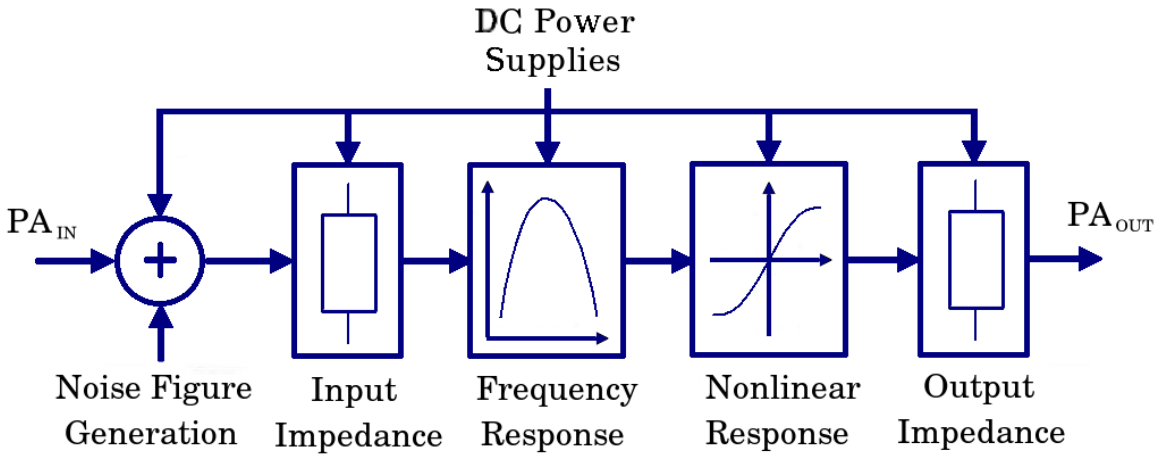
- **Power consumption support?**

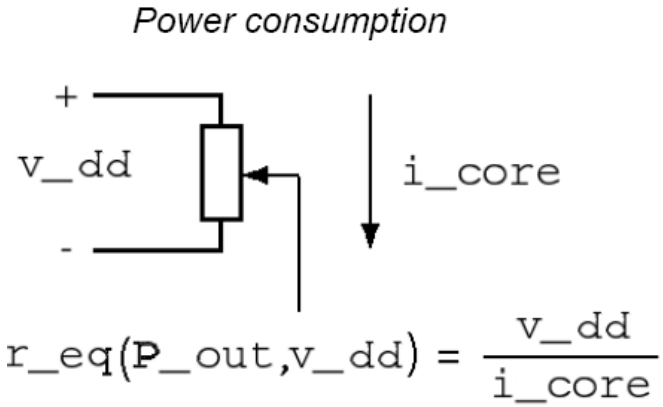
Hierarchical modeling (4)

- Conservative **behavioral model** (VHDL-AMS)
  - Power-aware model
  - Specifications as functions of inputs





- Power consumption modeled as a **variable impedance**

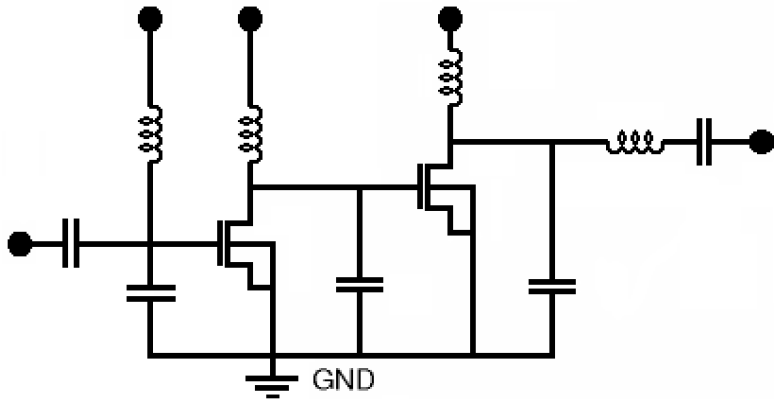


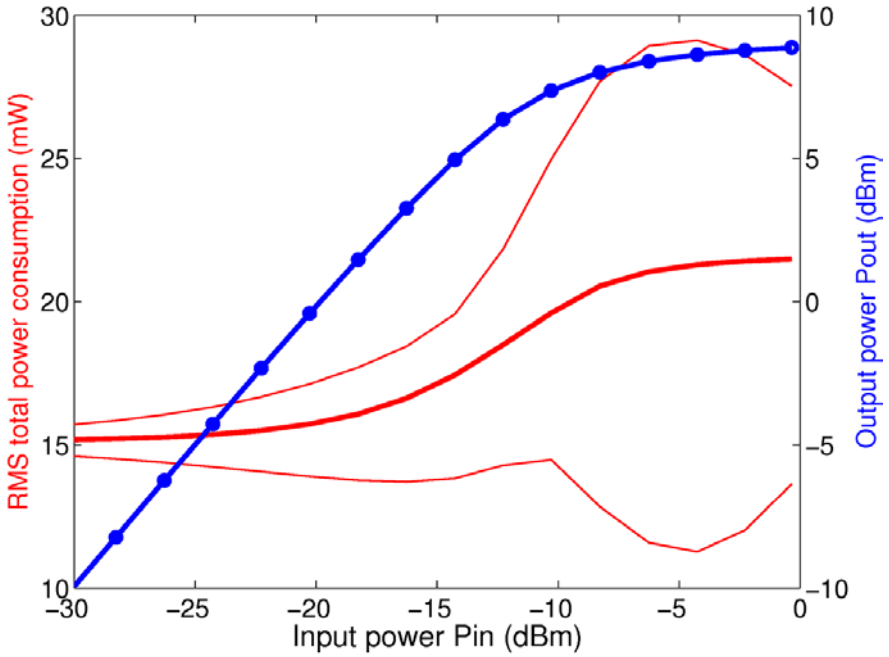
$$\eta_{\frac{W_{RMS}}{W_{RMS}}} = \frac{P_{out}}{P_{vdd}} = \frac{I_{load} * V_{load}}{V_{dd} * I_{core}} \rightarrow I_{core} = \frac{(v_{amp} - v_{output}) * v_{output}}{Z_{out} * V_{dd} * \eta}$$

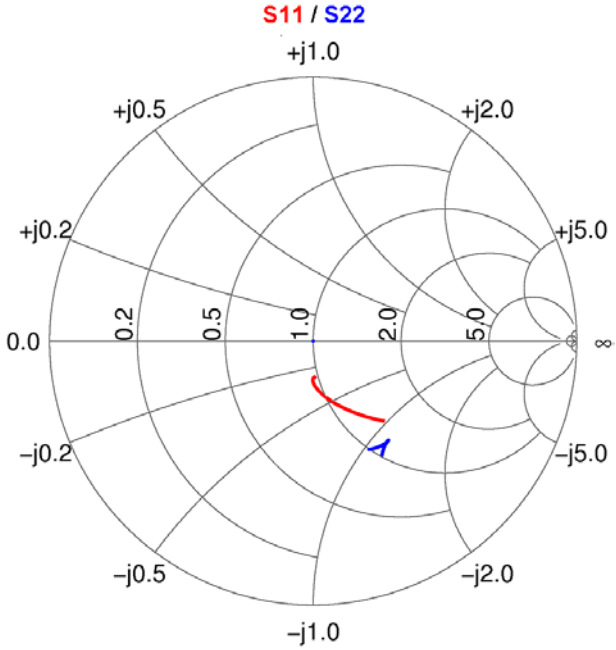
$$P_{out} = I_{load} * V_{load} = \frac{(v_{amp} - v_{output})}{Z_{out}} * v_{output}$$

Hierarchical modeling (5)

- **SPICE** circuit
  - Class-E topology
  - Exhaustive simulation for energy-consumption analysis
    - Wide input power range (ISM band)
    - DC supplies sweep



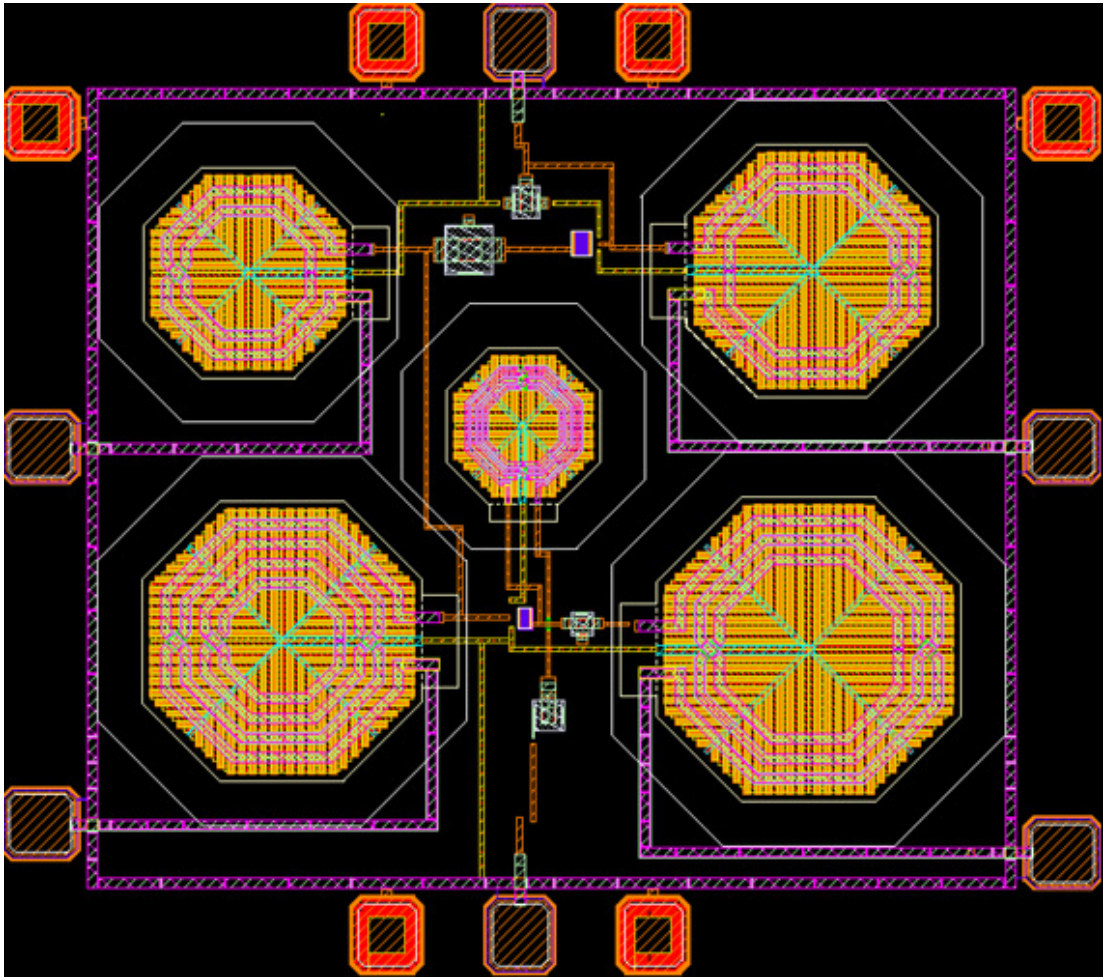




- In order to **fully characterize block's specifications**

Hierarchical modeling (6)

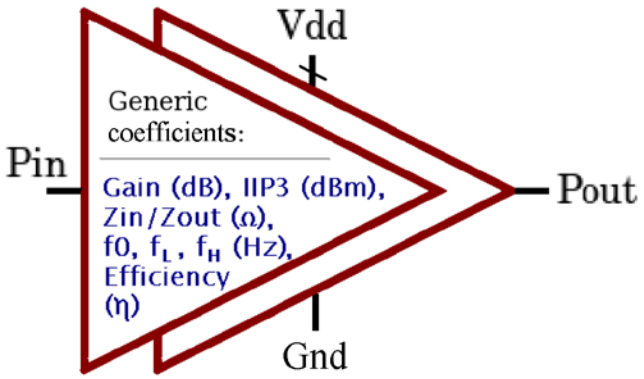
- **Physical layout** of the proposed circuit (Nov 2010)
  - Model could include post-layout and measured data

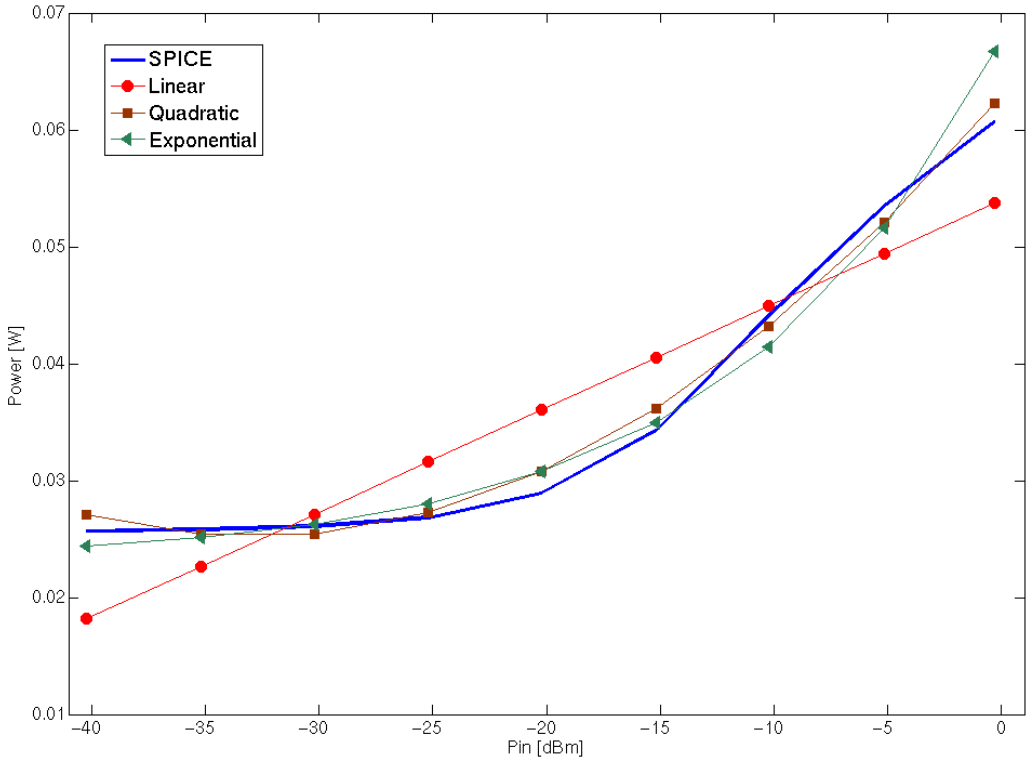


Hierarchical modeling (7)

- Refined conservative **behavioral model** (VHDL-AMS)
  - Power-aware model
  - Specifications as functions of inputs

- Different fitting functions can be tested
  - **Accuracy x Simulation time**

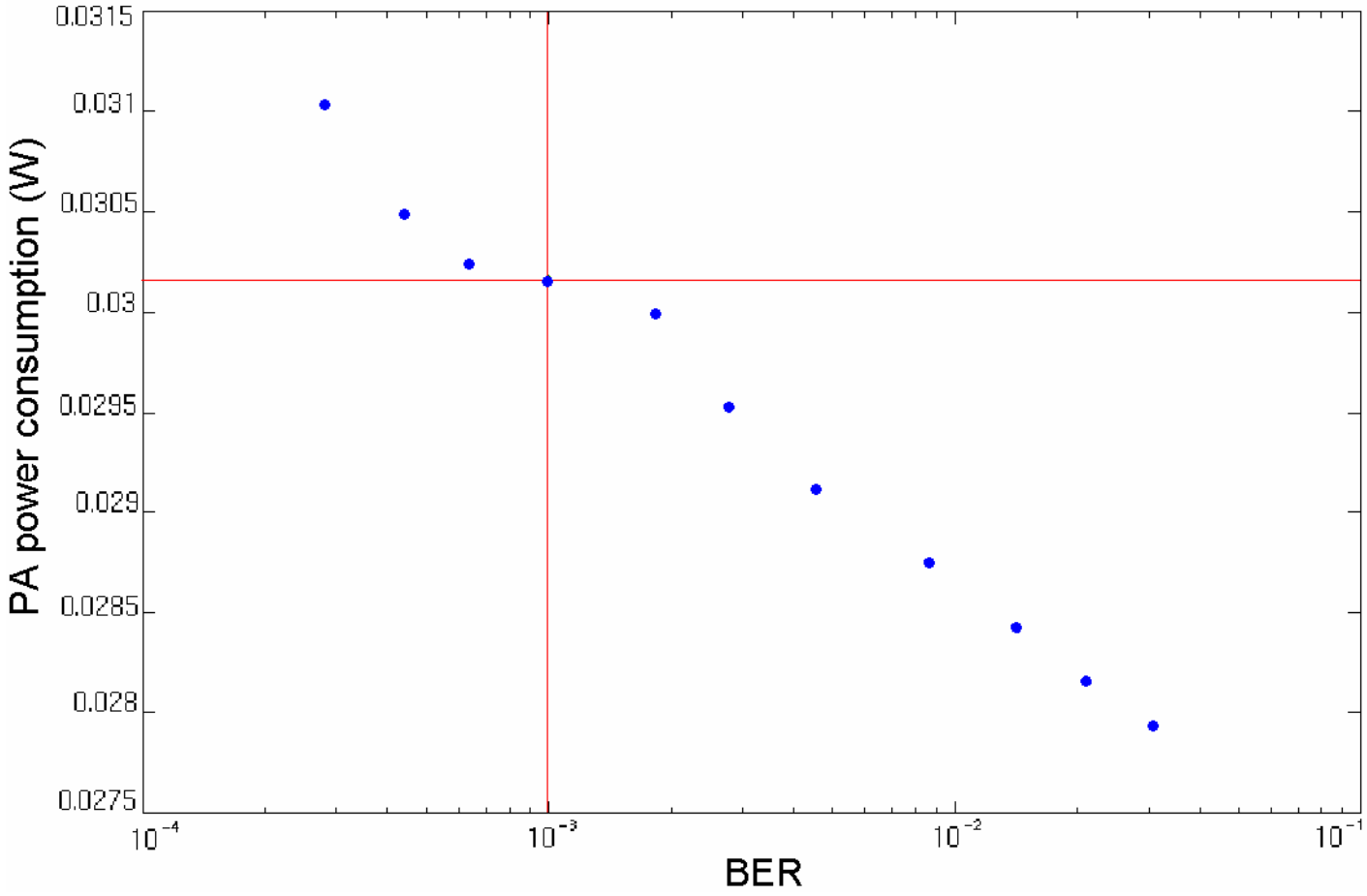




Conclusions

- **Hierarchical modeling** support within an **unified simulation environment** has been presented

- **System-level simulation** allowing power consumption estimation
  - Able to relate system's robustness to power consumption (e.g., BER)



Conclusions

- **Main drawbacks**
  - Need for SPICE electrical information
    - Electrical extraction -> model refinement
  - Lack of generic power consumption models
    - Deeply related to circuit topology
    - Genericity ⟷ Accuracy

Thanks for your attention!

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