Modeling Jitter in Continuous-Time Sigma-Delta Modulators

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ABSTRACT

In this paper, a fast and accurate technique for modeling and simulation of clock jitter in Continuous-Time sigma-delta ($\Sigma\Delta$) modulators is introduced. In addition to its high speed compared to the traditional jitter simulation method, the proposed technique is still continuous-time based which is more convenient than discrete-time based jitter modeling suggested in other publications. Mathematical principle of the proposed technique as well as simulations results are presented and compared to other simulation techniques.

1. INTRODUCTION

Continuous-time (CT) $\Sigma\Delta$ Analog-to-Digital Converters (ADCs) are receiving more and more attention due to their advantages compared to Discrete-Time (DT) $\Sigma\Delta$ ADCs. Inherent anti-aliasing filtering, lower thermal noise, higher sampling rate and lower power consumption are all attractive advantages of the CT $\Sigma\Delta$ ADCs that make them interesting solutions for high data-rate wireless communication systems [1].

The block diagram shown in Fig. 1 illustrates the structure of typical (CT) $\Sigma\Delta$ modulator. It composed of three major blocks: loop filter, comparator (quantizer) and feedback DAC (Digital to Analog Converter). The advantages of CT $\Sigma\Delta$ modulator over its DT counterpart is mainly due to two reasons. First, using a CT filter, which typically works at higher speed than DT filter, increases the modulator speed. Secondly, doing the sampling within the loop, instead of sampling the input before the loop as done in DT $\Sigma\Delta$ modulators, enhances modulator immunity to sampling errors and increases its SNR.

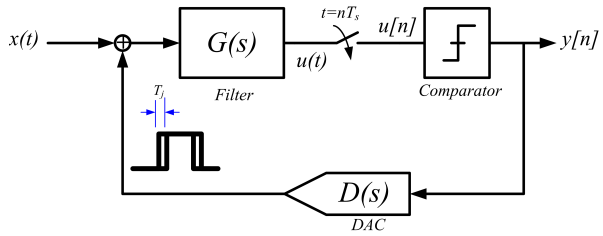

Figure 1: Continuous-Time $\Sigma\Delta$ modulator.

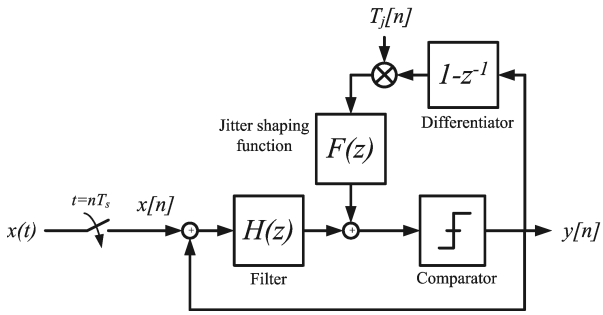

Figure 2: Jitter simulation model suggested in [3]

The main disadvantage of CT $\Sigma\Delta$ modulator is its sensitivity to the clock jitter of the feedback Digital-to-Analog Converter (DAC) which is not shaped with the loop filter due to its direct connection to the input node. This clock jitter noise appears as a white noise in the signal band and can limit the modulator performance [2].

Major difficulty in simulating clock jitter noise is the very long simulation time, as the simulation time step has to be sufficiently smaller than the clock jitter which is usually much smaller than the sampling clock period. To overcome this problem, discrete-time based methods were suggested in [3] and [4]. The basic idea of these technique is to replace the CT $\Sigma\Delta$ modulator with its DT equivalent, and convert all CT signals to approximate DT equivalent as shown in Fig. 2.

Although these discrete-time based techniques are very fast, their discrete-time nature limits their ability to model other circuit non-idealities such as loop filter non-linearity. In this work, we present a fast technique to simulate clock jitter without the need to convert the CT $\Sigma\Delta$ modulator to its DT equivalent [5]. The continuous-time nature of the proposed technique makes it very flexible and allow the designer to model other circuit non-idealities easily.

2. JITTER NOISE DEFINITION

Clock jitter is defined as the time-deviation of the clock transitions with respect to the ideal clock. To simplify clock jitter analysis, jitter effect can be modeled as an additive noise as shown in Fig. 3, where the added jitter noise is defined as the instantaneous difference between the jittered DAC pulse and the ideal DAC pulse [3]:

$$j(t) = h_j(t) - h(t) \tag{1}$$

where $h_j(t)$ is the jittered DAC pulse and $h(t)$ is the ideal DAC pulse.

Fig. 4(a-c) shows how the jitter noise can be deduced from the ideal DAC output and jittered DAC output. As the width of jitter noise pulses is usually very small compared to the clock period, they can be approximated as impulses as shown in Fig. 4(d).

3. PROPOSED TECHNIQUE

The proposed technique is based on the mathematical fact that the difference can be approximated as a differentiation as long as the time deviation due to clock jitter is much smaller than the clock period, which is usually the case. So, the jitter noise can be written in the following form:

$$j(t) \simeq T_j \frac{d}{dt} h(t) \tag{2}$$

where T_j is the root mean square (RMS) of the clock jitter. This indicates that the added jitter noise is extracted by differentiating the feedback DAC output and multiplying with a random number that has the same probability density function of clock jitter. The block diagram of proposed model and its waveforms are shown in Fig. 5 and Fig. 6, respectively.

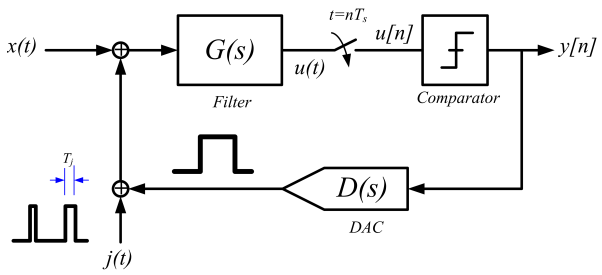

Figure 3: Modeling the jitter effect as an additive noise.

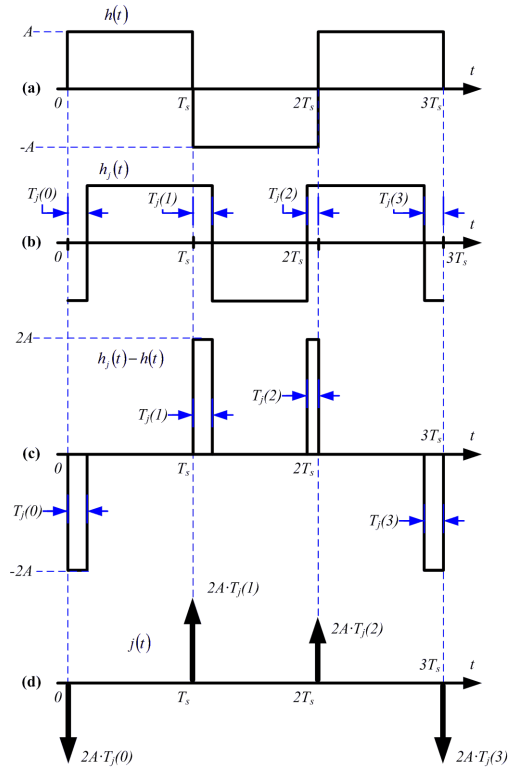

Figure 4: Deducing jitter noise waveform. (a) Ideal DAC pulse. (b) Jittered DAC pulse. (c) Jitter noise.

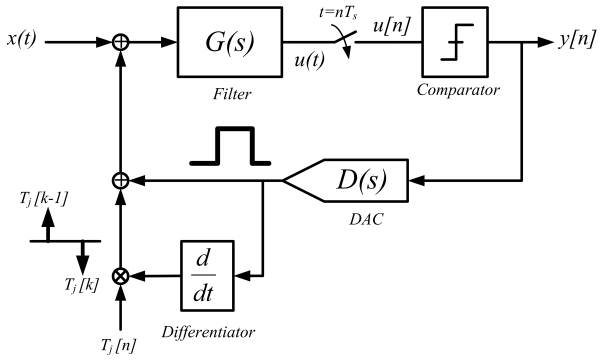

Figure 5: Proposed jitter simulation model.

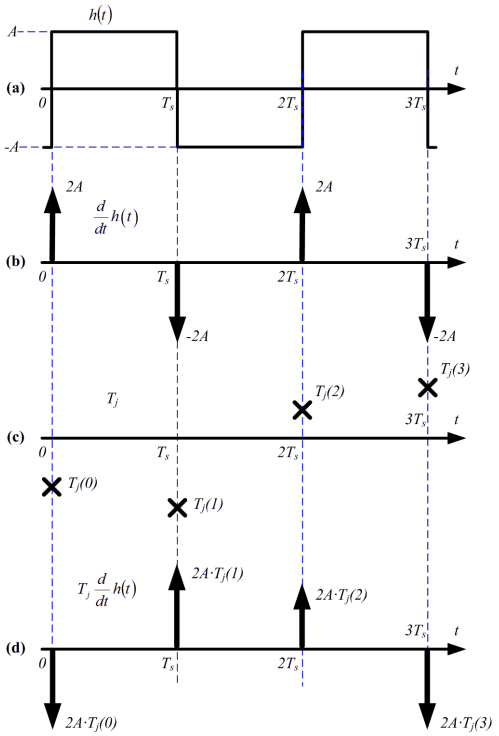

Figure 6: Waveforms of proposed model.

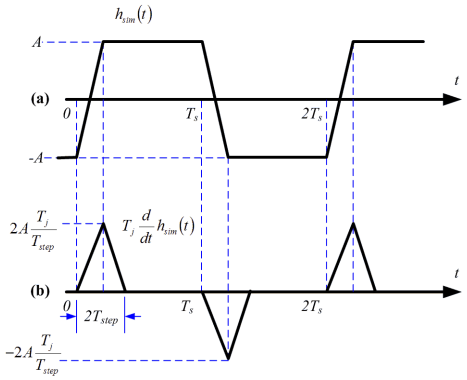

Figure 7: Simulated waveforms. (a) Simulated DAC waveform. (b) Simulated differentiation.

4. MODEL EFFICIENCY IN REAL SIMULATION

For ideal rectangular pulse, the proposed technique produces an impulse which is consistent with the traditional approximation [3]. However, for practical continuous-time simulations, the DAC waveform is trapezoidal rather than rectangular as shown in Fig. 7(a). For the trapezoidal pulse, the differentiation produces a triangular pulse instead of an impulse as shown in Fig. 7(b):

$$j(t) = T_j \frac{d}{dt} h_{sim}(t) = \frac{T_j}{T_{step}} tri\left(\frac{t}{T_{step}}\right) \tag{3}$$

where $h_sim(t)$ is the simulated DAC waveform and $tri(t)$ represents the triangular pulse and T_step is the simulation time step. In order to insure that the proposed technique produces acceptable performance in simulations, the spectrum of the jitter noise is found using Fourier transform:

$$J_{sim}(f) = T_j \, sinc^2(T_{step} \, f) \tag{4}$$

The output spectrum which is shown in Fig. 8 indicates that the jitter noise spectrum is almost flat in the Nyquist band. This result is valid as long as the simulation time step (T_{step}) is sufficiently smaller than the sampling time (T_s) which is usually the case for any continuous-time based simulation.

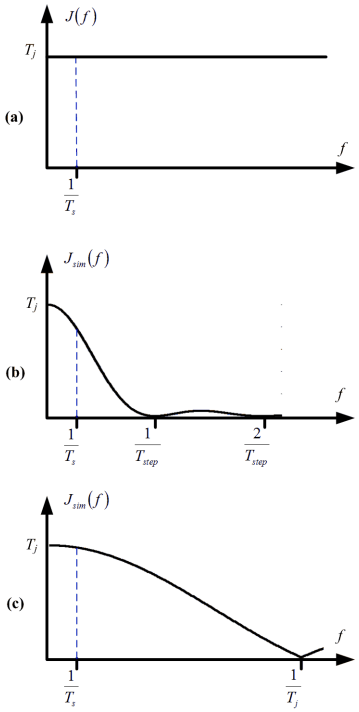

Figure 8: Spectrum of jitter noise. (a) Approximated as impulses [3] . (b) Proposed model. (c) Exact model.

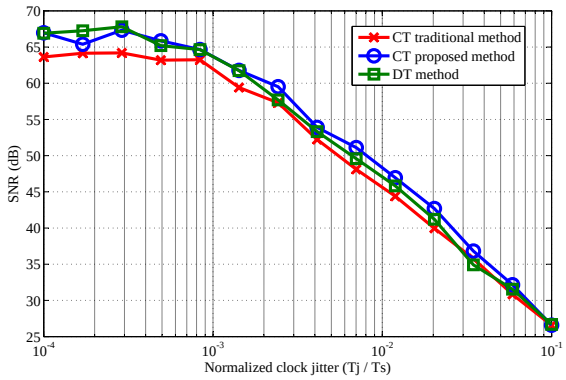

Figure 9: Simulation results

5. SIMULATION RESULTS

To validate the proposed technique, the model proposed in Fig. 5 was used to simulate the jitter in a 4^{th} order bandpass continuous-time $\Sigma\Delta$ modulator with a non-return-to-zero (NRZ) DAC. The clock jitter RMS value was swept from 0.01% to 10% of the sampling period. The same simulations were performed using the traditional continuous-time method used in [6] and also using the discrete-time method suggested in [3]. The simulation results illustrated in Fig. 9 showed good agreement between the three methods.

6. CONCLUSION

A technique for modeling clock jitter effect in continuous-time $\Sigma\Delta$ modulators was introduced. The proposed model combines both fast simulation time and continuous-time nature. Table 1 summarizes the main advantages and disadvantages of proposed model compared to other used techniques. Mathematical analysis shows that proposed technique is reliable even with relaxed simulation time step requirements. Simulation results showed good agreement between the proposed technique and traditional methods.

Table 1: Comparison between different methods of jitter simulation in CT $\Sigma\Delta$ modulators.

	Traditional method [6]	DT method [3]	Proposed method [5]
Simulation nature	CT	DT	CT
Simulation time	Slow (Hours)	Very fast (Seconds)	Fast (Minutes)
Adding non-idealities	Easy	Difficult	Easy
SPICE compatibility	Compatible	Not compatible	Compatible

7. REFERENCES

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