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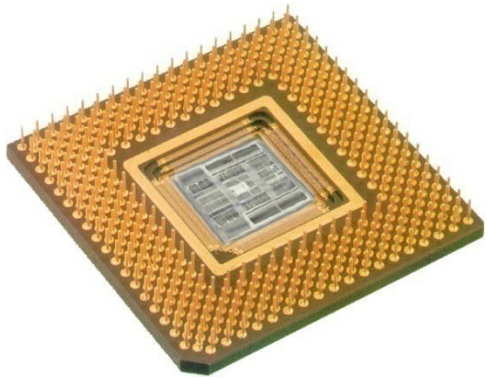
LIP6



SoC

Modeling Jitter in Continuous-Time ΣΔ Modulators

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Outline

- Introduction
- Existing Solutions.
- Proposed Technique.
- Real Simulator.
- Validation.
- Conclusions.

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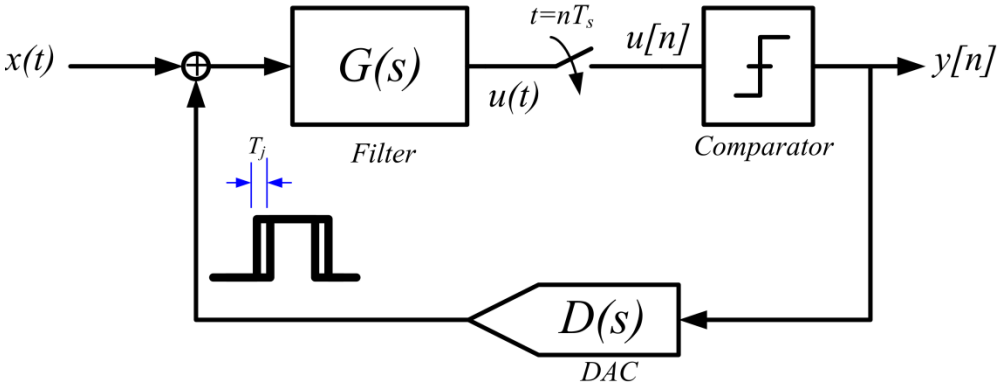
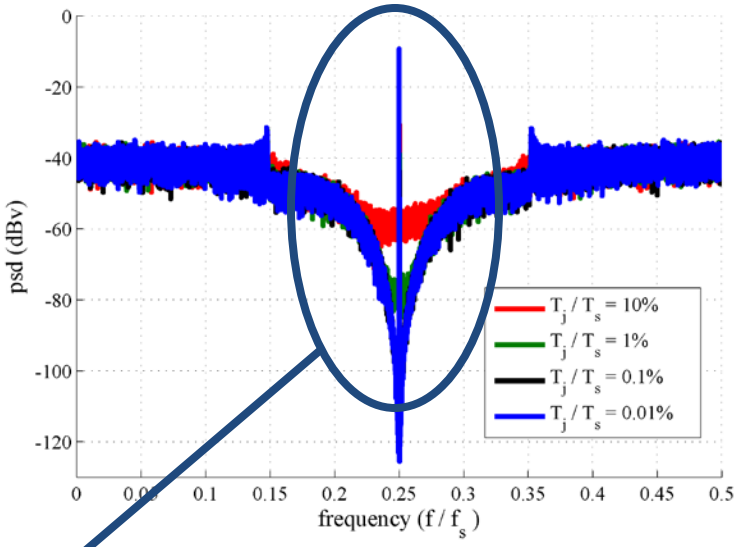
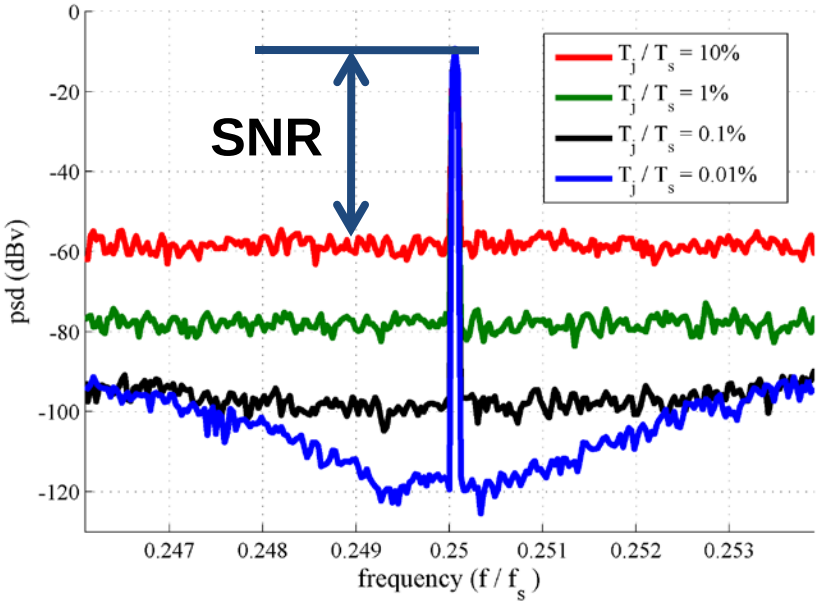
Clock Jitter Effect on ΣΔ Modualtor







Jitter Simulation

$T_j / T_s \sim 0.001$

T_j → Jitter deviations.
T_s → Sampling Time.
T_{step} → Simulation step.

- For an accurate simulation:

$T_{step} << T_j$

$T_{step} \sim 0.0001\ T_s$

- This means that 10,000 simulation points are needed in a single clock cylcle.
- Very slow and expensive simulation!

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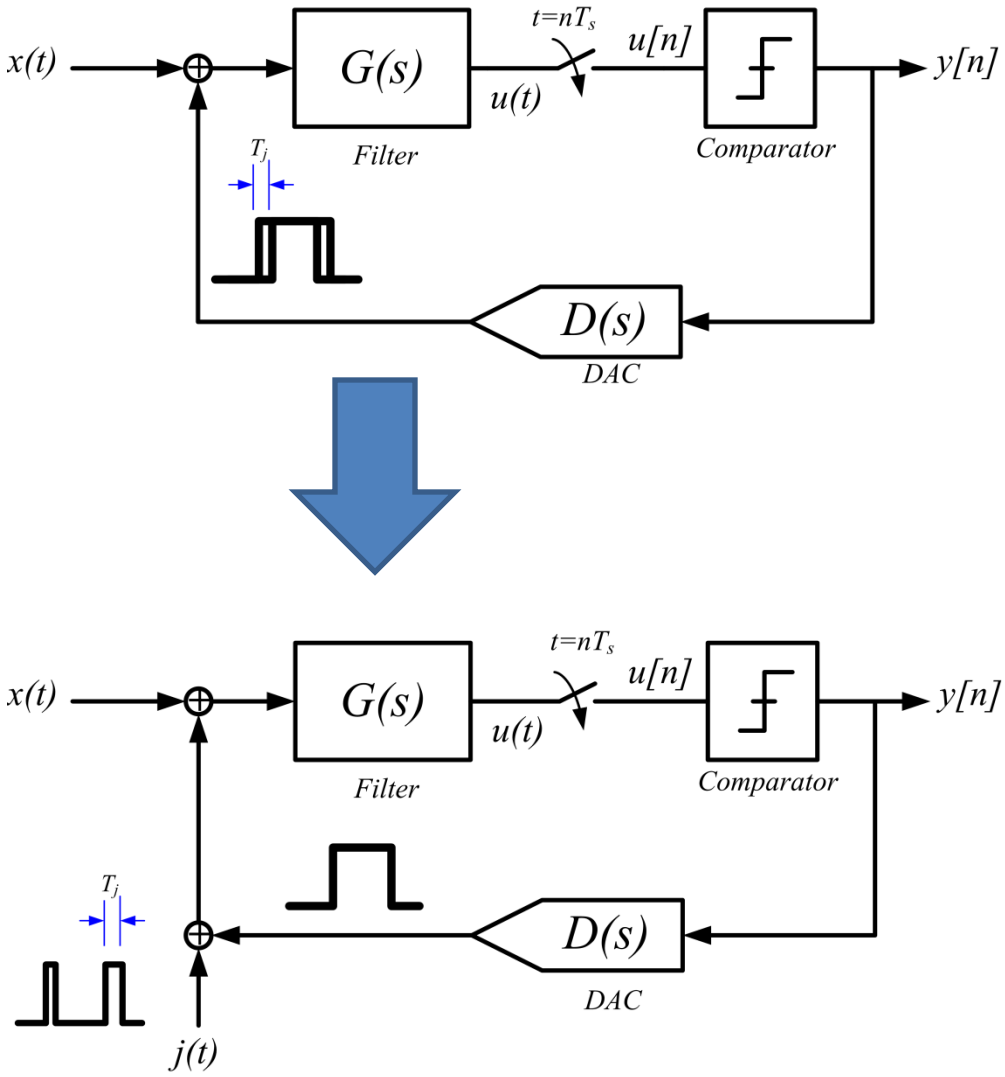
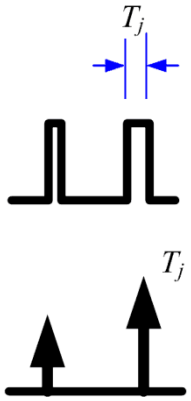
Modeling Jitter as Additive Noise

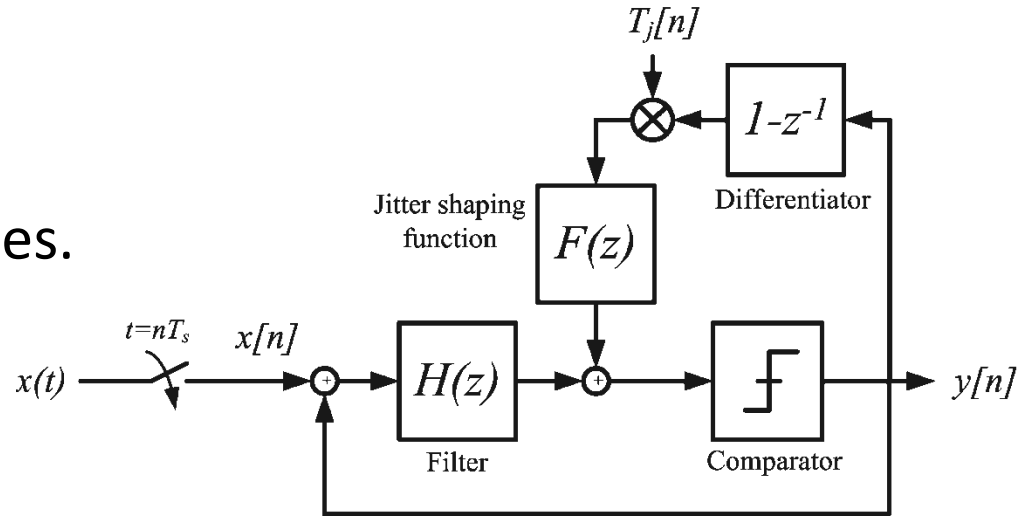
- Traditionally used to simplify jitter analysis.
- Replace "Jittered" DAC with an ideal DAC + jitter noise.



Discrete-Time Simulation

- Suggested by [Benabes-01]
- Find discrete-time equivalent.
- Approximate jitter pulses to ideal impulses.
- Very fast ($T_{step} = T_s$).
- Not flexible:
  - Tedious analytical effort.
  - Difficult to add non-idealities.
  - Not SPICE compatible.





[Benabes-01] P. Benabes and R. Kielbasa, "Fast clock-jitter simulation in continuous-time delta-sigma modulators," in Proc. IEEE 18th Instrumentation and Measurement Technology Conference, (IMTC'01), vol. 3, May 2001,.

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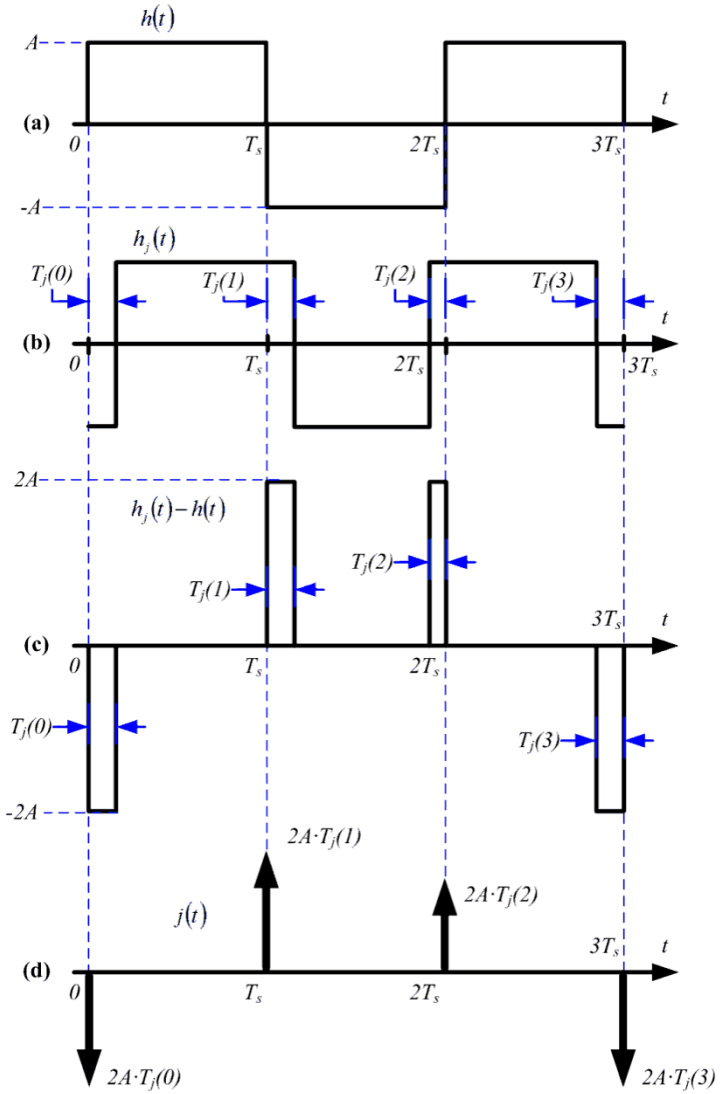
Proposed Technique

- Jitter noise is defined as a difference:

$$j(t) = h_j(t) - h(t)$$

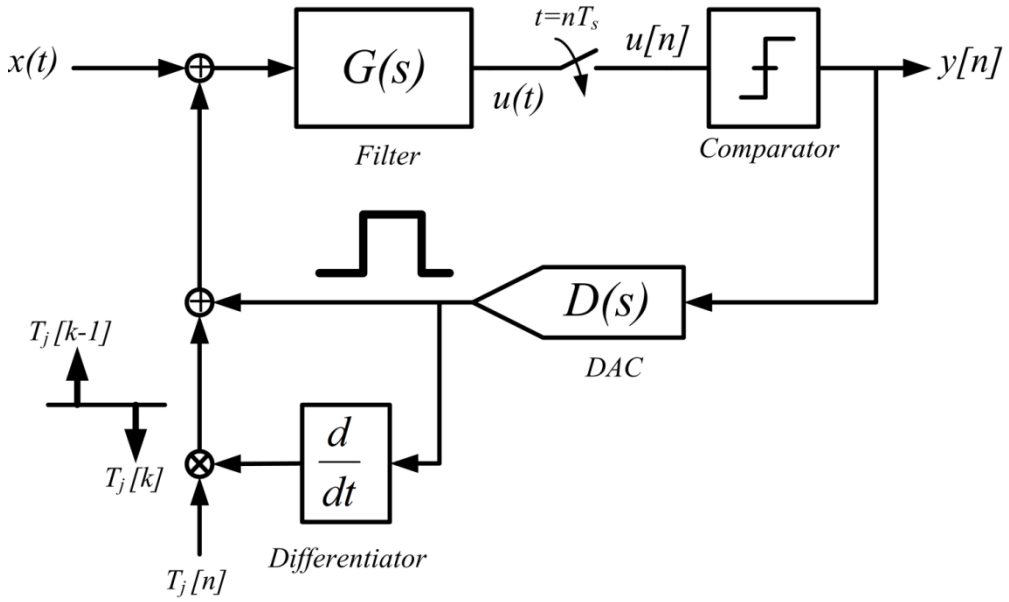
- For small time shift, difference can be approximated to a differentiation:

$$j(t) = h_j(t) - h(t) \approx T_j \frac{d}{dt} h(t)$$

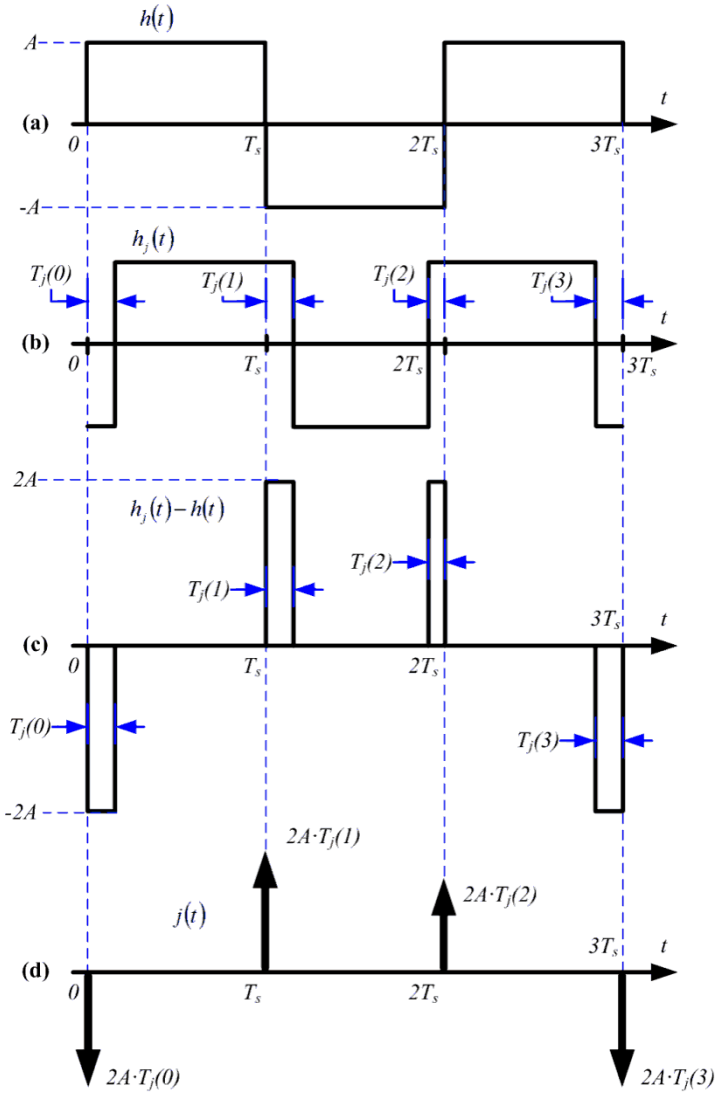


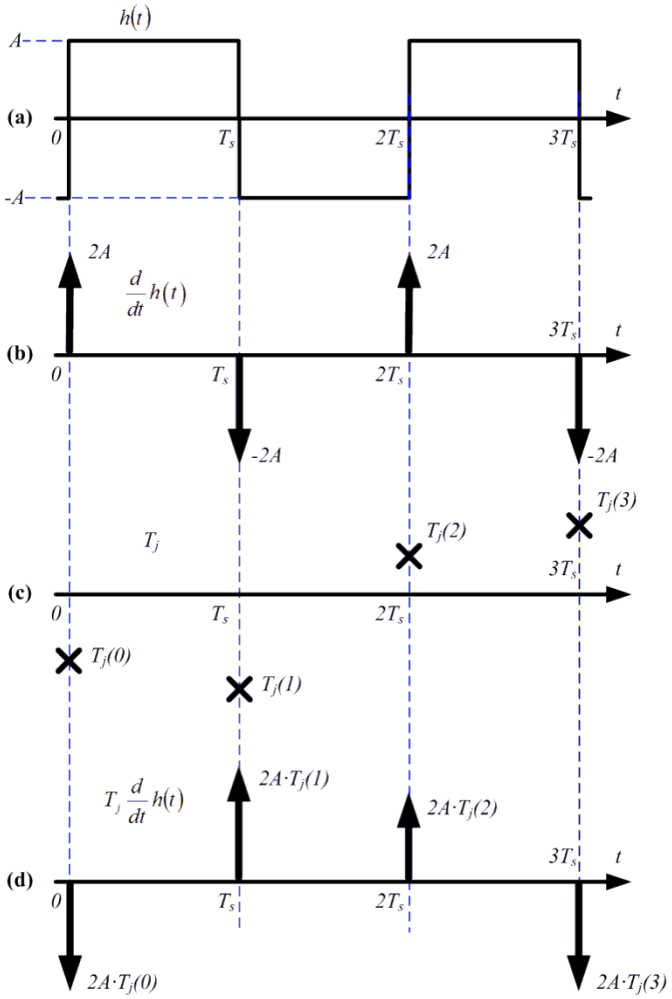
Proposed Block Diagram

- Differentiator is added to the DAC output.
- Random variable generator (new value each cycle)



Output Waveforms





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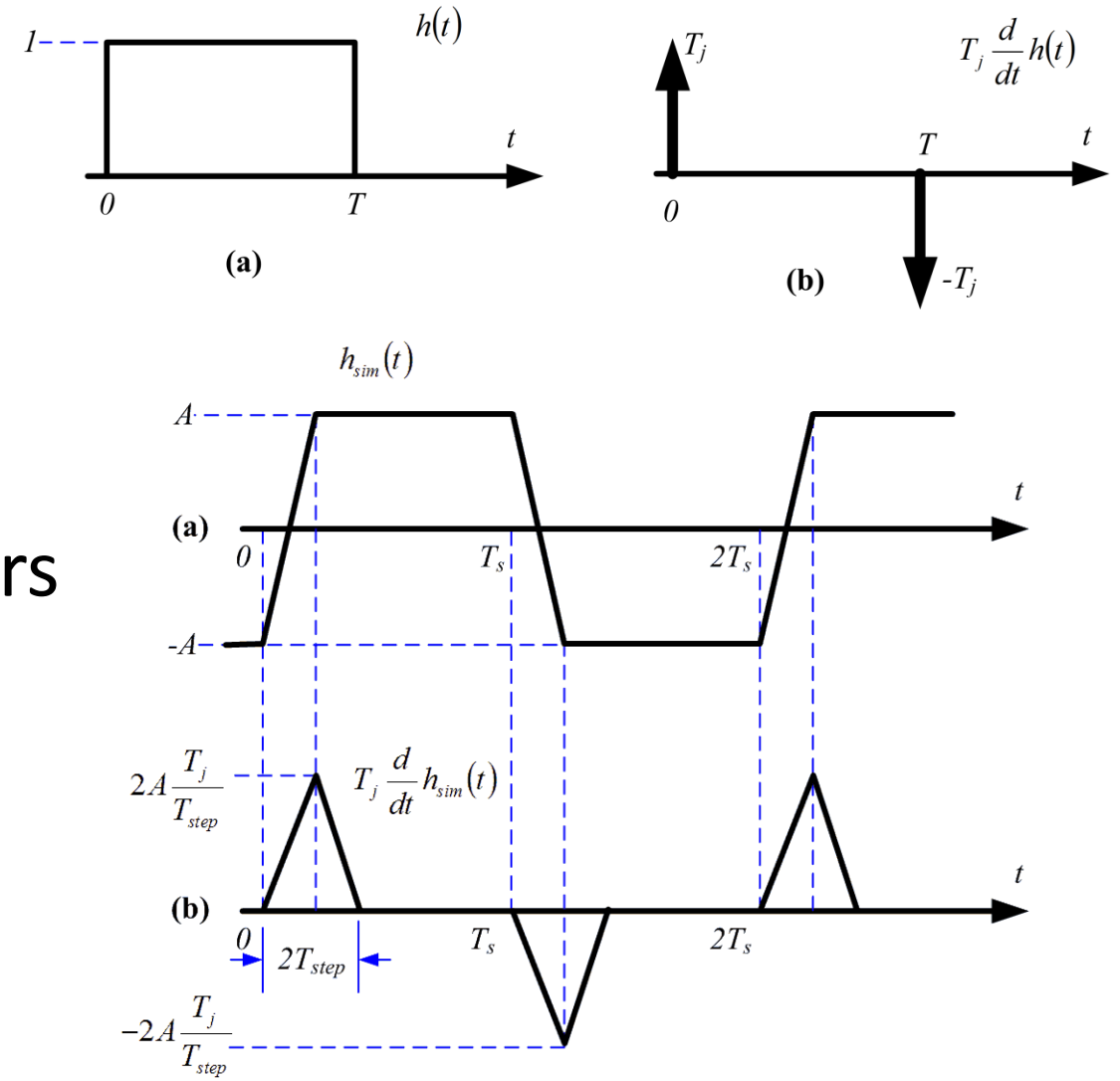
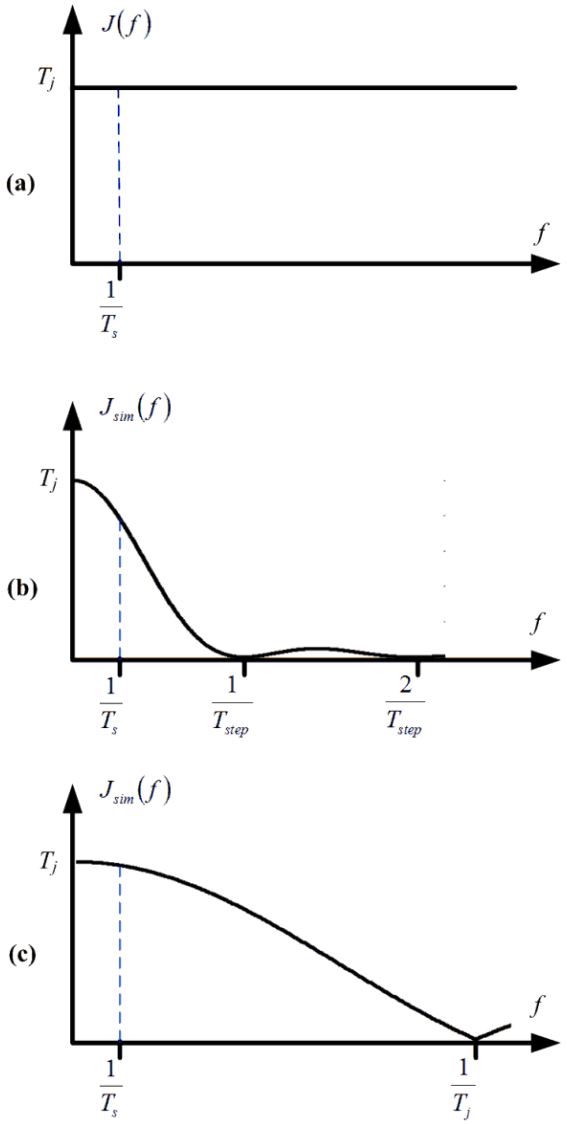
Real Simulator

- Ideally, the DAC output is a square wave.
- But, due to finite time-step, it appears as a trapezoidal.
- Is this a problem?



Real Simulator

- Figure on the right shows spectrum of:
  - Ideal impulse.
  - Triangle pulse of width $2T_{step}$
  - Pulse of T_j width.
- In all cases the spectrum is almost flat in the Nyquist band.
- Should give the same results



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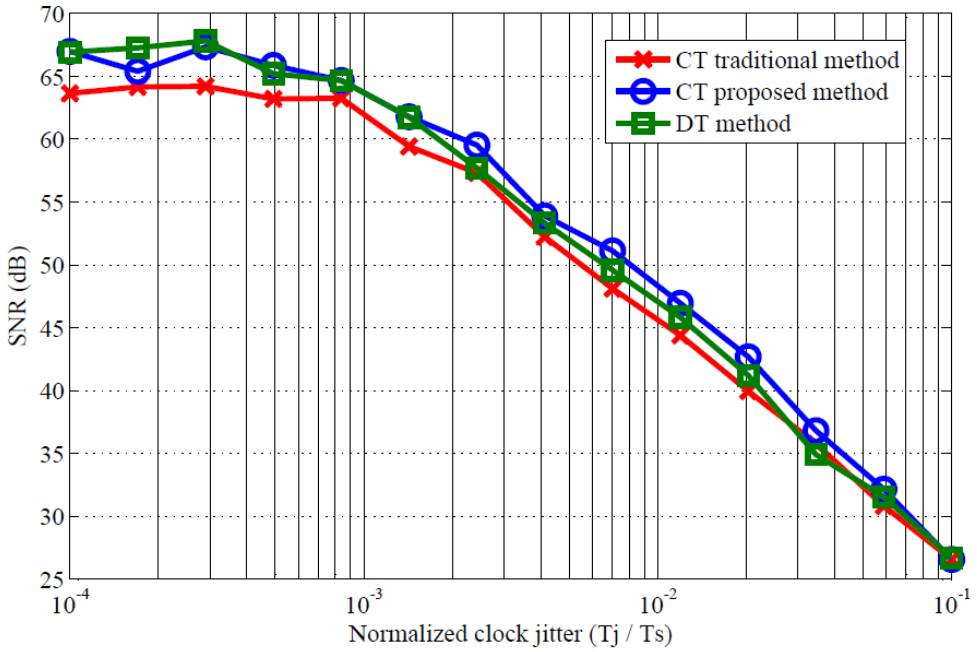
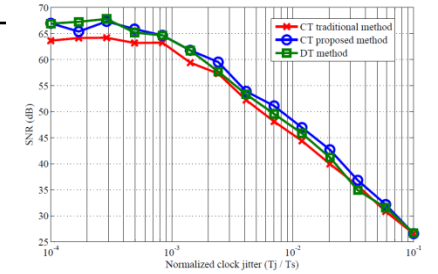
Simulation Results

- Figure shows jitter effect on SNR using 3 methods:
  - Traditional method (Very slow).
  - Discrete-Time method [Benabes-01].
  - Proposed method.
- Good agreement.



Comparison

	Traditional method	Discrete-Time [Benabes-01]	Proposed method
Simulation Nature	Continuous-Time	Discrete-Time	Continuous-Time
Simulation time needed to produce the above figure	Very Slow (10 hours)	Very fast (10 seconds)	Fast (10 minutes)
Possibility to model circuit non-idealities	Easily modeled	Very limited	Easily modeled
Spice compatibility	Compatible	Not Compatible	Compatible

Conclusions

- Clock jitter is a performance limitation of CT ΣΔ modulators.
- Jitter simulation is very slow.
- A fast and continuous-time based simulation technique is proposed.
- The proposed technique is valid even for finite-step simulators.
- Simulation results shows good agreement between proposed method and traditional methods.
- The proposed technique is a compromise between simulation speed and model flexibility.

Thank you

Questions?