Design and Modeling of a Successive Approximation ADC for the Electrostatic Harvester of Vibration Energy

R. Khalil, A. Dudka, D. Galayo, R. Iskander and P. Basset

Presented by:
F. Pecheux

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Outline

- Introduction
  - Harvester operation
  - Smart power management
  - Work goals
- Successive Approximation ADC
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  - SAR ADC Modes
  - Comparator
  - DAC and SAR Control

Outline

- SAR ADC into The Harvester Conditioning Circuit
  - Calibration technique
  - Model Results
- Conclusion

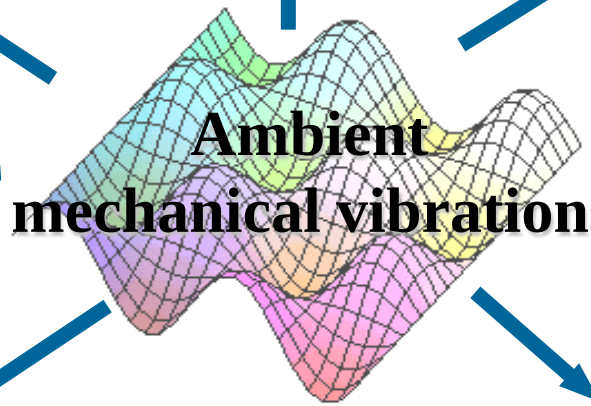
Introduction

Cars

Trains

Aircrafts

Industrial tools

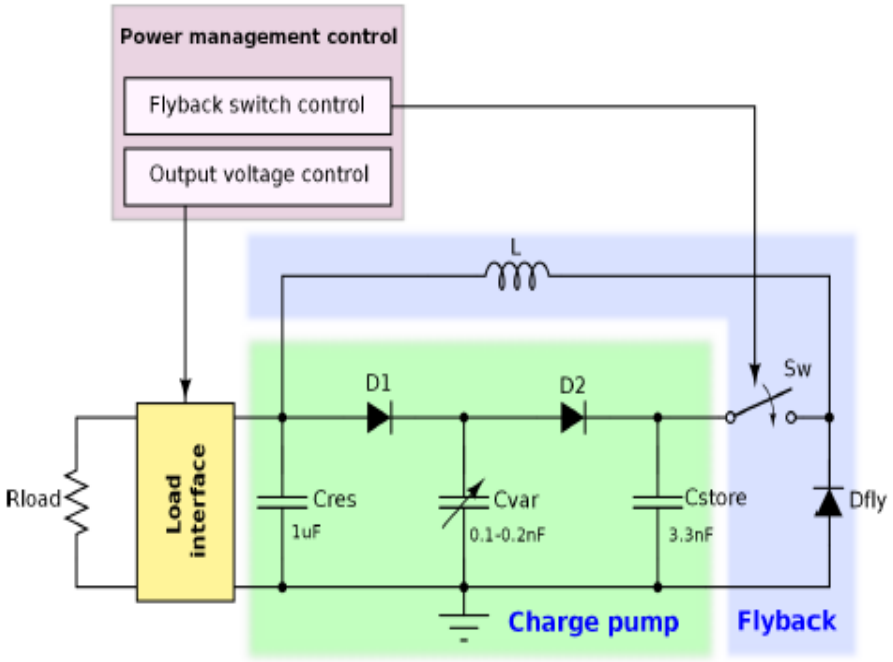


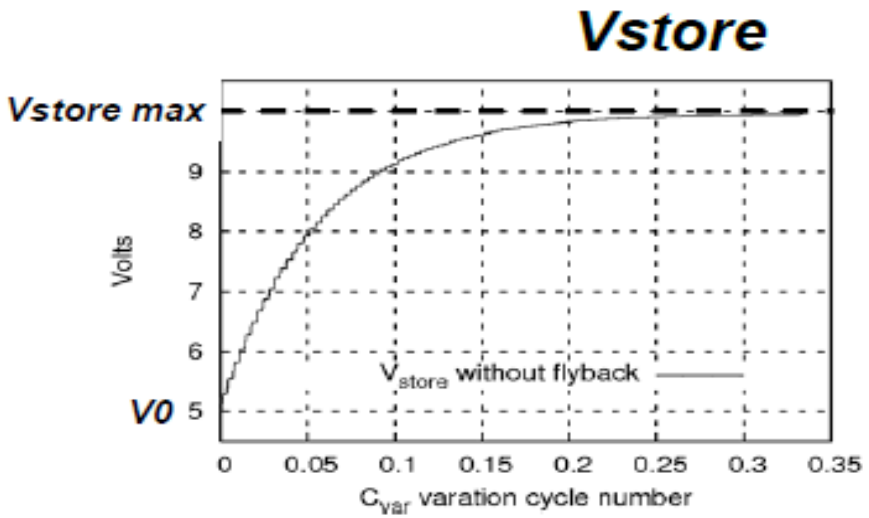
Human body

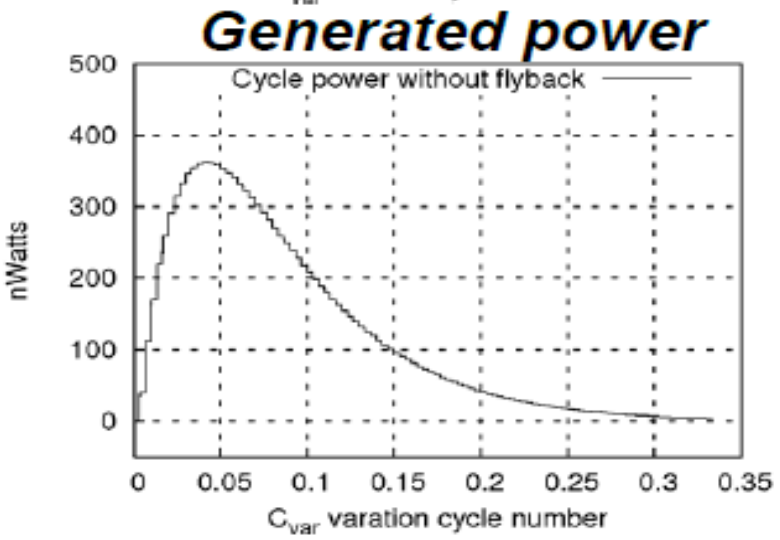
Vibrating structures

Environment surveillance

Harvester Operation



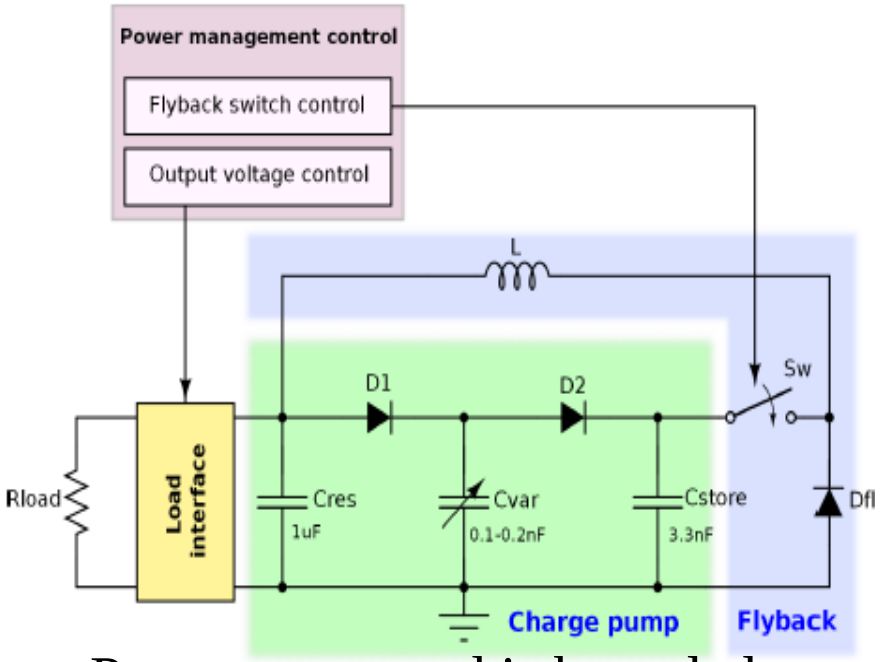


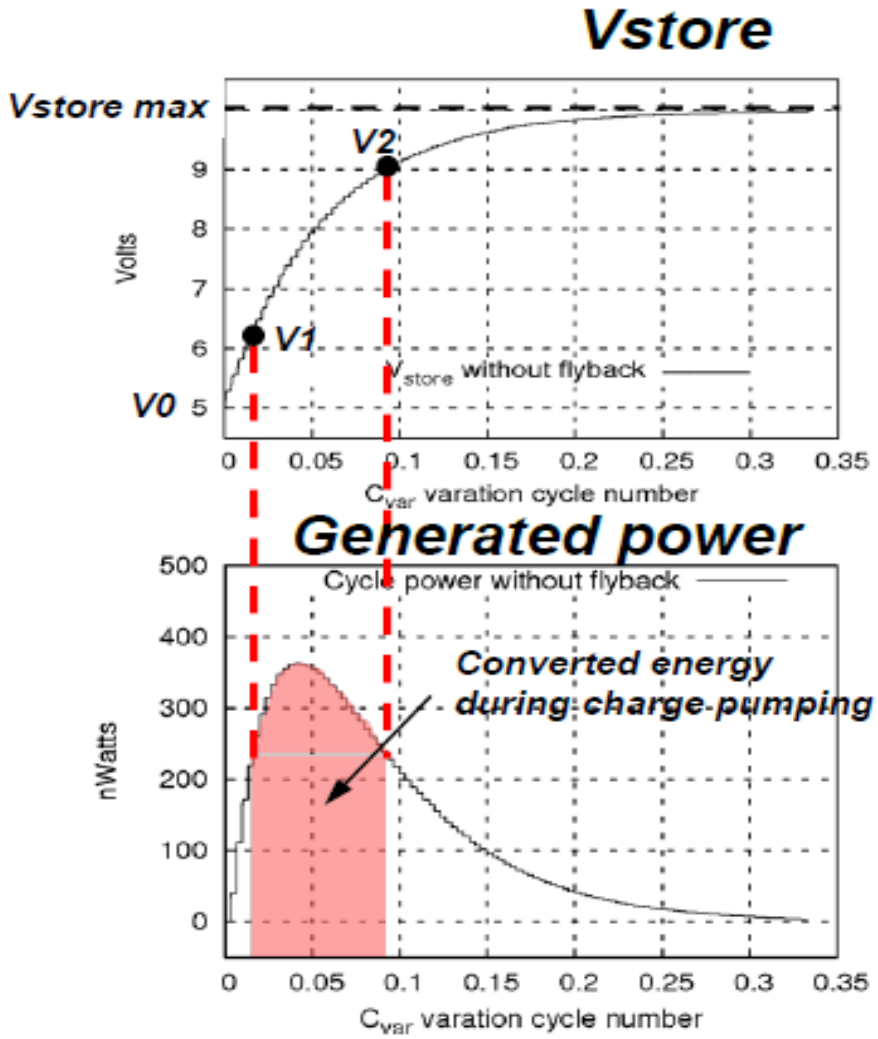


- U_{store} increases quickly –average power increases and becomes maximal

- U_{store} saturates –average power decreases and drops to zero.

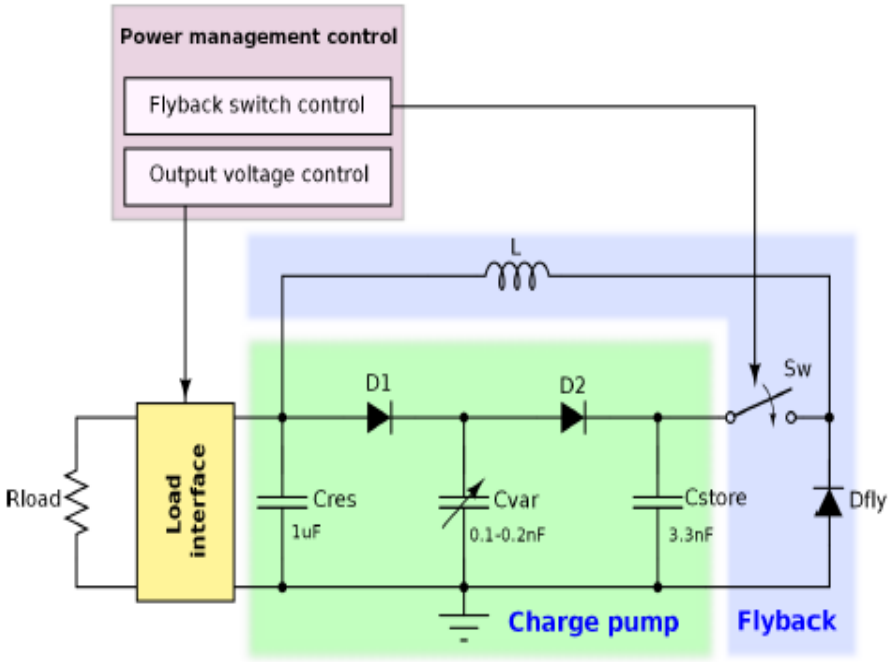
Harvester Operation

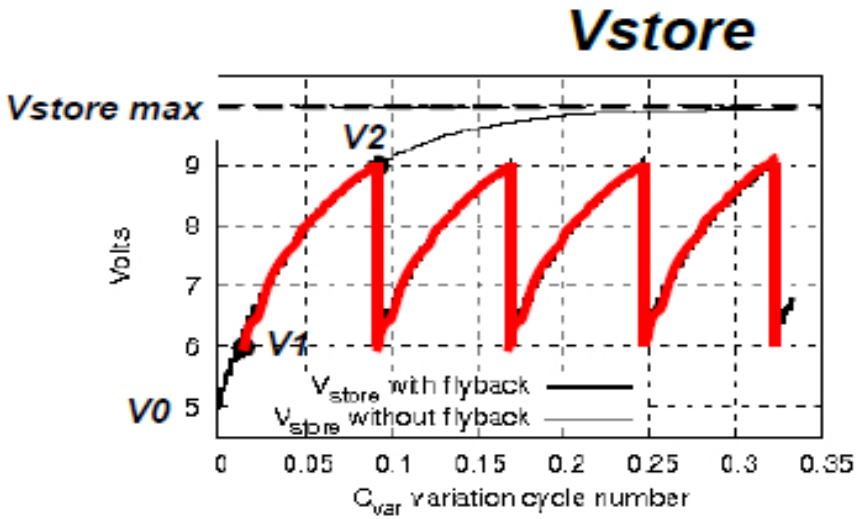


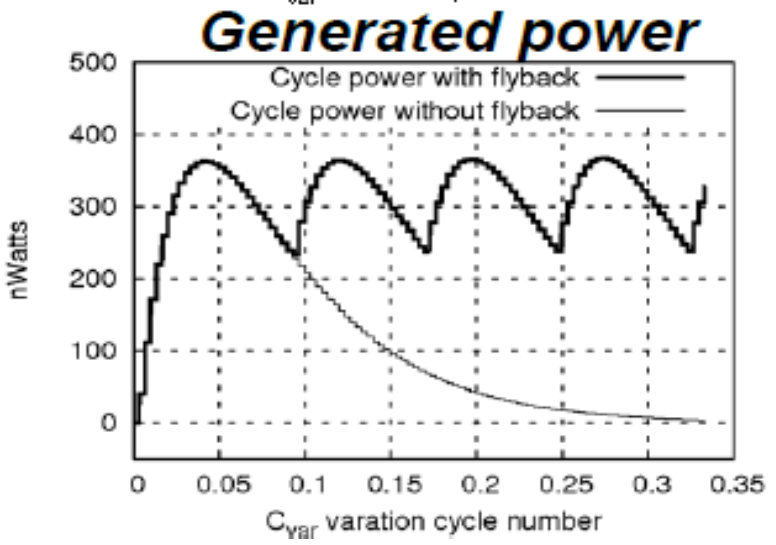


- Power converted is bounded between two limits U_1 and U_2.
- Power converted must be stored in C_{res}.
- The output power of the harvester equals 20 uW when Ustore=50V.

Smart Power Management

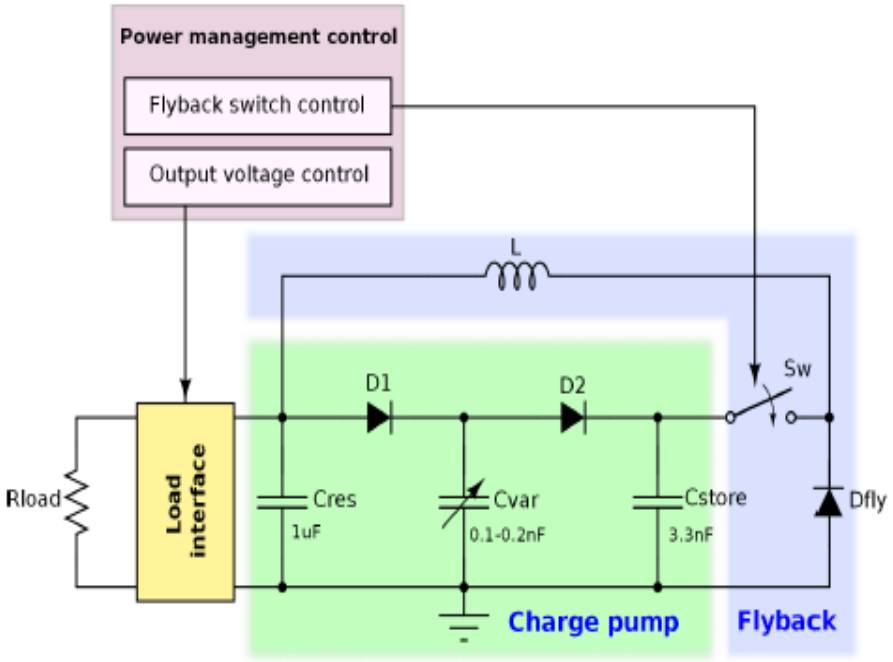


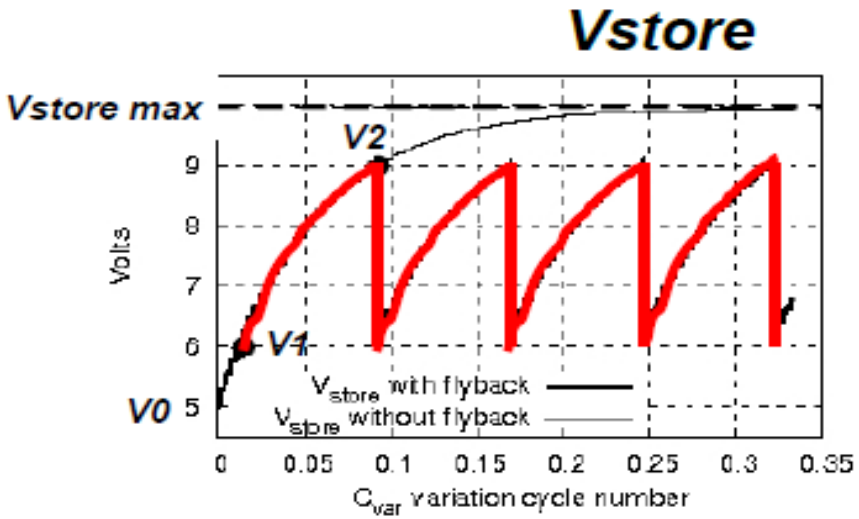


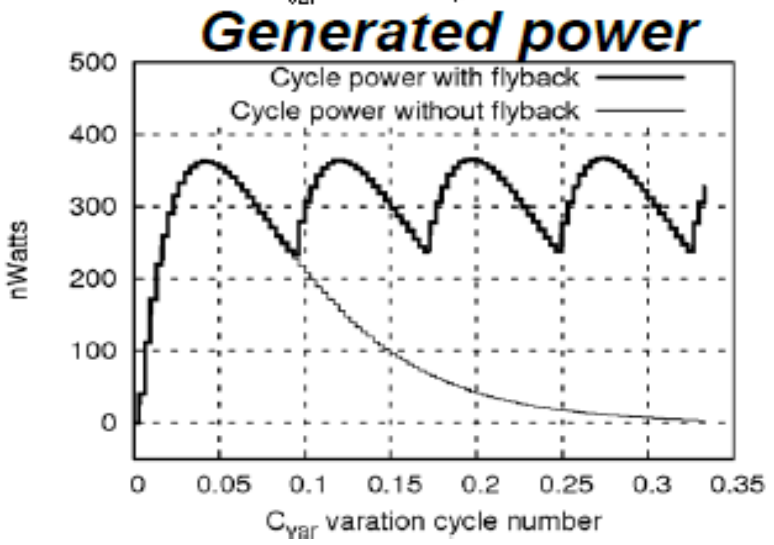


- Commutation parameters U_1 and U_2 are calculated with empirical formula.
- U1 and U2 depends on the initial voltage U_{res} and Ustore in saturation.

Smart Power Management





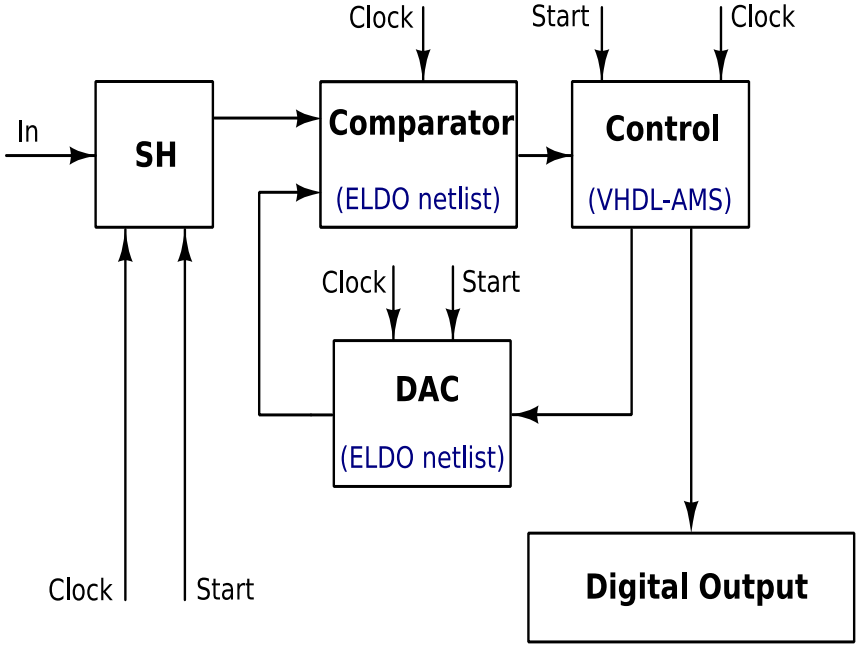


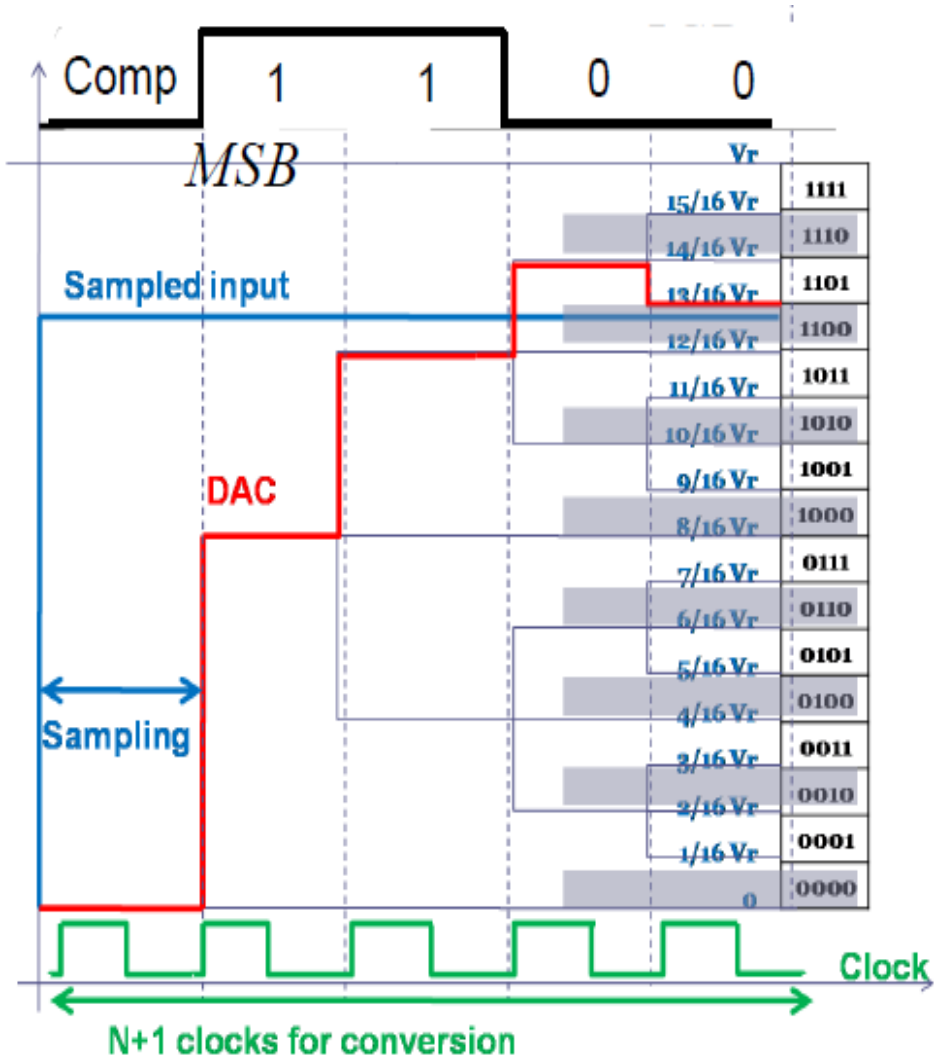
- Calibration cycles are needed
- Analog to Digital Converter is needed

Work Goals

- Create an interface between the harvester and the smart power management.
- Measure initial voltage U_{res} and U_{store} in saturation to calculate U_1 and U_2
- Calibration mode.
- Estimate the power consumption of this interface.

Successive Approximation ADC



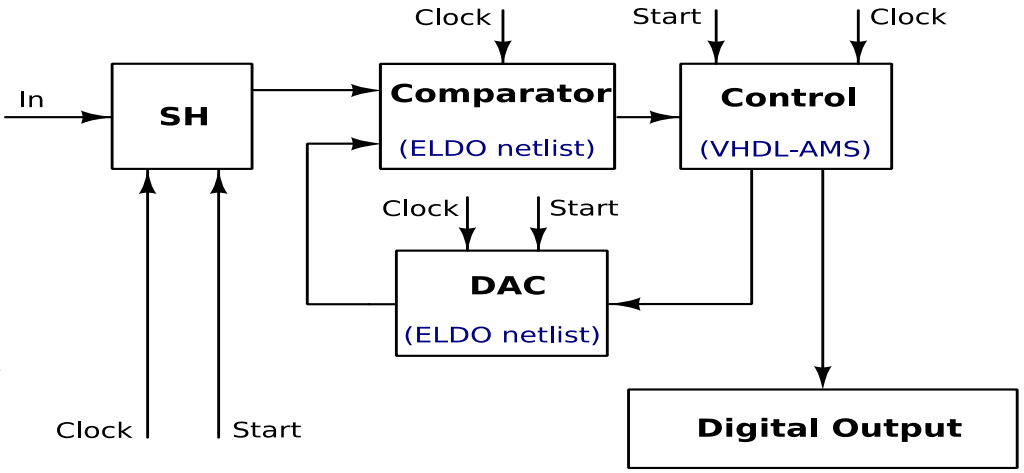


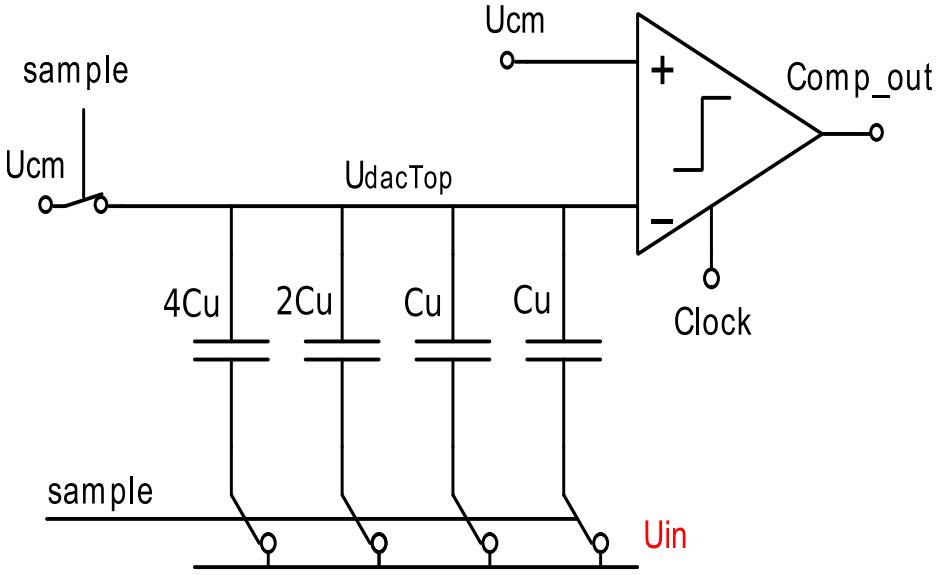
- The successive approximation ADC is known as one of the best candidates in terms of low power

- The model contains VHDL-AMS block and ELDO netlist blocks using 0.35um AMS technology

Successive Approximation ADC Architecture

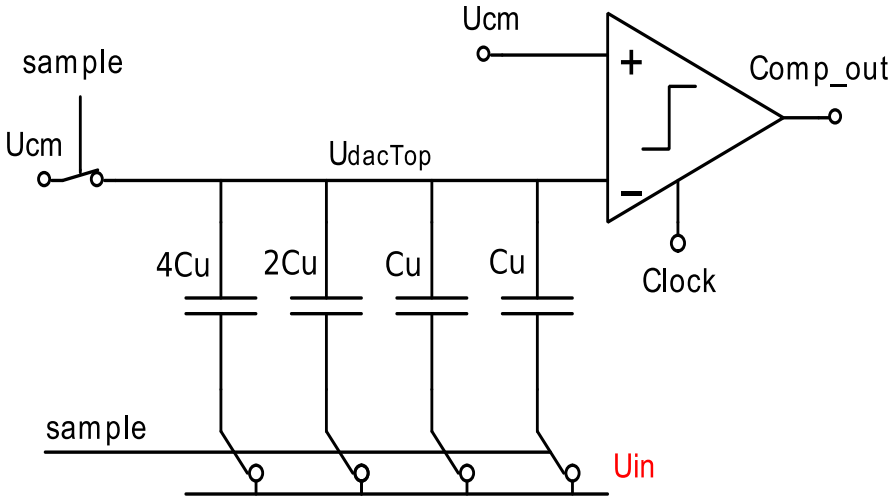
- The signal is sampled by the DAC
- DAC output is compared with U_{cm}
- The Comparator output is connected to SAR control.
- SAR controls the switches in the DAC
- 3 references used: U_{dd}, $U_{cm}=U_{dd}/2$ and *gnd*.
- SAR ADC modes: sampling mode, inversion mode and charge redistribution mode



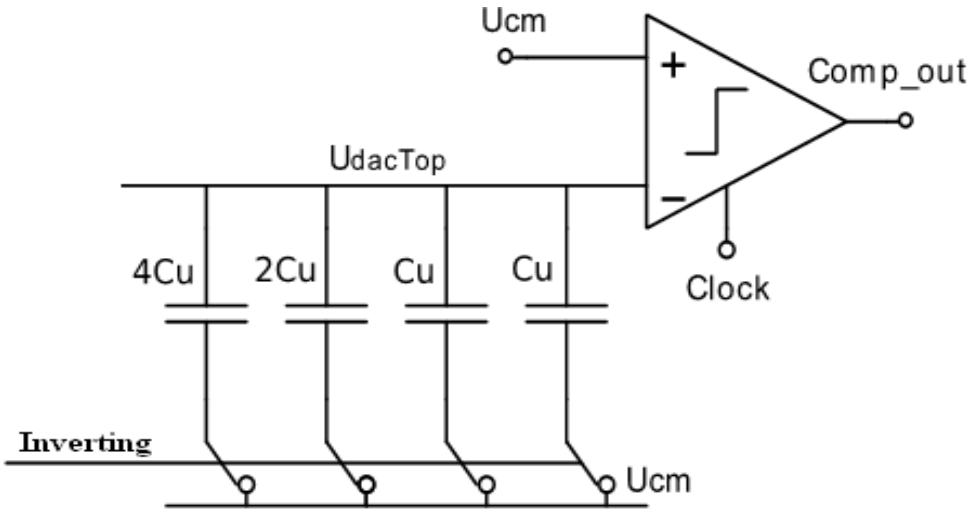


Successive Approximation ADC Modes

- The sampling mode:
  - In the first half of the first clock cycle.
  - DAC Bottom plates are connected to U_{in} .
  - DAC upper plates are connected to U_{cm} .
  - $U_{dacTop} = U_{dd} / 2$

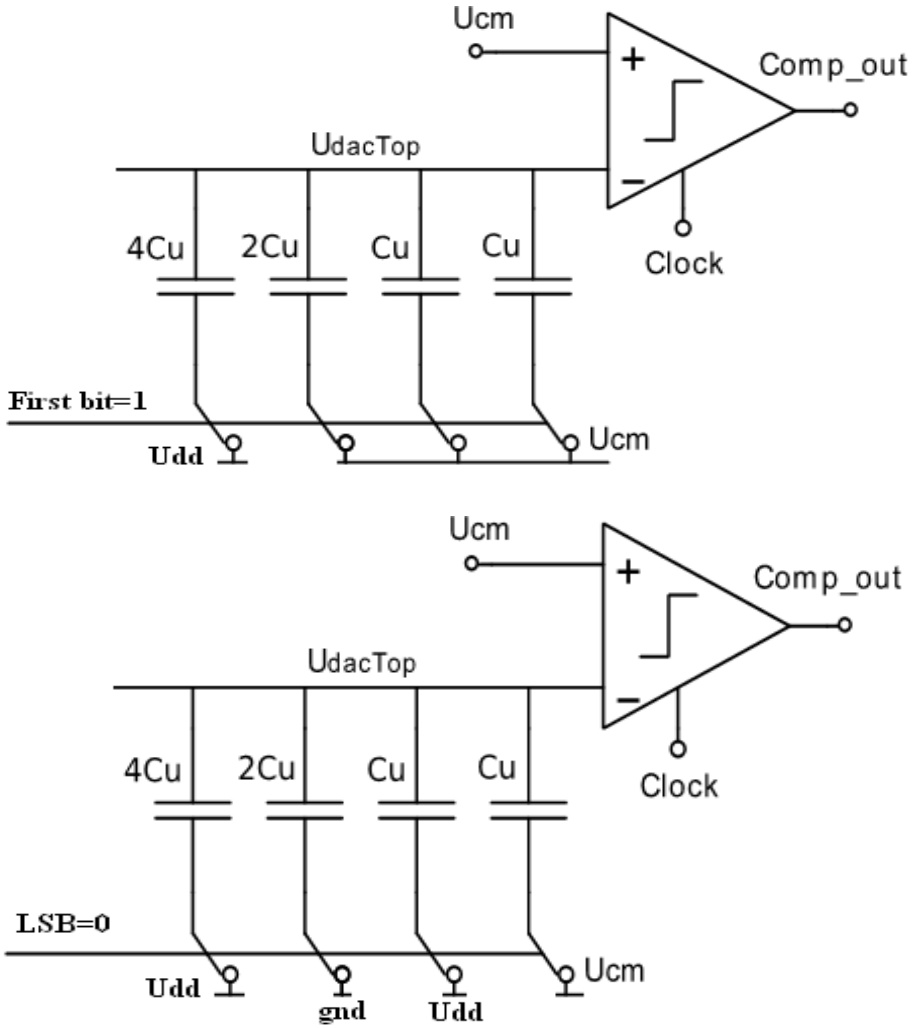


- The inversion mode:
  - In the second half of the first clock cycle
  - DAC Bottom plates are connected to U_{cm}
  - $U_{dacTop} = U_{dd} - U_{in}$
  - The output of the comparator represents the MSB



Successive Approximation ADC Modes

- The charge redistribution mode:
  - In the next N clock cycles.
  - Depending on the Comparator, the SAR control connects the DAC bottom plates to U_{dd} or gnd.
  - At the end of the charge redistribution mode, the digital output bits correspond to input signal .
- The SAR ADC used in the harvester conditioning circuit:
  - 8 bits
  - Ts=3.6ms and internal clock=2.5Khz



Comparator

•The comparator is designed using 0.35um technology (AMS035).

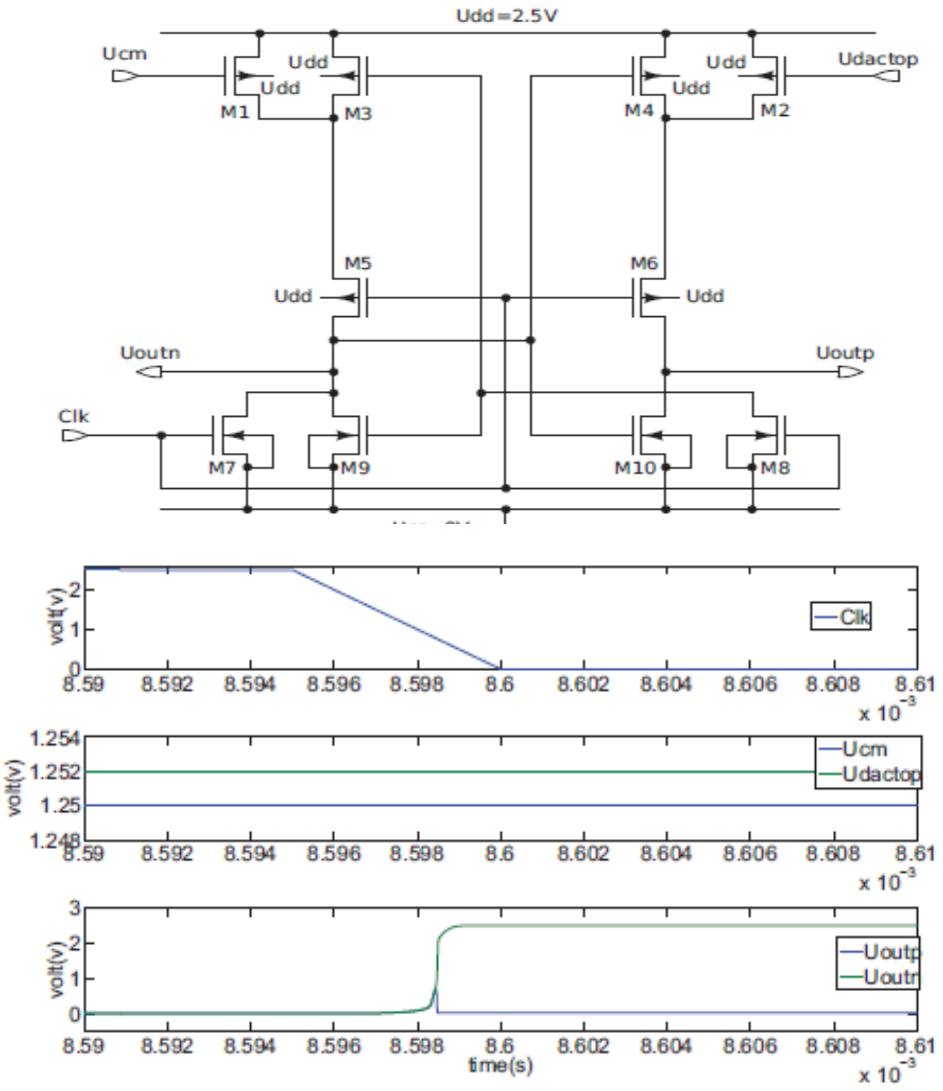
•Udd=2.5V

•The comparator is the only analog part in the SAR ADC architecture.

•It is a semi-dynamic clocked architecture.

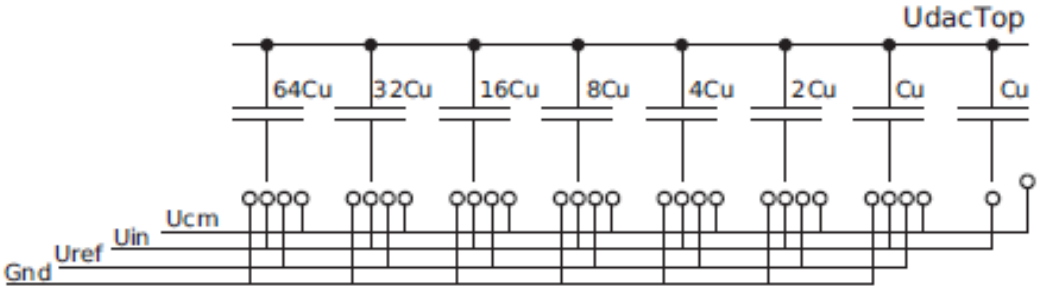
•The transistors M1 and M2 are used to amplify the input signal.

•The transistors M3, M4, M9 and M10 implement a couple of inverters connected to be a flip-flop.

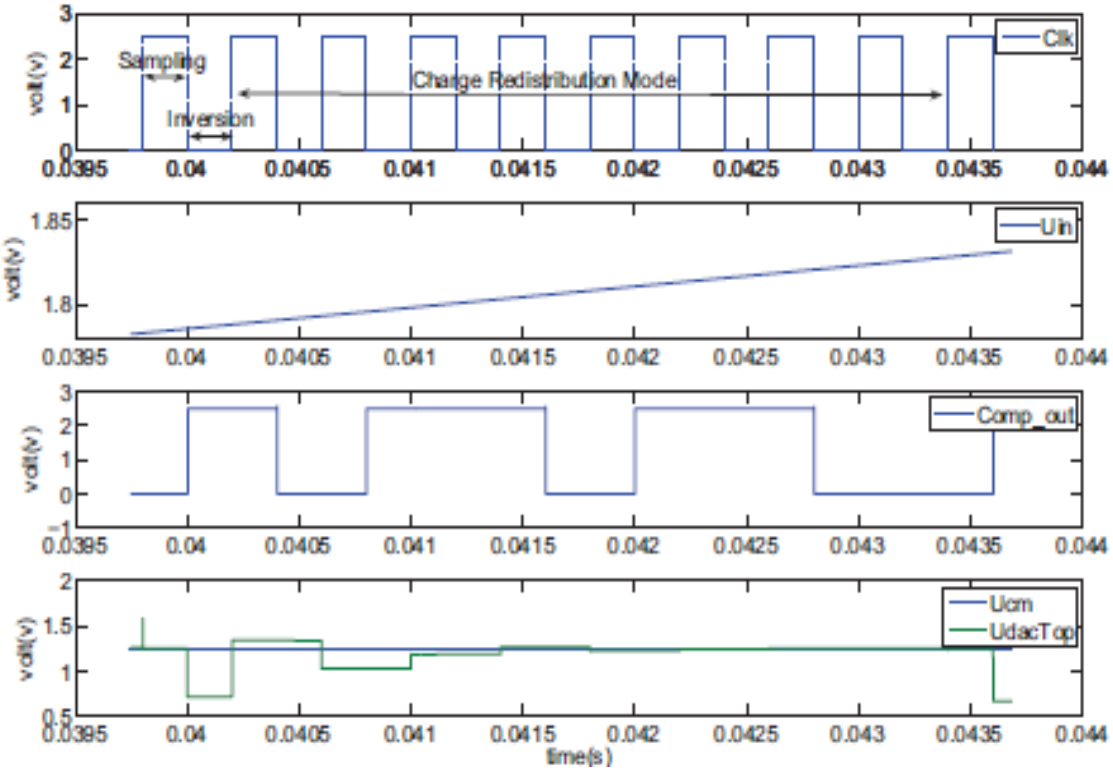


DAC and The SAR Control

- The DAC netlist:
  - Total capacitance=$(2^{N-1})C_u$
  - Binary weighted capacitor array.



- SAR control VHDL-AMS Model:
  - Produces the control signals for the switches during the 3 modes.
  - Produces the output bits at the end of each conversion



SAR ADC into The Harvester Conditioning Circuit

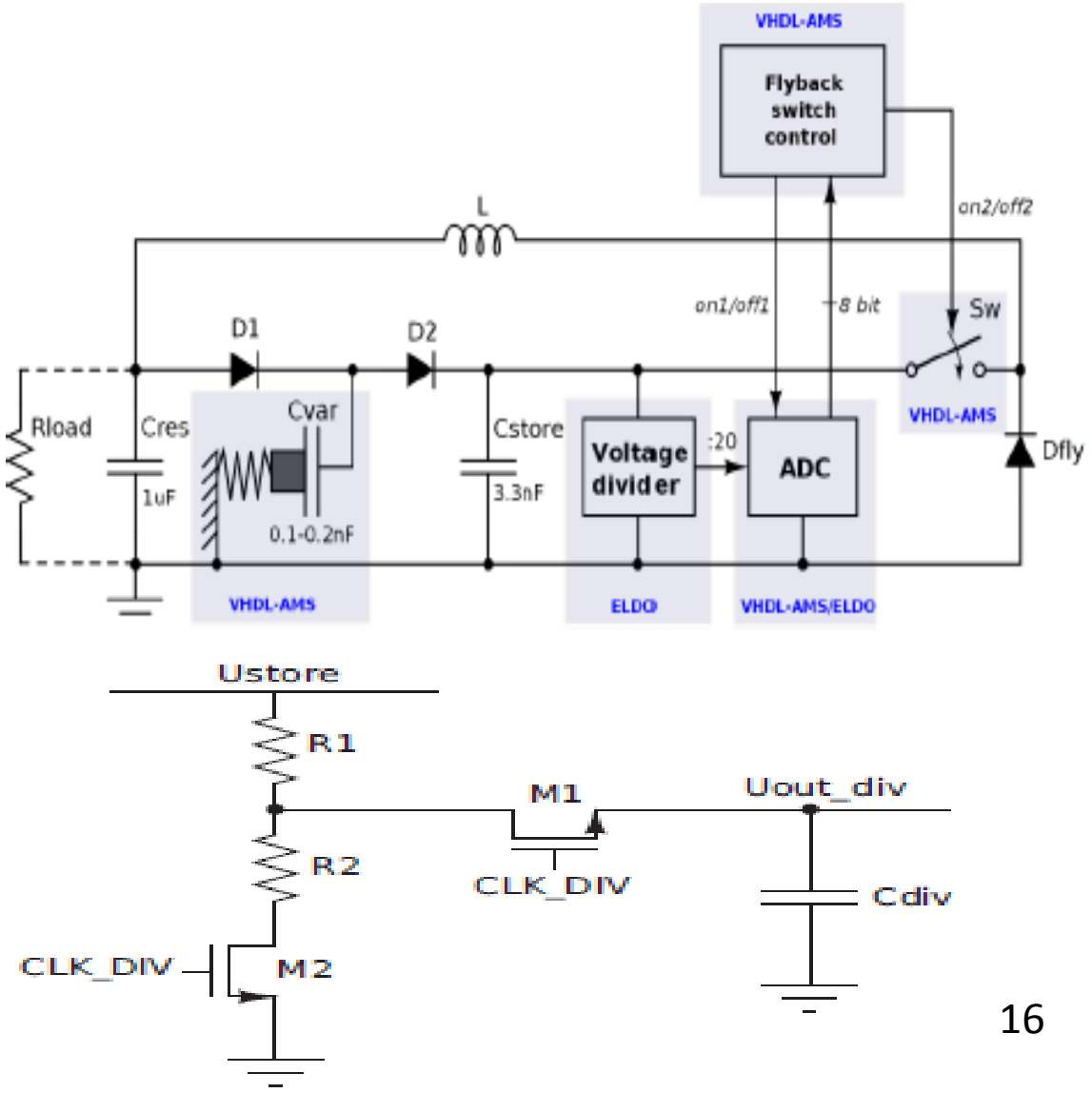
•The SAR ADC input is U_{sotre} divided by 20 ($U_{store\ max}/U_{dd}$).

• SAR ADC output bits are connected to the Flyback switch control.

•Flyback switch control enables the SAR ADC only in the calibration cycle.

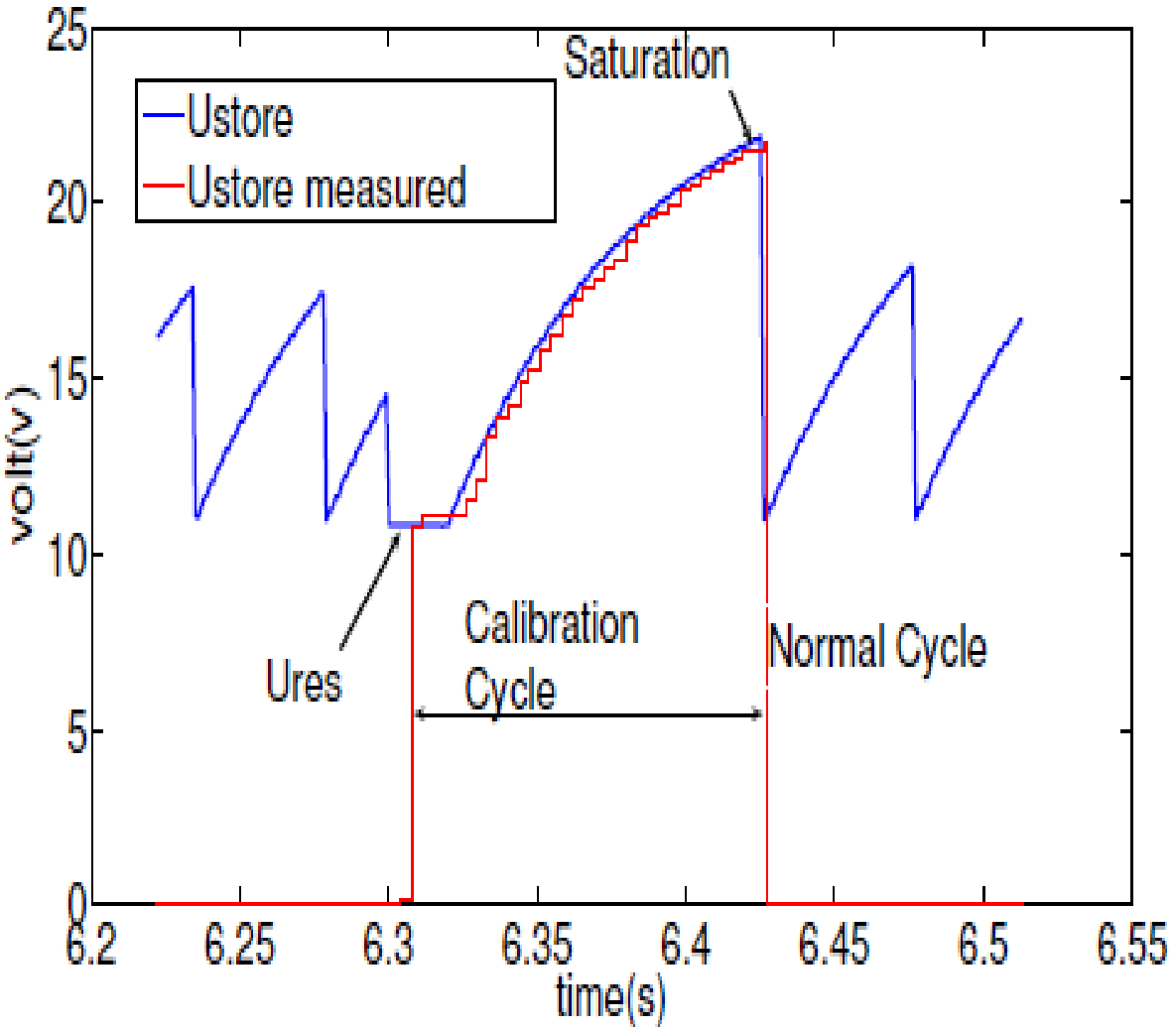
•The Calibration cycle repeats rarely.

•The whole harvester system model is mixed



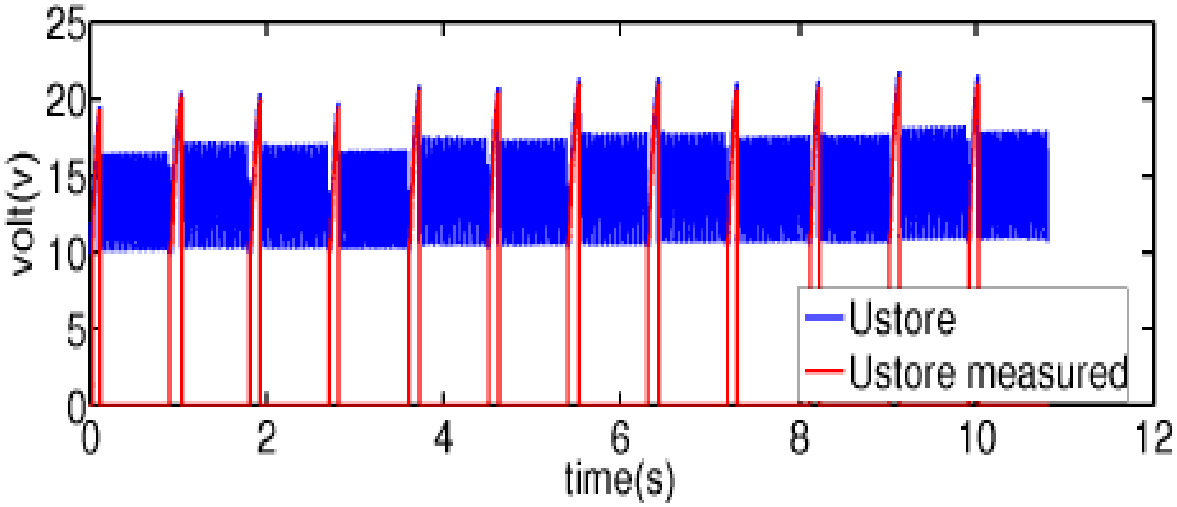
Calibration Technique

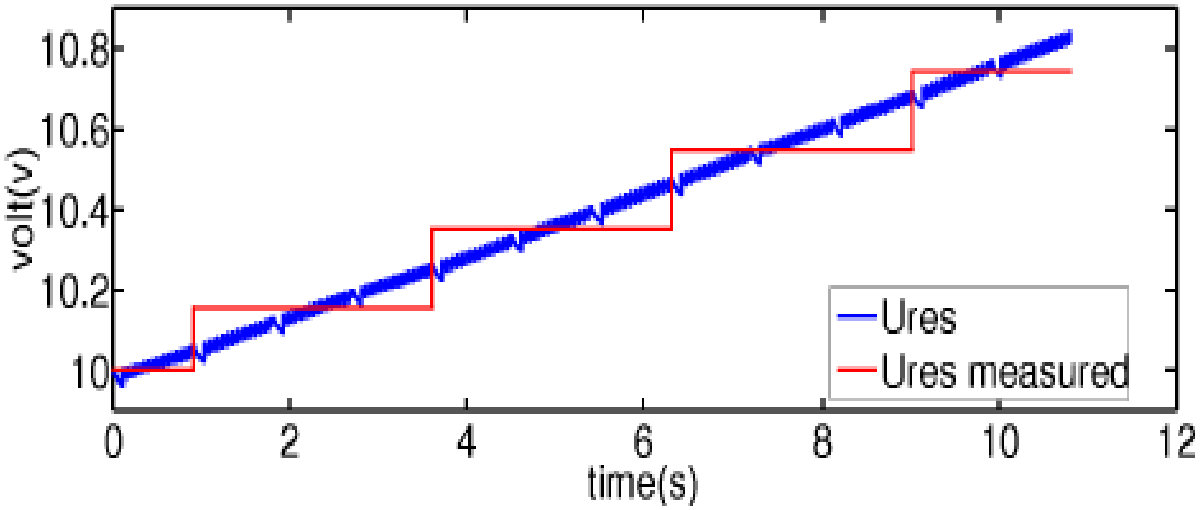
- Calibration is started.
- Measuring initial voltage U_{res}.
- Measuring U_{store} in saturation.
- Resolution=$(2.5/2^8).20$= 0.2 V.
- Flyback disables the SAR ADC.
- U_1 and U_2 are calculated.
- Normal cycles are started.



Model Results

- Example: long time simulation 11 s.
- Calibration cycle repeated every 900ms.
- U_{res} is measured at the beginning of every calibration cycle.
- U_{res} increases during normal mode.





Conclusion

- Interface between the Harvester conditioning circuit and the flyback control is done.

- The estimated power consumed of the SAR ADC is 1.25uW in one step conversion and the average power consumption equals to 180nW.
  - —The comparator is the dominant block in terms of power consumption.

- Calibration technique is implemented to achieve optimal electromechanical conversion .

Thank you