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Dependable System Lab [DSL]

Fault Injection in Mixed-Signal Environment Using Behavioral Fault Modeling in Verilog-A

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Outline

- Dependability
- Mixed Signal Flow
- Behavioral Fault Modeling
- Fault Models
 - Single Event Transient / Upset (SET/SEU)
 - Power Line Disturbance (PLD)
 - Electro Magnetic Interference (EMI)
- Results

Dependability and Reliability

- Dependability and Reliability
 - Not just words!
- An effective technique for the experimental **dependability evaluation**
- We propose a **simulation-based** fault injection method in mixed-signal environment.

Previous Fault Injection Tools

- Level of abstraction



HDL

The diagram consists of two overlapping circles. The left circle is light green and labeled 'HDL'. The right circle is light yellow and labeled 'Circuit'. The overlapping area in the center is a pale yellowish-green. Below the circles, the text 'solution: Mixed-signal fault injection' is written in a large, bold, yellow font with a drop shadow.

Does not include enough details
For accurate modeling

Circuit

Too slow, too old.
cannot include verification method like
testbenches, etc.

solution:
Mixed-signal fault injection

Flow

- Fault injection and simulation is performed in Mixed-Signal environment
 - Performance/Accuracy tradeoff
 - More accurate than RTL simulation
 - Faster than SPICE simulation
 - Fault injection on SoCs with analog cores
 - PLLs, DLLs, SRAMs, ...

Flow

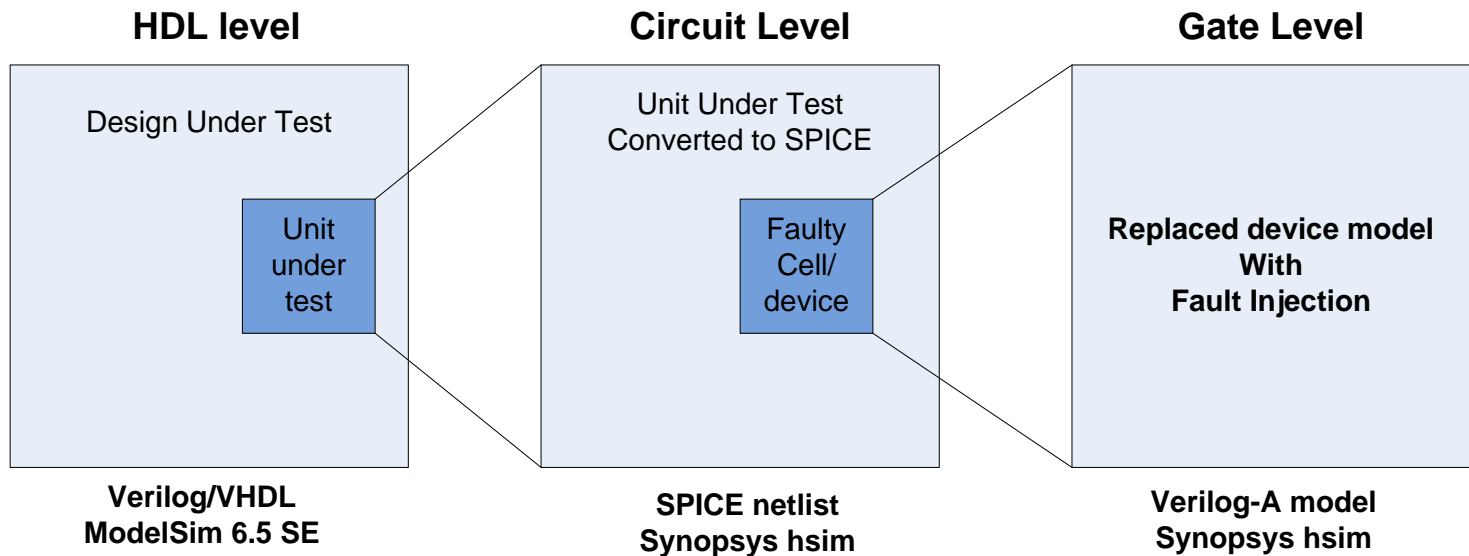
- SPICE simulation near the fault site:
 - accurate fault simulation
- HDL Simulation (elsewhere)
 - **Motive:** Most of the fault manifest themselves as an error outside the fault site
 - HDL simulation provides enough accuracy to continue simulation.
 - Original testbenches/verification scripts are intact
 - Faster simulation. Can compensate for the SPICE simulation penalty.

Fault Modeling

- We develop fault models in behavioral modeling languages (such as Verilog-A)
 - Easy modeling
 - Reduce development time
 - Accurate simulations
 - Access to internal nodes/ structure of transistor/electrical element

Tool-chain architecture

- Mixed-signal three-level of abstraction

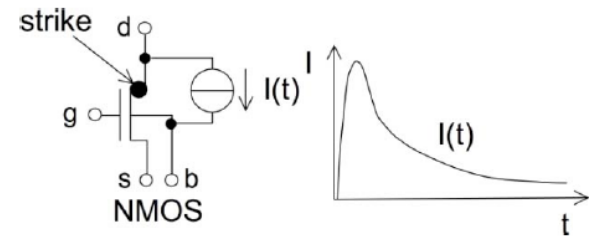
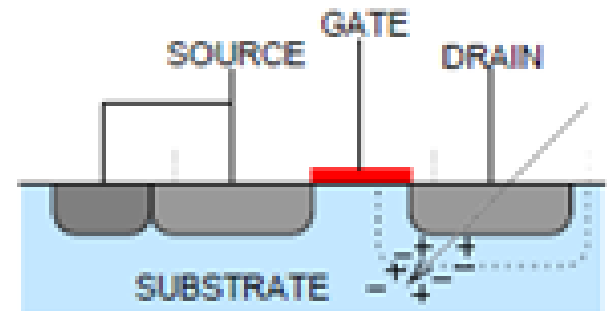
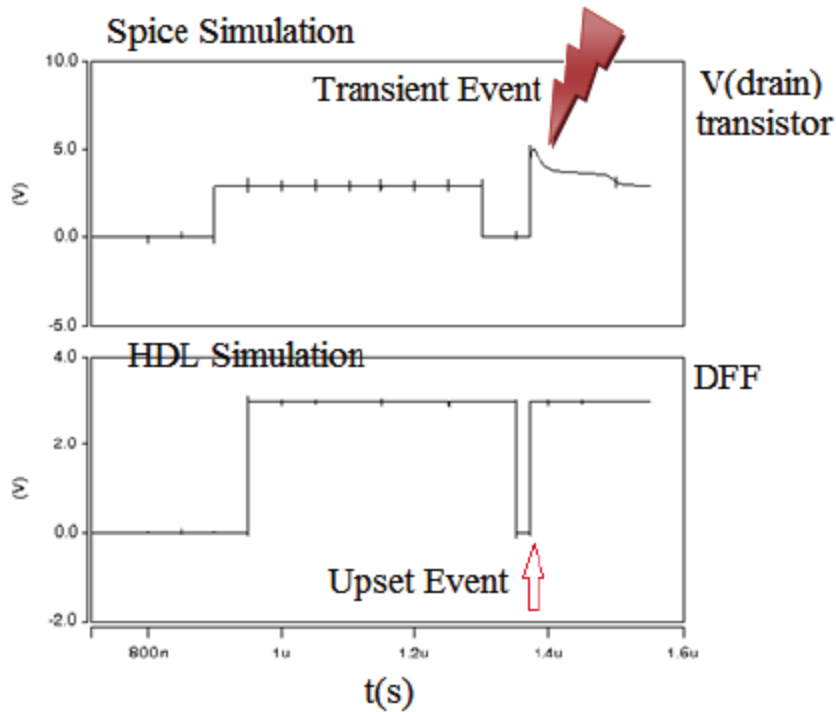


- Faults are embedded inside Verilog-A model.
- Resulted fault models are inserted to Circuit as an external component

Fault models

- Behavioral fault modeling
 - Single Event Upset (SEU)
 - Electro-Magnetic Interference (EMI)
 - Power Supply Disturbance (PSD)
- Our flow supports other fault models as well.

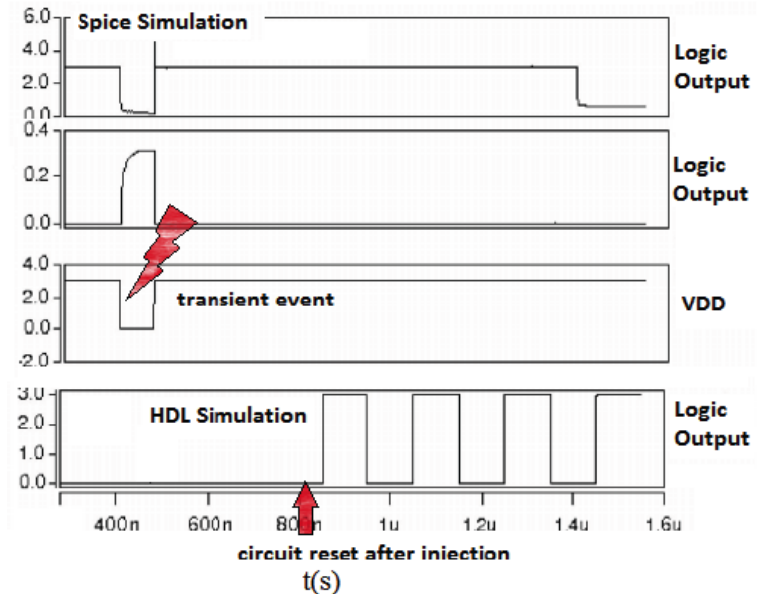
SET Fault Modeling



$$I(t) = I_0 \left(e^{-\frac{t}{\tau_a}} - e^{-\frac{t}{\tau_b}} \right)$$

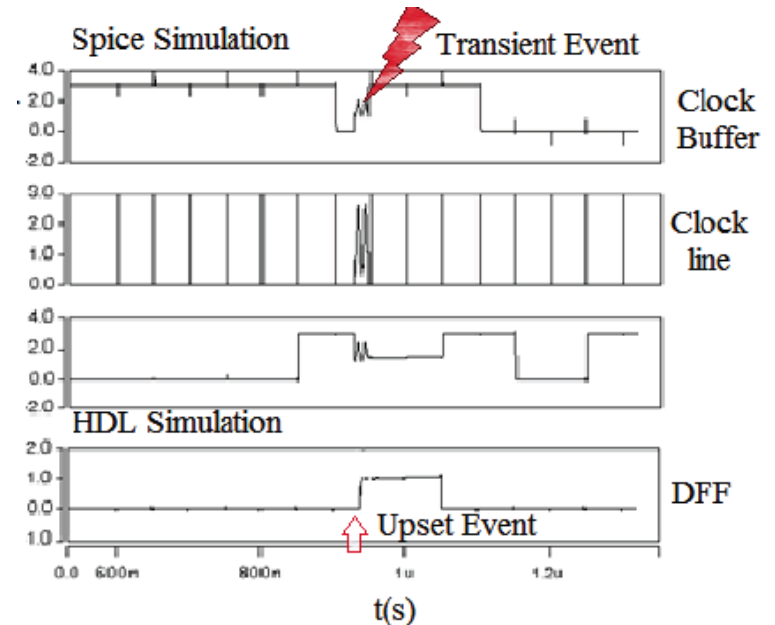
Power Line Disturbance Modeling

- Common PLDs:
 - Power supply noise
 - Overshoot, Undershoot
 - Ground Bouncing

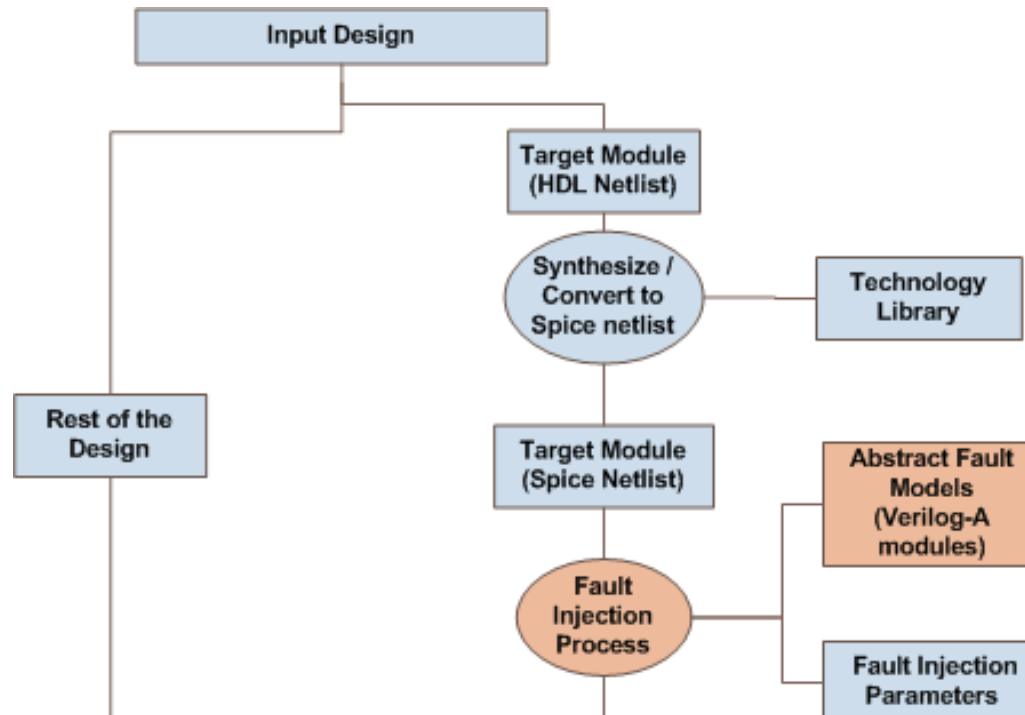


Electro-Magnetic Interference Modeling

- EM or RF induced interference
- Modeled as a Continues-wave RFI superimposed on specific nodes.
 - Input
 - Clock
 - ...



Flow: Initialization/Injection



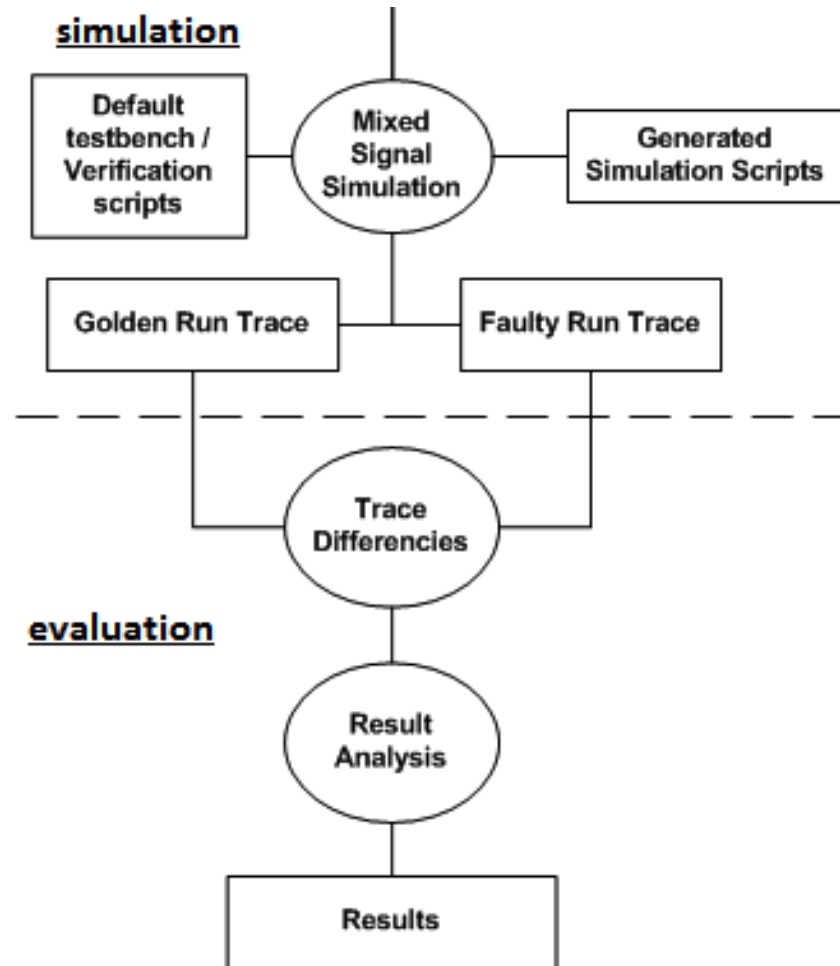
Abstract fault description for SET:

$$I(\text{drain, bulk}) <+ \text{TYPE} * Q/(\text{TO}-\text{TB})$$

$$* (\exp(-1 * ((\$abstime-\text{TINJECT})/\text{TO}))$$

$$-\exp(-1 * ((\$abstime-\text{TINJECT})/\text{TB})));$$

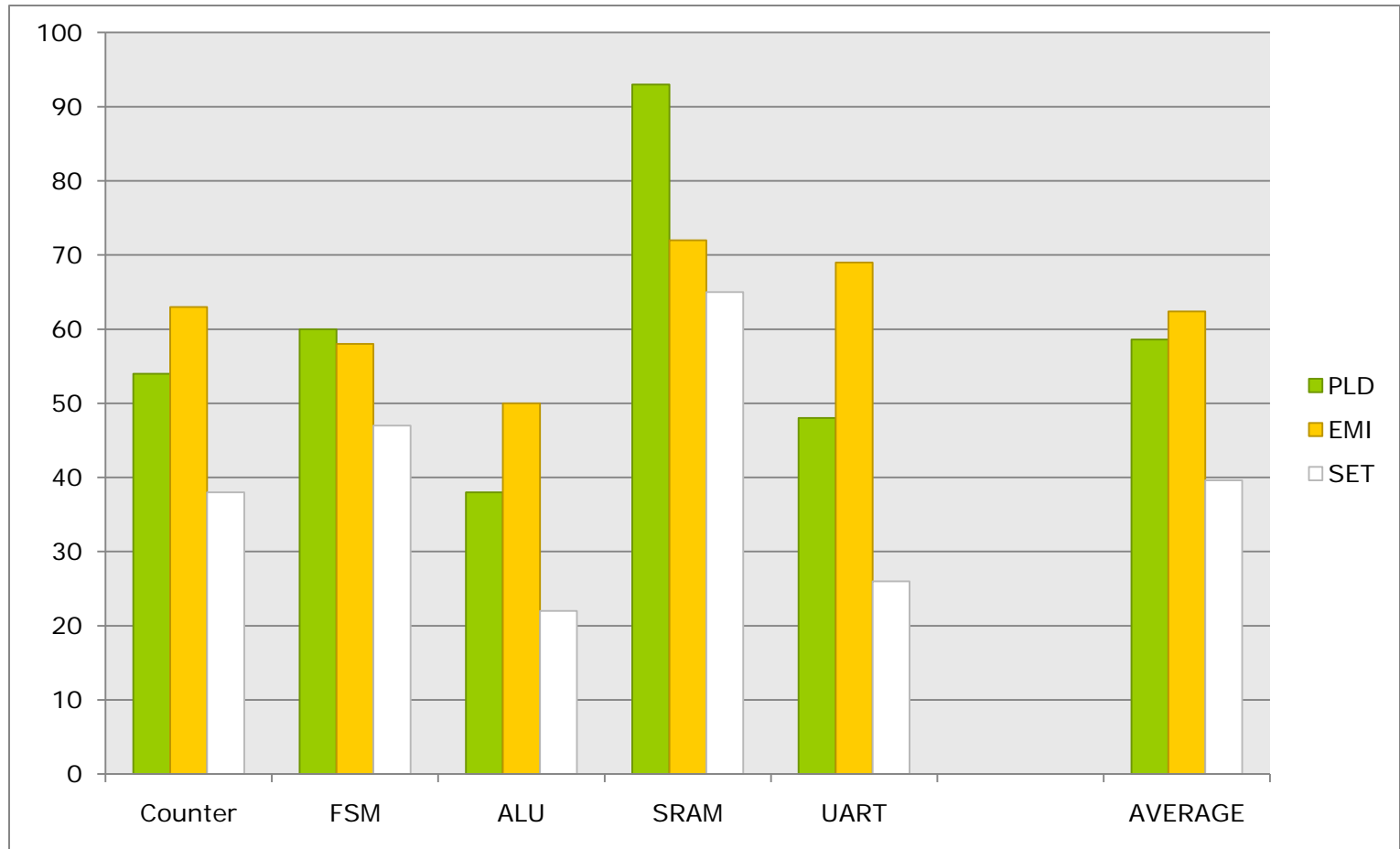
Flow: Simulation/Evaluation



Experimental Setup

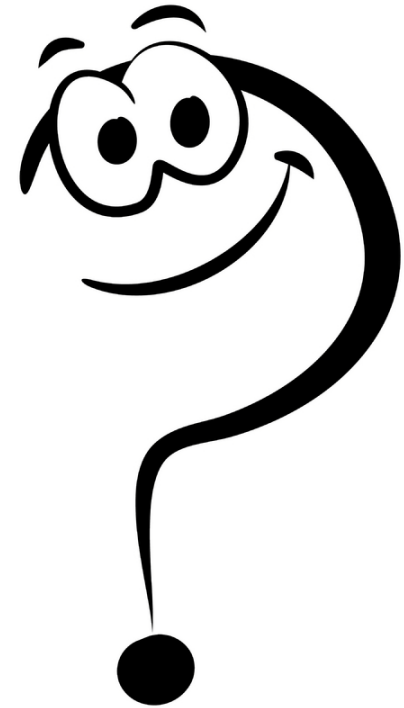
- We used the following 3rd party tools and IPs:
 - HDL Simulator: ModelSim 6.5 SE
 - Spice Simulator: Synopsys HSIM 2008.09
 - Process: TSMC 0.25 μ m
- Our fault characteristics:
 - **SET:** Q=10pc, with TO=TB=10ns , Random injection, Two exponential model
 - **EMI:** 100 MHz CW RF signal, V_{peak}= 0.5V , 100ns pulse envelope, Random injection
 - **PLD:** 100ns duration, Voltage shortage (from 2.5V to 0V) on VDD line, Random injection

Results of System Failures



Thank you!

- Questions?



- Thank you for your attention.